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ROLL NO. - 1701012006

Experiment NO. - 0

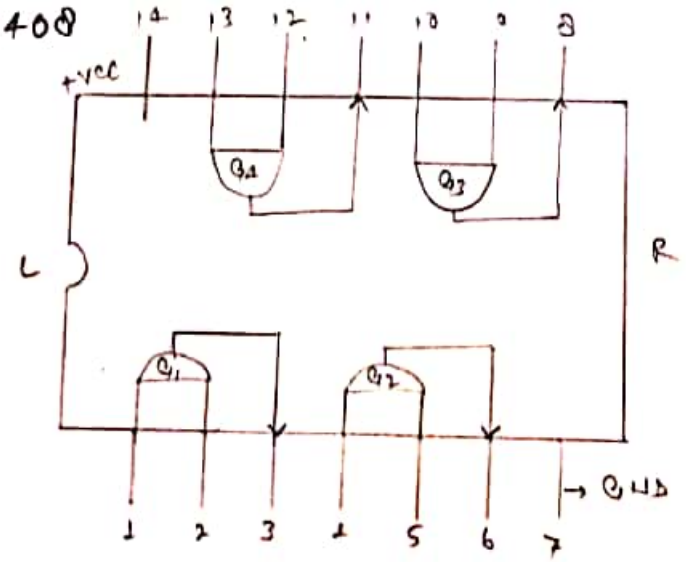
Object: Verify gates with the pin structures

Apparatus Required:

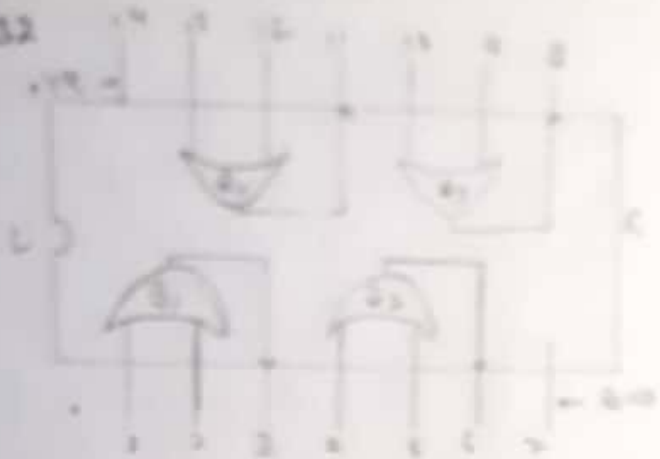
S.NO.	Instruments	Quantity	Discription
1	IC 7408	1	AND
2.	IC 7432	1	OR
3.	IC 7404	1	NOT
4.	IC 7400	1	NAND
5.	IC 7402	1	NOR
6.	Connecting wires	As required	

Circuit Diagram:

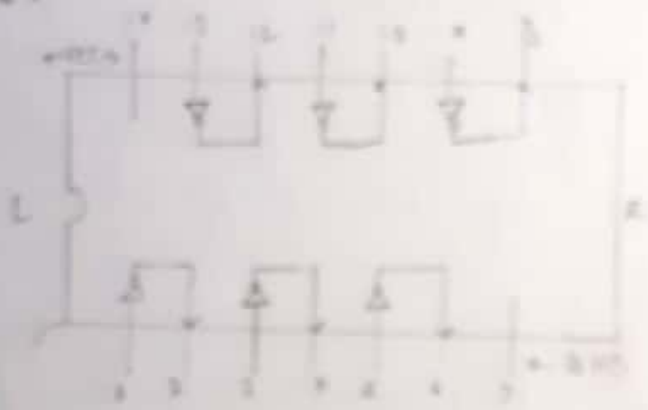
IC 7408



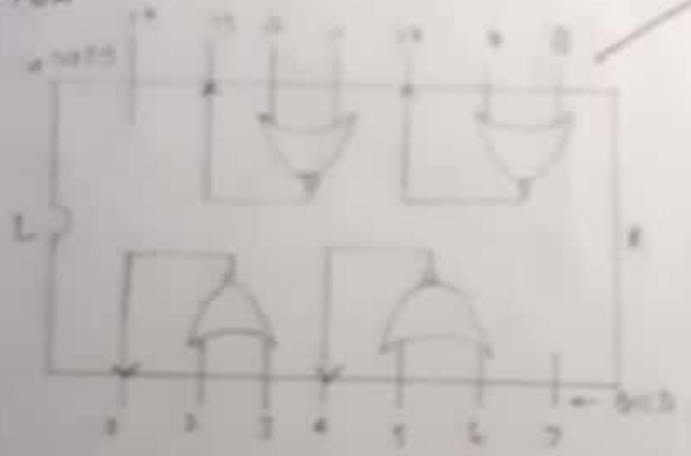
IC 7432



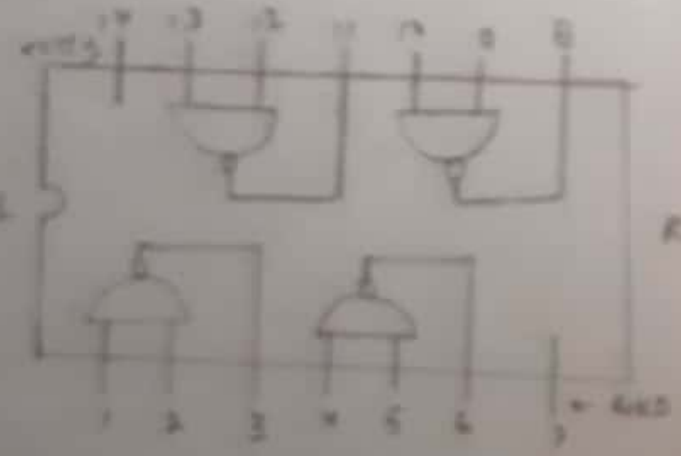
IC 7404



IC 7402



IC 7408



Theory:

IC7408: 7408 is a quad 2-Input AND Gates and contains 4 independent gate each of which performance the logic AND functions.

IC 7432: 7432 is a Quad 2-Input OR Gates and contains 4 independent gates each of which performed the logic operations.

IC7404: 7404 is a NOT Gate IC. It consists of six inverters which perform logical invert action.

IC 7400: 7400 is a Quad 2-Input NAND Gates that contains 4 independents gate each of which perform the logic NAND functions.

IC 7402: IC 7402 is a device contains 4 independent gate each of which perform the logic NOR performs the logic NOR operations.

Observation Table:

Truth table of AND gate (IC7408):

Input		Output
A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

Truth table of OR gate:

Input		Output
A	B	C
0	0	0
0	1	1
1	0	1
1	1	1

Truth table of NOT Gate:

Input A	output B
0	1
1	0

Truth table of NAND gate:

Input A	Input B	output C
0	0	1
0	1	1
1	0	1
1	1	0

Truth table of NOR gate:

Input A	Input B	output C
0	0	1
0	1	0
1	0	0
1	1	0

Result: All gates are verified

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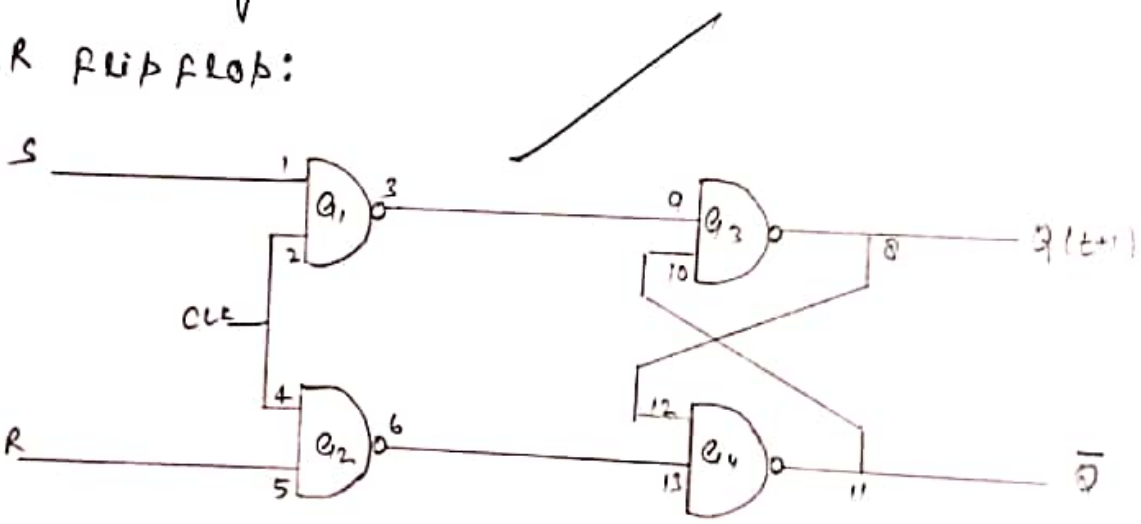
Experiment No. - 1

Object: Design and study of SR, JK, T and D flip flop using NAND gate.

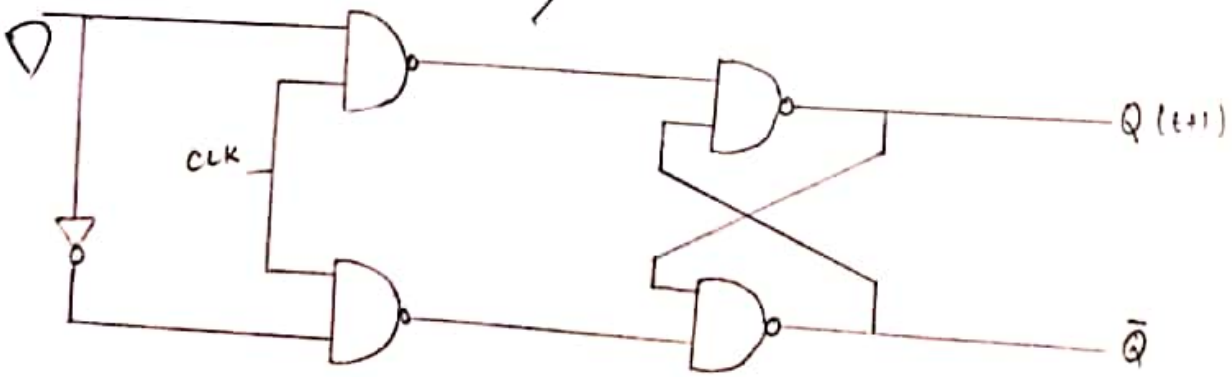
Apparatus required:
Connecting wires, IC 7400

Circuit Diagram:

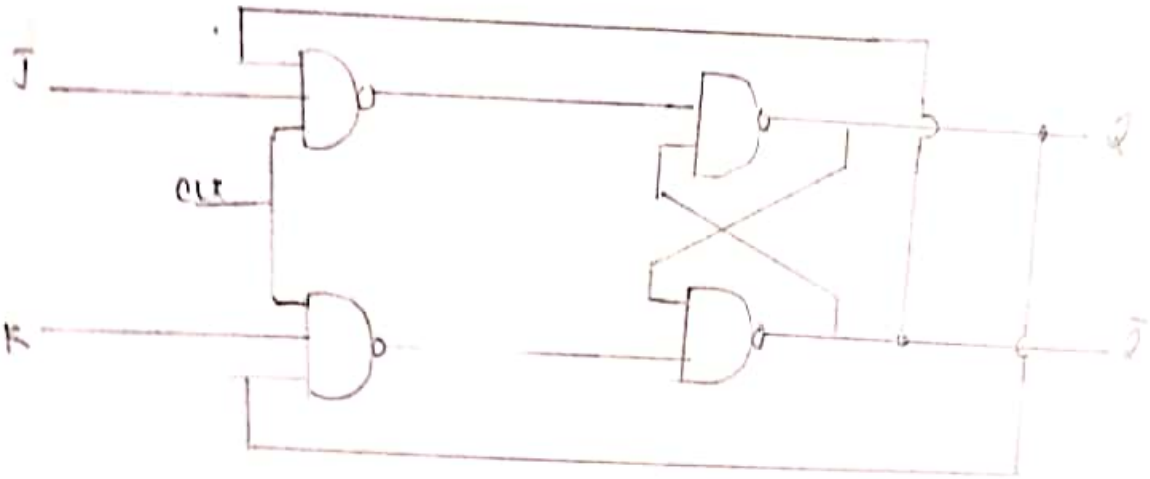
SR flip flop:



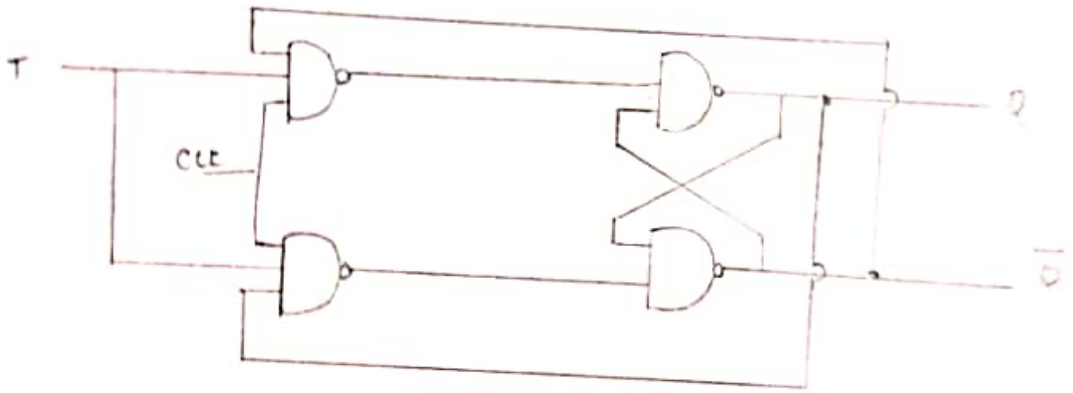
D flip flop



JK flip flop



T flip flop:



Theory:

Clocked SR flipflop: SR latch flip flop required the direct input but no clock. In the clocked SR F/F the F/F changes its state only when clock pulse is applied depending upon the inputs.

D flip flop: It is the modification of clocked SR F/F. In D flip flop single input is fed. At one gate the real input and at another its complement.

JK flip flop: One of the most useful and versatile flip flop is JK flip flop. If both inputs are 1 and the clock pulse is applied then the output will change its state. Regardless of previous condition.

T flip flop: It is also known as toggle flip flop. A method of avoiding intermediate state in RS F/F is to provide only one input. Toggle means to change in the previous state.

Observation:

Truth table of SR flip flop:

S	R	Q(t+1)
0	0	No change
0	1	0
1	0	1
1	1	Race

Truth table of D flip flop

D	Q(t+1)
0	0
1	1

Truth table of JK flip flop:

Inputs			Output
Q	J	K	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

Truth table of T flip flop:

Inputs		Outputs
Q	T	Q(t+1)
0	0	0
0	1	1
1	0	1
1	1	0

Results: Study and design of flip-flops is done.

1/2/19

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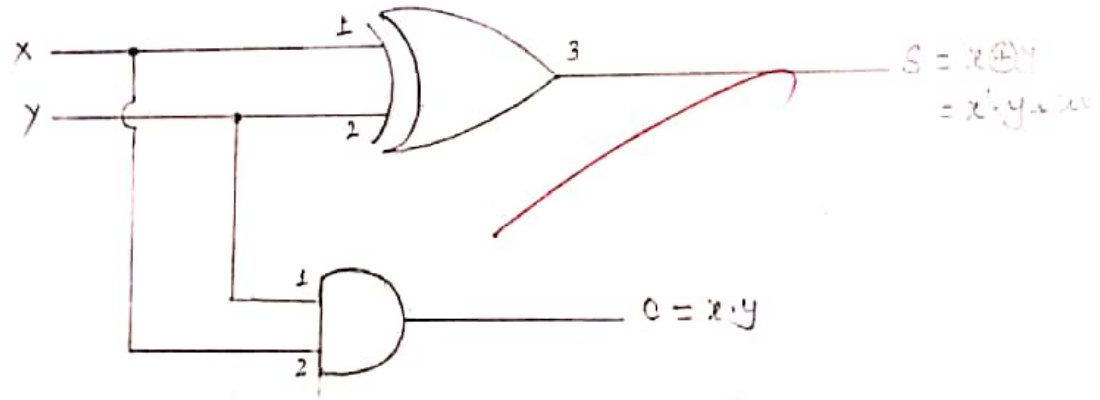
Experiment NO. 2

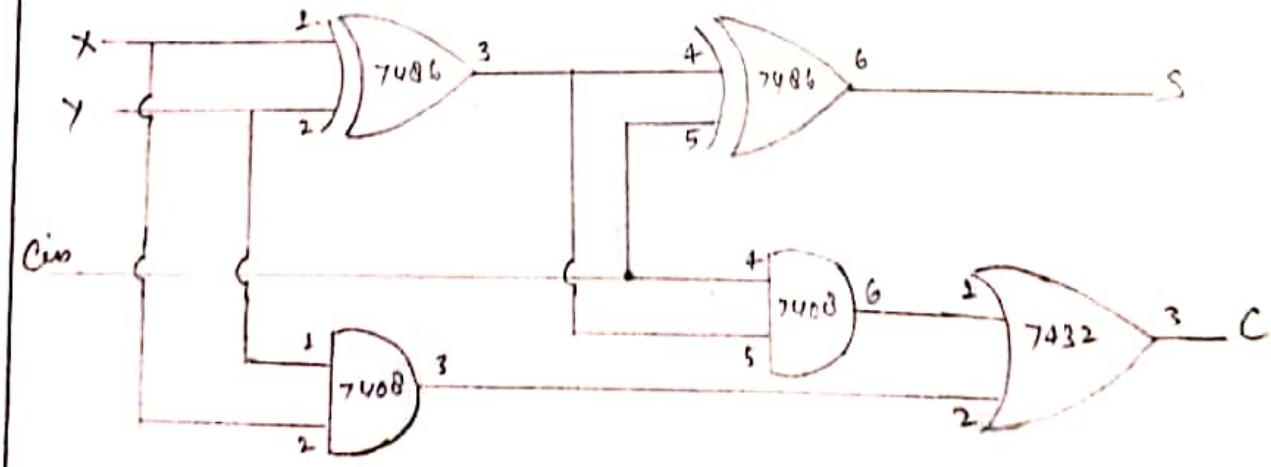
Object: Design and study of Half adder and full adder circuit.

Apparatus required: IC 7486, IC 7408, connecting wires.

Circuit diagram of half adder:



Circuit diagram of full adder:



Theory:

Half adder: A half adder is a type of adder an electronic circuit that performs the addition of numbers. The half adder is able to add two single binary digits and provide the output plus a carry value. It has two inputs and two outputs S(sum) and C(carry). The adder works by combining the operations of basic logic gates, with the simplest form using only a XOR and AND gate.

Full adder: A full adder is a digital circuit performs addition. full adders are implemented with logic gates in hardware A full adder takes two binary number plus a carry or overflow bit. The output is a sum and another carry bit. full adder is made from XOR, AND and OR gate. A full adder is effectively two half adder, an XOR and an AND gate, connected by an OR gate.

Observation table:

Truth table of half adder:

Input		Output	
X	Y	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Truth table of full adder:

INPUT			OUTPUT	
X	Y	Cin	S	C
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Result:- Design and study of half adder and full adder circuit is done.

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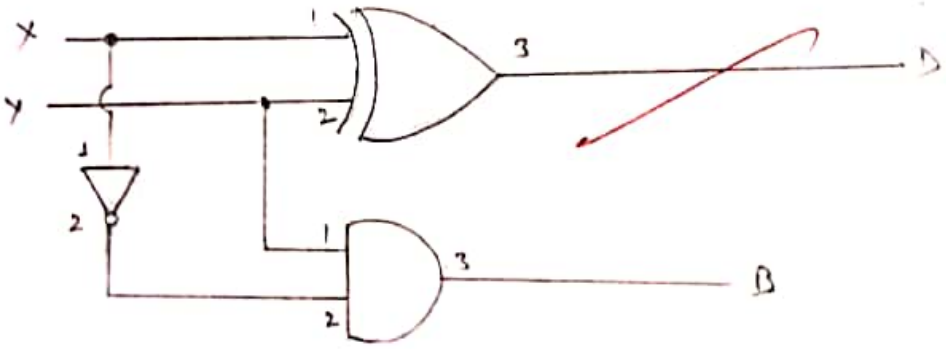
Experiment No. - 3

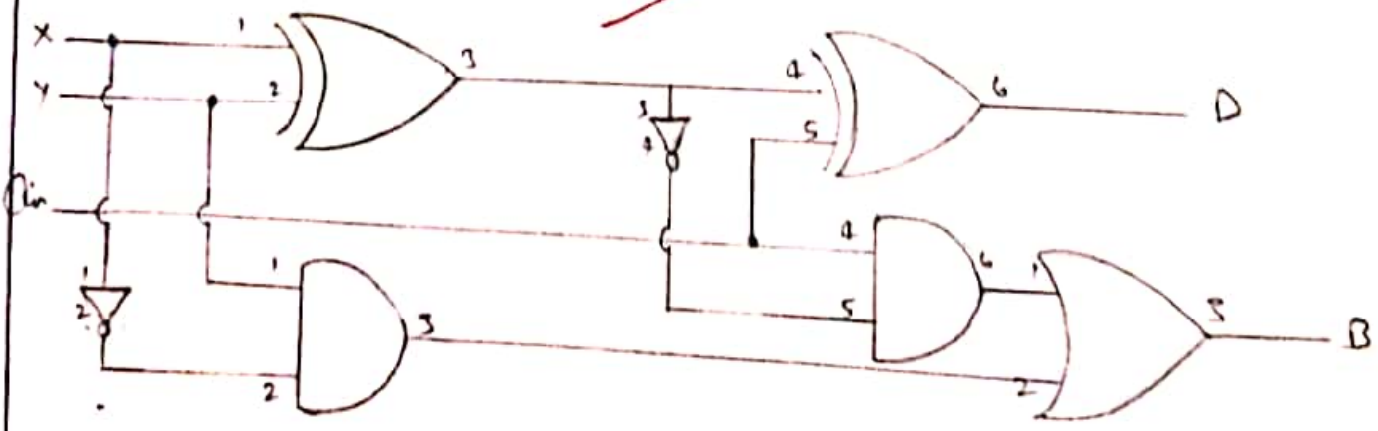
Object: Design and study of half subtractor and full subtractor.

Apparatus required: IC 7404, IC 7408 and IC 7486, connecting wires

Circuit diagram of half subtractor:



Circuit diagram of full subtractor:



Theory:

Half Subtractor: The half subtractor is a combinational circuit which is used to perform subtraction of two bits. It has two inputs X and Y and two outputs the difference D and borrow out Bout. The borrow out signal is set when the subtractor needs to borrow from the next digit in a multi-digit subtraction.

Full Subtractor: The full subtractor is a combinational circuit which is used to perform subtraction of three input bits X, Y and Bin. The full subtractor generates two output bits: the difference D and borrow out Bout. Bin is set when the previous digit is borrowed from X. Thus Bin is also subtracted from X as well as the Y. Like half subtractor, the full subtractor generates a borrow out when it needs to borrow from the next digit. Since we are subtracting X by Y and Bin a borrow out needs to be generated when X < Y + Bin. When a borrow out is generated, 2 is added in the circuit digit. Therefore $D = X - Y - Bin + 2Bout$.

Observation Table:

Truth Table of half subtractor:

INPUT		OUTPUT	
X	Y	D	Bout
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	0

Truth table of full subtractor:

INPUT			OUTPUT	
X	Y	Bin	D	Bout
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Result: Design and study of half subtractor and full subtractor is done.

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Branch - CSE
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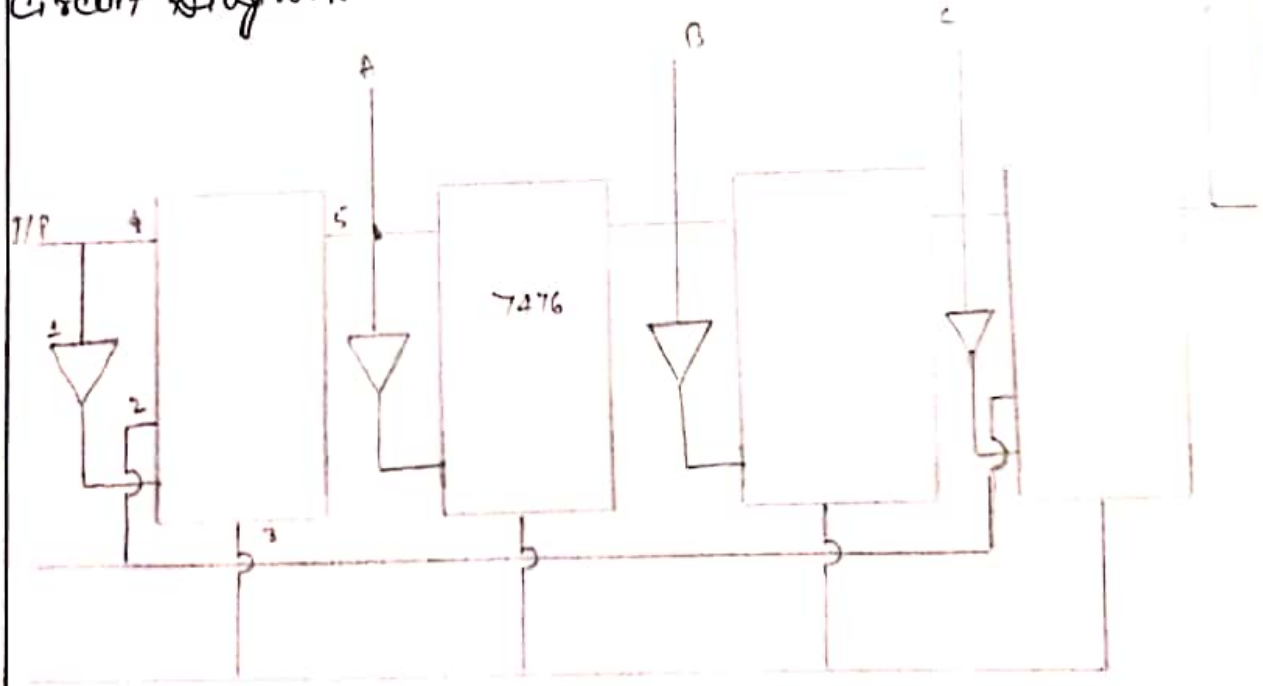
Experiment NO - 4

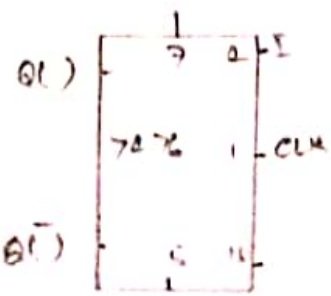
Object: Design and study of shift - register.

Apparatus required:

S.NO.	Instrument	Quantity	Specification
1.	Digital trainer kit	1	
2.	IC's	2	7476, 7404
3.	Bread Board	1	
4.	connecting wires	As per required	

Circuit Diagram:





V_{cc} = 5th pin

GND = 13th pin

Experiment NO -

1

Theory: Registers are main building blocks of the memory system. They are generally made up of flip-flop One flip flop can store one-bit of information. When a register is used to store binary information, it is called a memory register, when it is used to shift data to either left or right is called a shift register. A register capable of shifting in one direction only is a unidirectional shift register, and one that can shift in both directions are bi-directional shift register.

Observation Table: 4-Bit serial shift Register left to right

INPUTS			OUTPUTS			
			FF_A	FF_B	FF_C	FF_D
0	0	0	0	0	0	0
1	1	0	0	0	0	0
1	1	1	1	0	0	0
1	1	2	1	1	0	0
1	1	3	1	1	1	0
1	0	4	1	1	1	1
1	0	5	0	1	1	1
1	0	6	0	0	1	1
1	1	7	0	0	0	1
1	0	7	0	0	0	0

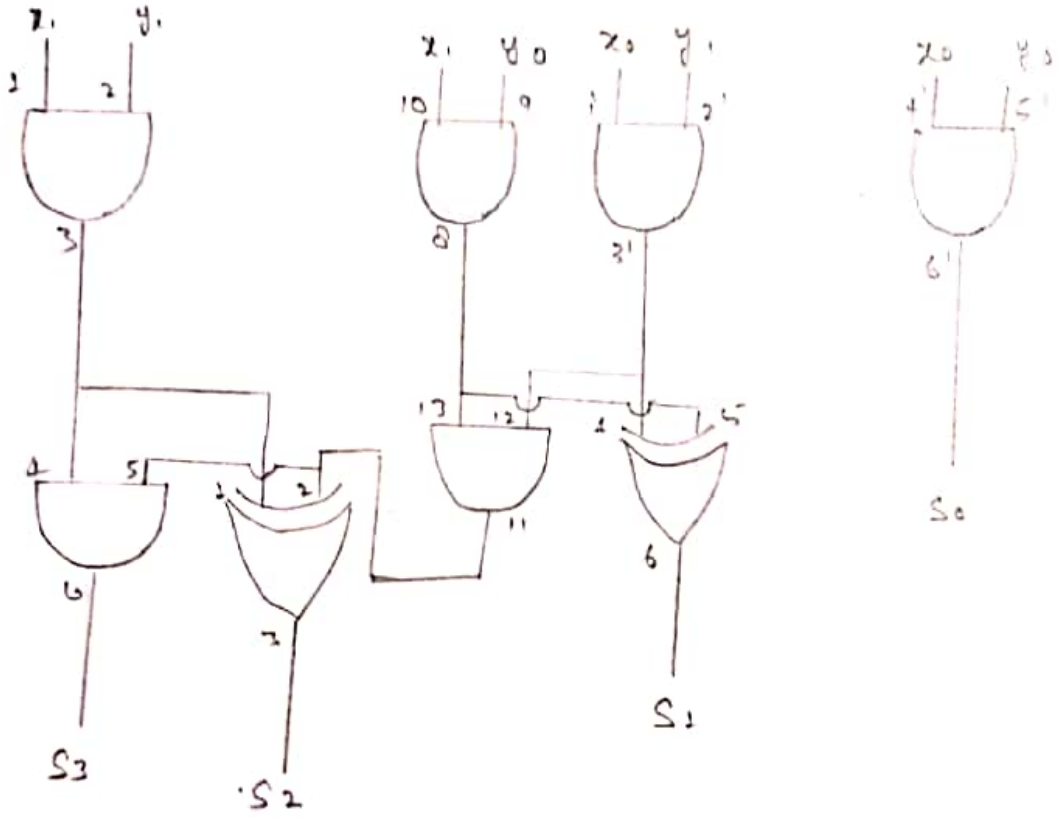
Results: Design & Study of 4-Bit register is done.

Experiment No -

Object: Design and study 2x2 bit multiplier by using gates and IC's

Apparatus required: IC-7486, IC-7408, Digital Trainer kit and connecting wires.

Circuit Diagram:



Theory: Consider the multiplication of two 2 bit number as shown in figure. The multiplicand bits are y_1 & y_0, the multiplier bits are x_1 & x_0 and the products are S_0, S_1, S_2, S_3. The first partial product is formed by multiplying x_0 by $y_1 y_0$. The multiplication of two bits such as x_0 & y_0 produces 1 if both bits are 1, otherwise it produces 0. This indicates to as AND operation. Therefore the partial product can be implemented with AND gates as shown in figure.

Observation Table:

x_1	x_0	y_1	y_0	S_3	S_2	S_1	S_0
0	0	0	0	0	0	0	0
1	1	1	1	1	0	0	1
0	1	1	0	0	0	1	0
1	0	1	0	0	1	0	0
0	0	1	1	0	0	0	0
1	1	0	0	0	0	0	0

Result: Function of 2x2 bit multiplier by using gates and IC's is verified.

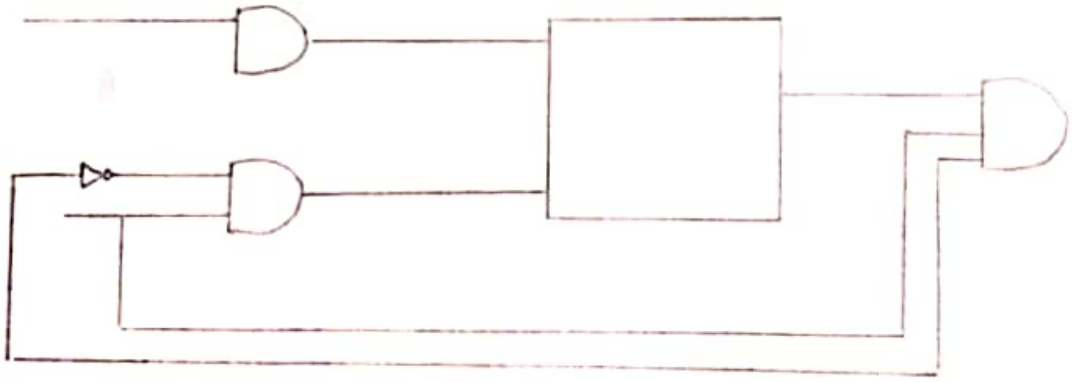
Experiment NO –

Object: To study and design of 1-bit memory cell.

Apparatus required:

Instruments	Specifications	Quantity
IC 7408	Quad 2 i/p AND gate	1
IC 7411	Triple input AND gate	1
IC 7404	Hex inverter	1
IC 7474	Dual D-flipflop	1
Digital trainer kit	–	1
connecting leads	–	6
connecting wire	–	As per required

Circuit diagram:



Theory: A 1 Bit memory cell is the basic element and all the memory IC's are built around a system of this basic 1 bit cell. The moment the clk is changed to logic 0, the output (Q) does not change and retains the D inputs level existed before the 1 to 0 transition at the clk R/W is to be at logic 1 for reading from the cell and at logic 0 for writing into the cell.

As long as $a_n = 0$, all the input and outputs activities are blocked and the cell is the hold where it stored the output is protected.

Observation Table:

Inputs

A_n	R/W	D_i	Mode
0	X	X	Hold, $D_o = 0$
1	0	0	Write 0 into memory, $D_o = 0$
1	0	1	Write 1 into memory, $D_o = 0$
1	0	X	Read, D_o = stored D_i bit.

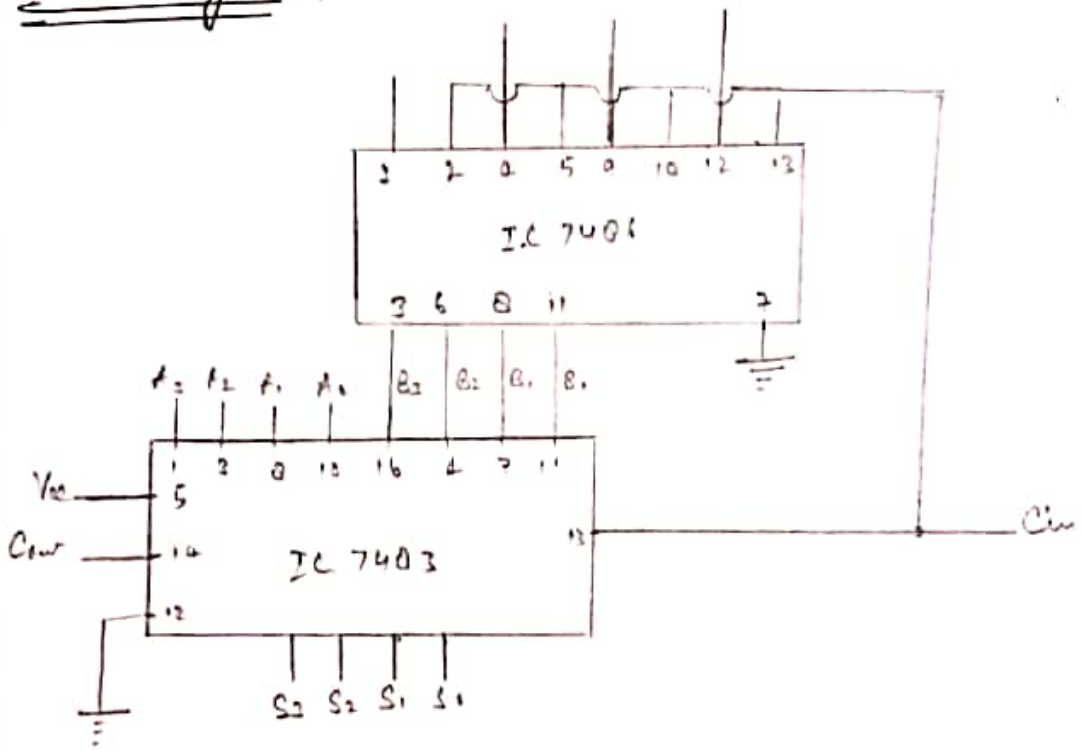
Result: Study and design of 1 bit memory cell is done.

Experiment No -

Object: Study and verify 4-bit adder / subtractor using IC 7483 and IC 7486

Apparatus required: Digital trainer kit, IC 7483, IC 7486, Breadboard and connecting wires.

Circuit Diagram:



If $C_{in} = 0$

$$\begin{array}{llll} & C_1 & C_2 & C_0 \\ & A_3 & A_2 & A_1 \; A_0 \\ + & B_3 & B_2 & B_1 \; B_0 \\ \hline & S_3 & S_2 & S_1 \; S_0 \end{array}$$

If $C_{in} = 1$

$$\begin{array}{llll} & A_3 & A_2 & A_1 \; A_0 \\ - & B_3 & B_2 & B_1 \; B_0 \\ \hline & D_3 & D_2 & D_1 \; D_0 \end{array}$$

Observation Table:

INPUTS									OUTPUTS				
C_{in}	A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	C_4	S_3	S_2	S_1	S_0
0	1	1	1	0	0	0	0	1	0	1	1	1	1
0	1	1	1	1	1	1	0	1	1	1	1	0	0
0	0	0	1	1	1	0	0	0	0	1	0	1	1
:	:	:	:	:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:	:	:	:	:
1	1	1	1	1	0	0	1	1	1	1	1	0	0
1	1	0	0	0	1	0	0	0	1	0	0	0	0

Theory: The operations of both addition and subtraction can be performed by one binary adder. Such binary circuit can be designed by adding an XOR gate with each full adder. The 4-bit adder/subtractor which has two 4 bit inputs as $A_3A_2A_1A_0$ and $B_3B_2B_1B_0$. The mode input control line is connected to carry input of the least significant bit of the full adder. This control line decides the type of operation. When $C_{in} = 1$, the circuit is subtractor and when $C_{in} = 0$, the circuit becomes adder. The XOR gate consists of two inputs to which one is connected to B and other is C_{in}. When $C_{in} = 0$, B XOR of 0 produces B. Then full adders add the B with A with $C_{in} = 0$ and hence an addition operation is performed.

Result: Design and study of 4-bit adder and subtractor is verified or done.

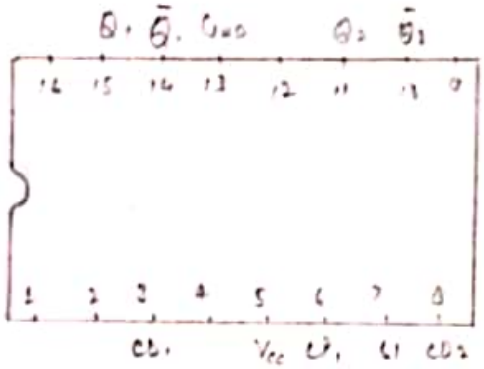
Experiment No -

Object: Design and study MOD 10 counter using flipflop and logic gates and verify truth table.

Apparatus required: IC 7476, IC 7400, IC 7408, Digital Trainer kit.

Circuit Diagram:

IC 7476 Pin configuration:-



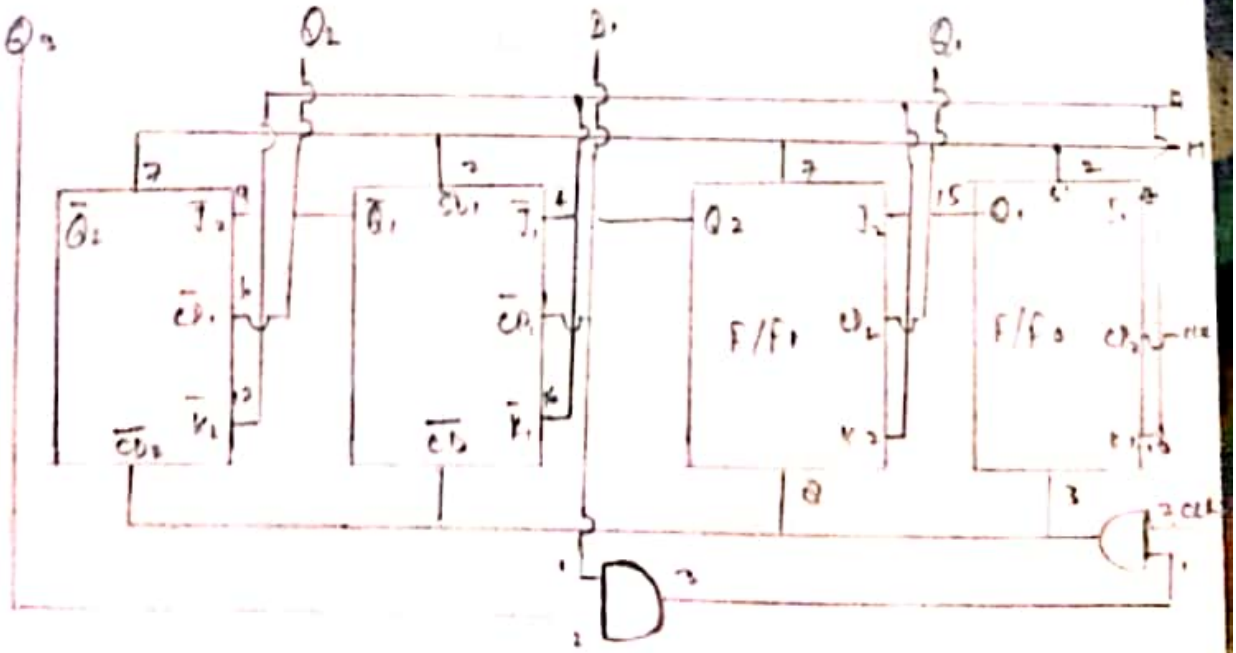
CP_1, CP_2 } Clock Pulse

CD_1, CD_2 } Direct Pulse

SP_1, SP_2 } Direct set

Q_1, $\bar{Q}_1$, Q_2, $\bar{Q}_2$ } output

Circuit Diagram of MOD 10 flipflop Counter



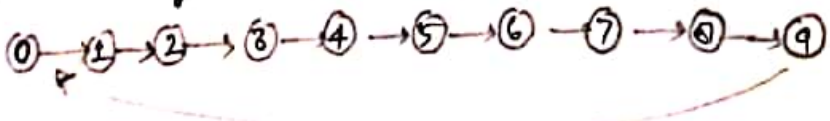
Theory: A ripple counter is an asynchronous counter where only the first flip-flop is clocked by an external clock. All subsequent flip-flop are clocked by output of the proceeding flip-flop. Asynchronous counter are also called ripples counters because of the way the clock pulse supplies it way through the flip-flop. The MOD of the ripple counter or asynchronous counter in 2^n if n flip-flops are used. For a 4 bit counter in the range of the count in 0000 to 1111 $(2^n - 1)$.

Observation Table:

Truth table

Q_3	Q_2	Q_1	Q_0	O/P
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9

State Diagram:



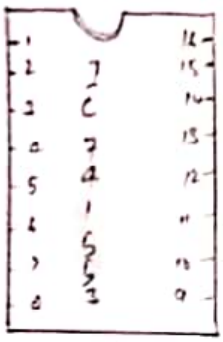
Result: Design & study of MOD-10 counter is verified.

Experiment NO - 10

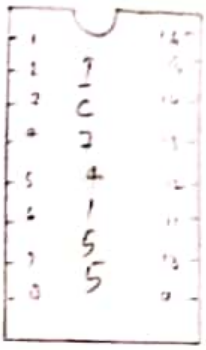
Object: Design and study of truth table of multiplexer and demultiplexer using IC 74153 and 74155

Apparatus required: Digital Trainer kit, IC-74153, IC-74155, Bread board and connecting wires.

Circuit Diagram:



MUX



DMUX

Observation table:

(MUX)

G_0	Select		y_0
	S_0	S_1	
0	0	0	A_0
0	0	1	A_1
0	1	0	A_2
0	1	1	A_3
1	X	X	0

(DMUX)

D_0	G_0	S_0	S_1	y_0	y_1	y_2	y_3
X	1	X	X	1	1	1	1
0	X	X	X	1	1	1	1
1	0	0	0	0	1	1	1
1	0	1	0	1	0	1	1
1	0	0	1	1	1	0	1
1	0	1	1	1	1	1	0

Theory:

Multiplexer: It is a device that combines several analog or digital input signals and forwards them into a single output line. A multiplexer of n inputs has select lines which are used to select which input line is used to the output.

Demultiplexer: It is a device that takes a single input line and routes it to one of several digital output. A demultiplexer of 2^n outputs has of select line, which are used to select which output line to send the input.

Result: Design and study of multiplexer & demultiplexer is done.