AMITY UNIVERSITY
UTTAR PRADESH

L	T	P/S	SW/FW	TOTAL CREDIT UNITS
3	0	2	0	4

Course Title: Digital Electronics
Course Code: ECE205
Credit Units: 4
Level: UG

Course Objectives: This course is an introduction to the basic principles of digital electronics. At the conclusion of this course, the student will be able to quantitatively identify the fundamentals of computers, including number systems, logic gates, logic and arithmetic subsystems, and integrated circuits. They will gain the practical skills necessary to work with digital circuits through problem solving and hands on laboratory experience with logic gates, encoders, flip-flops, counters, shift registers, adders, etc. The student will be able to analyze and design simple logic circuits using tools such as Boolean algebra and Karnaugh Mapping, and will be able to draw logic diagrams.

Prerequisites: An Introduction To Modern Electronics, Basic Algebra

	Weightage (%)
Module I Overview of fiber optic communication systems:	**25%**
• Analog & digital signals, DeMorgan's theorems • 1`s complement and 2`s complement, • BCD subtraction using 9's and 10's complement methods , • introduction of weighted and non weighted codes • BCD to Gray and Gray to BCD code conversion • Standard representation of logical functions (SOP and POS forms, • 5-variable K-map simplification, don't care conditions • XOR & XNOR simplifications of K-maps, Tabulation method.	
Module II Combinational Circuits	**25%**
• Serial adder ,Parallel Adder and Parallel subtractor • Difference between serial and parallel adder, • Multiplexer, de-multiplexer, • decoder & encoder, code converters, , BCD to seven segment decoder/encoder • 1 & 2 bit comparators • Implementation of logic functions using multiplexer/de-multiplexer and decoder, Implementation of 16×1 MUX using 4×1 MUX, 4×16 decoder using 3×8 decoder etc. • Logic implementations using PROM, PLA & PAL	

Module III Sequential Circuits • Difference between combinational and sequential circuits, Latch, Flip-flops: SR, JK, D & T flip flops – Truth table, • Excitation table, Conversion of flip-flops, set up and hold time, race around condition, Master Slave flip flop, • Shift registers: SIPO, PISO, PIPO, SIPO, • Bi-directional, 4-bit universal shift register; • Counters: Asynchronous/ripple & synchronous counters – up/down, • Ring counter, sequence detector.	**25%**
Module IV Logic families & data converters • Logic families: Special characteristics (Fan out, Power dissipation, propagation delay, noise margin), • working of RTL, DTL, TTL, • ECL and CMOS families • Data converters: Special characteristics • ADC – successive approximation, • linear ramp, dual slope • DAC – Binary Weighted • R-2R ladder type	**25%**

Student Learning Outcomes:

- Recognize digital electronic circuit architectures
- Apply basic techniques for analyzing digital electronic circuits.
- Identify and describe logic gates combination.
- Review of a wide range of digital applications, selecting and critically evaluating suitable implementation methodologies.

Pedagogy for Course Delivery:

The course would be covered under theory and laboratory. In addition to assigning project–based learning, early exposure to hands-on design to enhance the motivation among the students. It incorporates designing of problems, analysis of solutions submitted by the students groups and how learning objectives were achieved. Continuous evaluation of the students would be covered under quiz, viva etc.

List of Laboratory Experiment

- To design half adder, full adder, half subtractor, full subtractor using gates and verify their truth tables.
- To implement control circuit using multiplexer..
- To design a BCD to seven segment decoder converter and verify the truth table.
- To design a 4-bit BCD to Excess-3 code converter .
- To verify the truth table of R-S , D , J-K and T-flip flops.
- To design a 3-bit asynchronous UP-counter using J-K flipflops.

- To design a 3-bit synchronous Down counter using J-K flip flops
- To design a 4-bit serial in serial out shift register.
- To design and study a sequence detector

Assessment/ Examination Scheme:

Theory L/T (%)	Lab/Practical/Studio (%)	Total
75%	25%	100%

Theory Assessment (L&T):

Continuous Assessment/Internal Assessment					End Term Examination
Components (Drop down)	Mid-Term Exam	HA	Quiz/Viva	Attendance	
Weightage (%)	10%	7%	8%	5%	70%

CT: Class Test, HA: Home Assignment, S/V/Q: Seminar/Viva/Quiz, EE: End Semester Examination; A: Attendance

Lab Assessment (P):

Continuous Assessment/Internal Assessment					End Term Examination
Components (Drop down)	A	**PR**	**LR**	V	
Weightage (%)	5%	15%	10%	10%	60%

A: Attendance, PR- Performance, LR – Lab Record, V – Viva. EE- External Exam,

Text & References:

- Moris Mano : Digital Design, fourth edition Pearson Education India, 2008, ISBN -8131714500, 9788131714508.
- R. P. Jain: Modern Digital Electronics, fourth edition Tata McGraw-Hill Education, 2010 , ISBN 0070669112, 9780070669116.
- Thomas L. Floyd: Digital Fundamentals, 10th edition Pearson Education India, 2011,ISBN 813173448X, 9788131734483.
- Malvino and Leech: Digital Principles & Applications, 7th edition Tata McGraw Hill,1995 ,ISBN 0070141703, 9780070141704.