Wideband Switching Power Amplifier for Imaging SONAR

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***Abstract*— Due to wide bandwidth and ability to travel farther, acoustics signals are preferably used for underwater imaging sonar applications. A power amplifier drives the piezo transducer such that an interpretable echo can be received. This paper presents a SONAR amplifier designed and built to power a particular acoustic transducer with 50 Ω impedance at resonant frequency of 400 kHz. Because of its high power performance and compact nature, the class D topology was chosen as the power amplifier topology over any linear counterpart. Since the load is capacitive in nature, therefore, to drive the acoustic transducer with a peak power of about 500 W sourced from 96 V dc source, a boost type impedance matching network (IMN) is designed. The results show that the designed amplifier reduces power losses and waveform distortion, while improving the bandwidth.**

Keywords—sonar, impedance matching network (IMN), class D amplifier.

I. Introduction

SONAR is the acronym for sound navigation and ranging. A sonar device is widely used for detecting under water objects because of the ability of acoustic waves to travel a longer distance than optical and radio waves. Active sonar sends out a sound wave and then listens for echoes that bounce off underwater surfaces [1].

The components of a sonar transmitter are shown in Fig. 1, which include the power inverter, impedance matching network (IMN), and control circuit. Since the acoustic signal weakens as it travels, a low-distortion noise power amplifier is used to boost the power delivered to the transducer, extending the range of the sonar imaging device.

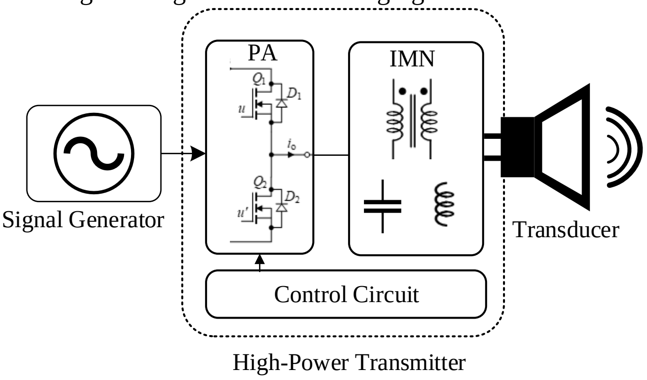

Fig. I. Block representation of sonar transmitter

The sonar transducer serves as an electrical load at the transmitter end, and the power applied determines the amplitude of the acoustic signal. Fig. 2 shows the impedance-based Butterworth-Van Dyke (BVD) model of a piezoelectric transducer, which indicates that the transducer is capacitive in design. However, the parallel mixture of capacitance C_2, inductance L_2, and resistance R_2 provides a more reliable model in comparison to capacitance C_1. As a result, the transducer needs reactive power, which is supplied by the inverter, resulting in increased switching and conduction losses. To compensate for reactive power, an IMN is typically used between the inverter and the transducer.

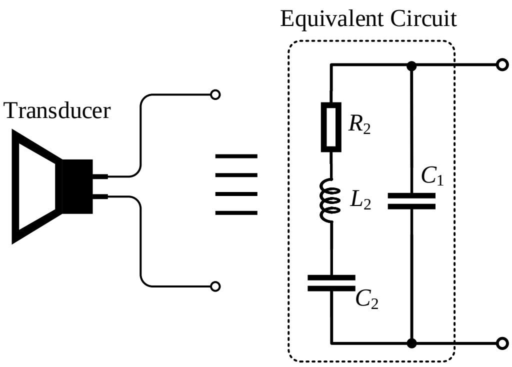

Fig. 2. The BVD model of sonar transducer

This paper is outlined as; section I presents a brief introduction. In section II the design and working of power amplifier is analyzed broadly. Design implementation is explained thoroughly in section III along with simulations. In section IV, experimental results verify the performance of the proposed design, leading to results and discussions. Finally, a fine conclusion is drawn in section V.

II. Design Concepts

The power amplifier is the essential part of the sonar transmitter. The amplifier must ensure minimum distortion in the passband to accurately produce the electric to be converted into acoustic signal without polluting the environment. In addition, it is vital for the power amplifier to exhibit large bandwidth, high efficiency, and high operating voltage [2].

In a linear amplifier, the triode area is used to achieve the boosted signal with the least amount of distortion. Class A, class B, and class AB are the most well-known members of the linear amplifier family. At elevated operating power, the efficiency of these linear amplifiers degrades much more, necessitating the use of large heat sinks. To increase the performance of linear power amplifiers, various control mechanisms such as Doherty's architecture and load-modulation were used in addition to advanced fabrication techniques including laterally diffused metal oxide semiconductor (LDMOS) [3]. The switching power amplifier, also called as the class D amplifier is known for its high efficiency [4]. Since operating active devices in the cutoff or saturation regions decreases power dissipation, increasing reliability and reducing the need for a heat sink, the heat sink demand is reduced. Alternatively, the switching or class D power amplifiers offer higher output efficiency which signifies lower power dissipation. Hence, in the proposed power amplifier, class D switching amplifiers are employed.

A. *Block Diagram*

The block diagram of the proposed PA for the transmitter is shown in the Fig. 3 below.

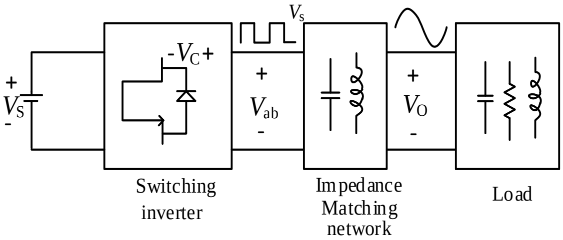

Fig. 3. Sonar system general representation

At the initial stage, an input DC signal V_s is fed to a switching inverter, through the sophisticated technique of Pulse Width Modulation that DC waveform is converted into AC waveform. Due to the capacitive nature of the load, an impedance matching network (IMN) is designed for low pas filtering. That AC signal, denoted as V_{ab}, is fed to IMN to be filtered out as a sinusoidal waveform. In this way, a low distortion amplified signal is used to deliver the power to the load.

III. DESIGN IMPLEMENTATION OF SWITCHING POWER AMPLIFIER

The switching power amplifier also known as the class D amplifier glorified by its high-efficiency encodes the reference signal into pulse-width modulation output using a switching power circuit, with pulse-width proportional to the amplitude of the reference signal [4].

A. *Switching Power Inverter*

Two main topologies were considered i.e. half bridge and full bridge. Both have their own advantages depending upon the circuit but the full-bridge mode provides twice the output voltage swing and four times the output power of the half-bridge mode. This advantage leads to better utilization of the supply voltage [3].

Fig. 4. illustrates full-bridge PA comprising four MOSFETs Q_1-Q_4. The pair of Q_1, Q_2 and Q_3, Q_4 operates in complementary fashion to produce bipolar output waveform. This type of modulation is commonly referred to as bipolar modulation.

The MOSFET which would be best for class D power amplifier are NMOS rather than PMOS as they offer better switching performance compared to PMOS transistors. Therefore, they can be employed at both high side and low-side of the output stage [3]. To turn on the high-side NMOS transistor, its gate voltage should be high enough from its source voltage, where it is referenced to the positive supply voltage.

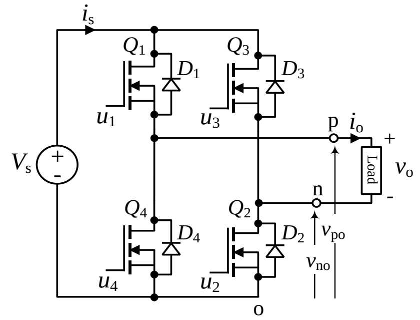

Fig. 4. Full bridge PA

With rapid upgrades in emerging technology, there are many ready-to-use gate driver integrated circuits (ICs), which make NMOS output stages possible in more compact and less complicated way [4]. In our design, gate driver IC IR2086S is used to drive the MOSFET IRF740, with the capability to deliver 1.2A output current and maximum Frequency up to 500K Hz per channel and adjustable dead time which range between 50ns to 200ns.

The components should be selected by taking power handling capabilities into considering. It needs to be ensured that the MOSFET has an adequate maximum V_{DS} (drain-to-source voltage) rating. Increase in V_{DS} will decrease the conductivity of the channel and will affect that works to decrease the drain current I_D. Apart from that reverse recovery charge (Q_{rr}) should also be kept in mind while making MOSFET selection which is the amount of charge flowing during reverse recovery time. By keeping all the above parameter in mind, we can reduce the conduction losses as well as switching losses.

An RC snubber circuit is attached with each MOSFET for protection and performance enhancement. RC snubber circuit can save a MOSFET from overvoltage spikes, which may arise during the reverse recovery process. A very common snubber circuit for a power diode consists of a capacitor and a resistor connected in parallel with the MOSFET as shown in Fig. 5. The RC snubber is the familiar and most effective technique which offers flexibility to achieve the desired level of suppression. However, the experience-based design commonly leads to inadequate damping [5].

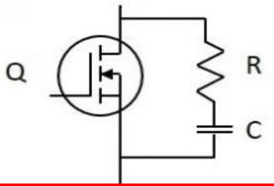

Fig. 5.

Another challenging part while constructing class D power amplifier is selection of gate driver. Its main function is to provide soft switching and avoid shoot-through current in full bridge by creating dead time. The switching transition of an electronic device is not instantaneous because of the finite rise and falls time. Therefore, a blanking time known as dead-time is inserted at every switching transition to ensure that the other switch in phase-leg is triggered to turn-on only when the turn-off of the outgoing switch has elapsed. This is essential for avoiding the shoot-through, causing high current stress and possibly failure of switching devices. Dead time control is a critical feature for a successful operation at the expense of distortion in the output signal. As the dead-time increases, the distortion will increase, and considering the direct relation, a tradeoff has to be made [6].

Switching frequency has a significant impact on the working of class D Amplifiers. With the increase in switching frequency, the harmonics will take place away from the fundamental harmonic, which will reduce the use of higher order filters.

B. *Impedence Matching Network*

As the frequencies get higher, the importance of maximum power transfer becomes immensely critical. The transducer, which acts as an electric load, is capacitive in nature while the source does not carry any reactive component. When the improper matching of impedances occurs, it leads to rising losses, and higher sensitivity. Moreover, it would cause the source energy to bounce back to the source over and over again until it is dissipated as heat or radiation.

Therefore, to compensate the reactive power and ensure maximum power transfer between the source and load, an impedance matching network is inserted between power amplifier and transducer. An IMN transforms the output impedance of the source such that it is equals to the complex conjugate of the load impedance. This matching is important to prevent the flow of unnecessary current in the system, to reduce losses.

1. Design of parallel RLC Network

The IMN is designed in such a way that the THD and total voltage gain can meet the required specifications. The basic function of IMN is low-pass filtering. Additionally, it is used for voltage gain. The IMN suppresses the unwanted harmonics for producing nearly sinusoidal output V_o. In the IMN, switching frequency determines the fundamental frequency of ac output. Moreover, the voltage gain is commonly controlled using switching frequency modulation. For improving selectivity of the network high Q factor is required. Meeting our design criteria, parallel RLC Network provides a higher output voltage and a higher Q factor, essential for lower THD.

Fig. 6 illustrates the parallel RLC network, connected with the power inverter. The circuit is simplified by replacing the inverter with a square wave source. The capacitor is in parallel with the load, that's where the word parallel comes from.

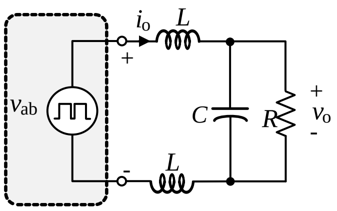

Fig. 6. Parallel resonance network

The design involves computation of L and C values using Q for the given load resistance R i.e. 50 and THD. For Q = 2.99, value of L = 6.65 μH and C = 23.9 nF. The output sinusoidal voltage swings between ±360v, with amplification factor of 2.66 and a THD of 1.39%. When Square waveform $V_{ab.}$ i.e. ±96v is applied to the resonant network due to narrow band only fundamental component appear at the load.

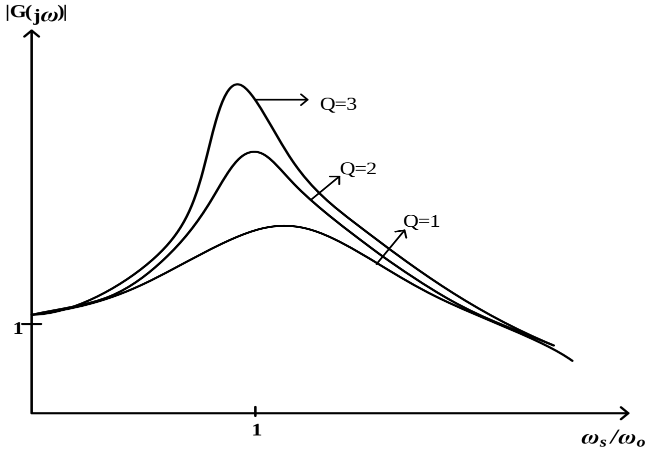

Fig. 7. Gain characteristic for parallel network

Gain can be obtained from the equation,

$$G(jw) = \frac{1}{1-\left(\frac{w}{w_o}\right)^2 + j\frac{w}{w_o}\left(\frac{w_o L}{R}\right)} = \frac{1}{1-\left(\frac{w}{w_o}\right)^2 + j\frac{w}{w_o}Q_p} \quad (1)$$

Equation (1) shows that using frequency modulation we can step-up or step-down output voltage. Output voltage can be controlled by varying the switching frequency f_s.

C. *Simulations*

All circuit simulation works are performed in LT-SPICE and the results are demonstrated using MATLAB

Since the operation mode of full-bridge inverting depend upon the switching configuration. Table. I show the different operations mode of MOSFET

TABLE I. OPERATION MODES OF MOSFET

Mode	ON Position	Measured Voltage v_{ab}
1.	Q1, Q3	0
2.	Q1, Q2	+96V
3.	Q2, Q4	0
4.	Q3, Q4	-96V

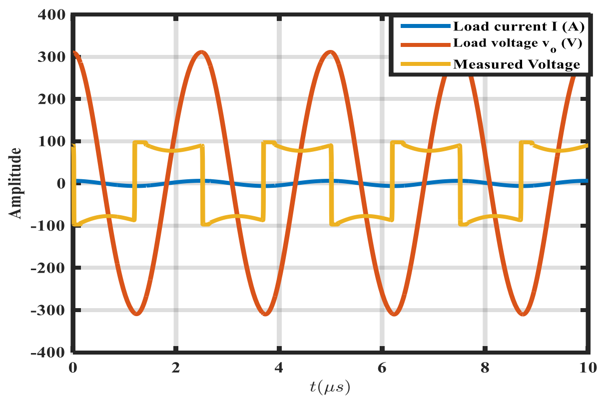

Fig. 8. Output waveform of parallel RLC network at 400 kHz

Since the square waveform V_{ab} is applied to the resonant network and due to narrow band only fundamental component appear at the load. The voltage across the capacitor that's also appear at the load is sinusoidal if the operation is near the resonant frequency as shown in Fig 7.

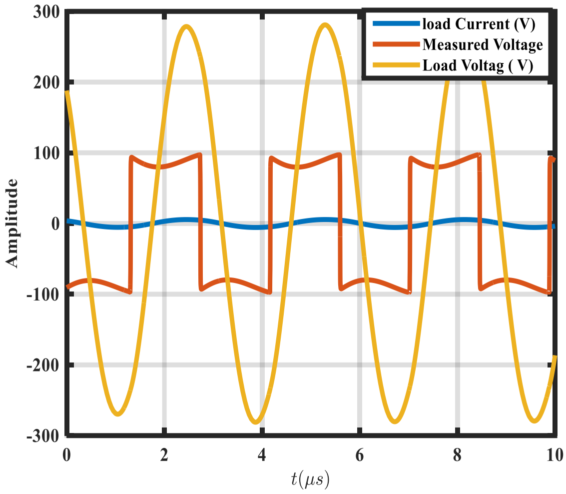

Fig. 9. Output waveform of parallel RLC network at 450kHz

In the Fig. 8, Output voltage can be controlled by varying the switching frequency $f_{s.}$ When $\omega_s < \omega_o$ the load is capacitive as current i_o leads V_{ab} i.e. ±96V. in this case the circuit act as capacitive and hence the maximum powered is not being transferred.

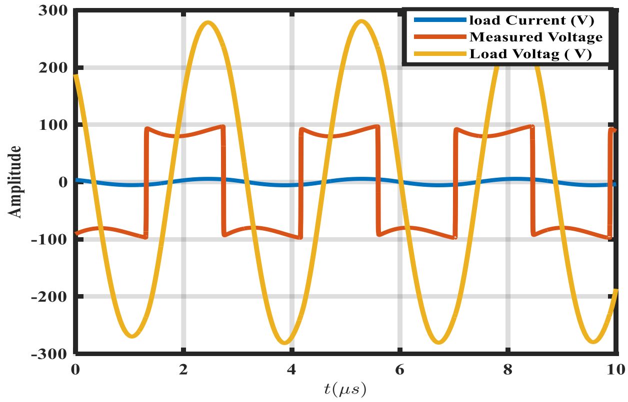

Fig. 10. Output waveform of parallel RLC network at 350 kHz

In the Fig. 10, when $\omega_s > \omega_o$ the load is inductive as current i_o lags voltage $V_{ab.}$ i.e. ±96V. In inductive mode i_o first flow through diode due to negative direction of current and communicate to transient before turn-off. The turn-on in inductive mode is lossless as diode conducts before transients. Since the load is inductive the maximum power is not being transferred

IV. Experimental Results

This work is the design of power amplifier for driving the transducer, focusing on the enhancing the bandwidth for improving resolution of sonar detection. Table II lists the design parameters for switching power amplifier. Low THD is required to minimize the radiation of unwanted signals in the environment having deleterious effect on system operation. Besides, the amplifier must enable high power transfer to the transducer while maintaining a high efficiency.

TABLE II. Design Parameters of Switching Amplifier for Sonar System

Parameters	Value
1. Gain	10 dB to 40 dB
2. Central frequency	400 kHz
3. Bandwidth	400 kHz ± 50 kHz
4. Output power	1.6 kW
5. Output impedance	50 Ω
6. Output harmonics	<-40 dB
7. Supply voltage	DC=+96 V
8. Input sensitivity	300 mVrms to 2 Vrms
9. Input impedance	≥ 10 kΩ

The PCB for the power switching amplifier was designed in Altium-Designer which after fabrication results in the 11cm x 5 cm board shown in Fig. 11.

Fig. 11. PCB for power amplifier after stuffing.

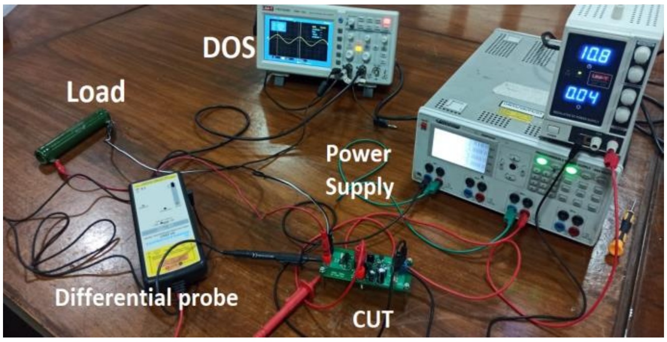

Fig. 12. Experimental setup for testing the prototype of switching power amplifier

Fig. 12 shows the experimental setup for testing power switching amplifier. Two power supplies are required to run the circuit: first to power the gate driver, and second to apply voltage to the bridge inverter. For the farmer 10.8 V while for latter 60 V supply is required. Both power supply features current limit, that is essential for protection of circuit during early test. For early tests, the supply voltage to the bridge was kept low (less than 10 V) to make sure that the overall circuit behaves well according the design. Then, tests were performed as elevated supply voltage. For recoding waveform of output voltage, a differential voltage probe was used with 100x scaling.

The frequency of gate pulses from IR2086STRPBF IC can be adjusted with the help capacitor CT and resistor RT. For instance, to set a desired frequency of 400 kHz, RT=12.1 kΩ and CT=220pF can be employed. The output of the full bridge is connected to Impedance Matching Network (IMN) i.e. parallel RLC circuit. The experimentally measured values of inductors and capacitors are 2.7 μH and 33.2 nF, respectively. Therefore, in experimental setup the Q_s=0.19 and Q_p=5.21, which means the gain will be higher relative to simulation results. External 47 Ω resistor is used as load in place of the transducer.

Results have been recorded for different switching frequencies and presented in Fig. 13 to Fig. 15. Fig. 12 shows the output of switching amplifier at f_s=431 kHz, where amplifier is delivering a power of 511.1 W to the resistive load. The waveform also suggests that converter is operating in inductive mode, and therefore no significant spurious spikes in the drain-source voltage waveform were observed.

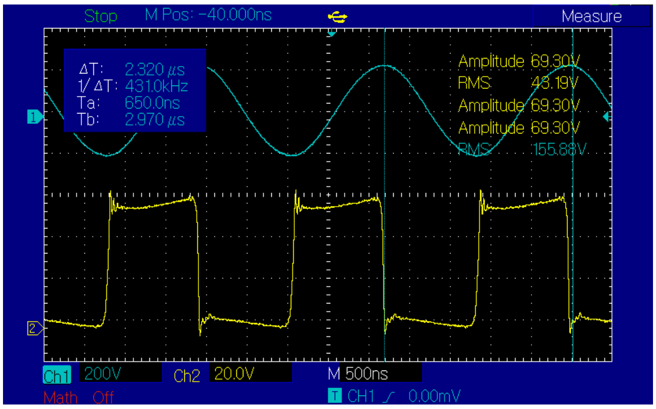

Fig. 13. Output voltage (Blue) and drain-source voltage of MOSFET Q3 at f_s=431 kHz (Yellow)

When the switching frequency is raised, the converter still enjoys the inductive mode. However, the gain declines when switching frequency deviates from the resonant frequency as shown in Fig. 14

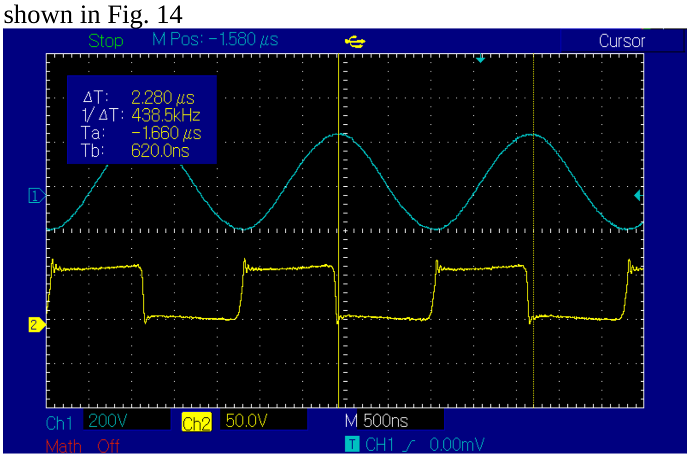

Fig. 14. Output voltage (Blue) and drain-source voltage of MOSFET Q3 at f_s=438 kHz (Yellow)

Fig 15 shows the operation in capacitive mode, when f_s=400 kHz. The capacitive nature is evident from the dent in the drain-source voltage waveform. The delivered power is 472.1 W which further declines by when switching frequency reduces.

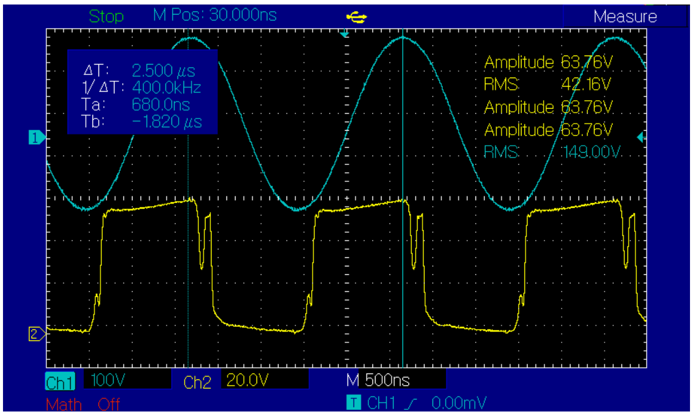

Fig. 15. Output voltage (Blue) and drain-source voltage of MOSFET Q3 at f_s=400 kHz (Yellow)

Fig. 16. shows the efficiency of power amplifier for different load currents. The graph shows that at lighter load, the MOSFETs and passive components consume less power resulting in higher efficiency. However, at heavy load the efficiency deteriorates due to power loss by above mentioned components.

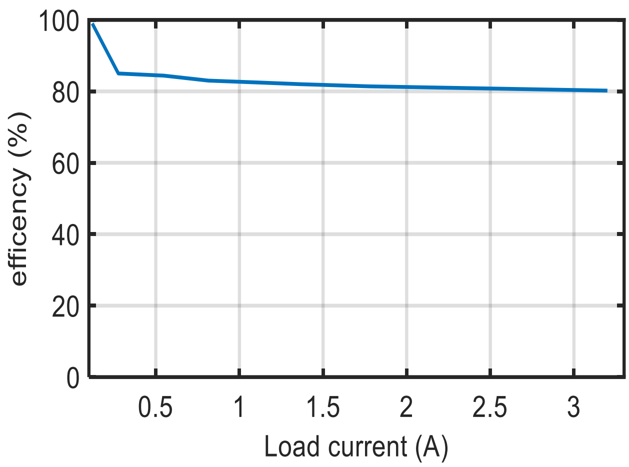

Fig. 16. Efficiency of switching power amplifier at f_s=438 kHz

V. CONCLUSION

The purpose of this project is to design a high-power SONAR power amplifier developed to drive a specific acoustic transducer. Power amplifier is a critical part of an active SONAR system. It generates required electrical power and it delivers this power to an acoustic transducer, which converts electrical energy into acoustic energy. A 400 kHz Full Bridge switched Class D power amplifier embedded in a sonar equipment has been designed, fabricated, and measured.

To ensure maximum power transfer, it is necessary to introduce impedance matching network. So that maximum power can be transferred through the transducer. The circuit is designed to satisfy several requirements and its functionality is validated by several tests. As the measurement results reveal that the design is able to provide a peak-power of 1.6kW and generate a sinusoidal waveform at 400 kHz frequency with 3.2% total harmonic distortion

VI. REFERENCE

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