# Development of a technology for the fabrication of Low-Gain Avalanche Detectors at BNL

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**Abstract**

Low-Gain Avalanche Detectors are gathering interest in the High-Energy Physics community thanks to their fast-timing and radiation-hardness properties, which are planned to be exploited, for example, in timing detectors for the upgrades of the ATLAS and CMS detectors at the High Luminosity LHC. This new technology has also raised interest for its possible application for photon detection in medical physics, imaging and photon science. The main characteristic of this type of device is a thin and highly-doped layer that provides internal and moderate gain, in the order of 10-20, that enhances the signal amplitude. Furthermore, the thin substrate of a few tens of microns allows fast carrier collection. This paper details on the fabrication technology, specifically developed at Brookhaven National Laboratory for the detection of minimum ionizing particles. The static electrical characterization and the gain measurements on prototypes will be reported, too.

*Keywords:* silicon sensors, avalanche multiplication, electrical characterization, high voltage, high-energy physics

## 1. Introduction

Studies of fast-timing detectors have attracted widespread interest in the scientific community around the world in relation to the development of next generation of collider experiments and imaging techniques in a variety of applications [1]. Silicon-based particle sensors that combine fast-timing and radiation-hardness properties are a rapidly developing research area, thanks to their applications in timing and tracking systems of the upgraded ATLAS [2] and CMS [3] experiments at the CERN Large Hadron Collider (LHC) for the High Luminosity phase (HL-LHC), expected to begin in 2026 [4, 5]. One of the selected technologies for such detectors that can deliver the sought timing performance of few tens of ps is a silicon pad with internal amplification, fabricated on a thin substrate: the so called Low-Gain Avalanche Detector (LGAD) [6]. Since the time-resolution $\sigma_t$ is given by (e.g. [7], page 35):

$$\sigma_t = \frac{\sigma_n}{\frac{dS}{dt}}$$

where $\sigma_n$ is the r.m.s. voltage noise of the system and $S$ the signal amplitude, large and short signals are needed. For the signal to be short, a thin substrate is needed, in

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the order of few tens of micrometers (30-50 $\mu$m). However, a thin substrate causes a loss in signal, due to the lesser amount of material crossed by the interacting particle and, thus, of signal carriers. This loss of signal carriers can be more than compensated by an internal gain, which enhances the signal amplitude S by a factor of 10-20. Keeping the gain value at a moderate level, i.e. considerably below the avalanche regime, is instrumental to keep the noise low [8].

The structure of a typical LGAD is shown in Figure 1. The active thickness of the device is an epitaxial layer or a thin silicon wafer wafer-bonded to a thick substrate, that acts as a mechanical support. The thickness of the epitaxial layer can be a few tens of $\mu$m, in order to have a short drift of the carriers. An $n^+-$layer creates the junction with the $p-$type substrate, as in a regular diode. Additionally, a $p-$layer is implanted just below the $n^+$ implant (*gain layer*). Application of a bias to the junction leads to depletion of this layer, which results in a high electric field in a superficial region that extends in depth for about a micron. This electric field will create impact ionization to the electrons crossing it, while keeping the ionization rate of the holes at a negligible level (excluding thus the onset of a breakdown). The result is an amplified current pulse, dominated by the motion of the holes through the whole thickness of the substrate. These amplified current pulses are inherently fast and can offset the limited amount of charge released by a minimum ionizing particle (MIP) in the thin substrate (as compared to a standard 300 $\mu$m thick silicon).

For a stable and reproducible amplification, the electric field lines inside the device, when depleted, must be straight and parallel to each other as much as possible. To achieve this goal, edge effects are minimized by designing pads with sizes of about 1 mm, thus far larger than the silicon thickness. At the edge of the $n^+$ implant, an additional deep $n^+-$implant is inserted to protect from an early breakdown [9]. This is usually called *Junction Termination Edge (JTE)*. To keep dead area small at the edge of the devices, the JTE must be as narrow as possible.

The LGAD, especially after irradiation, operates at relatively high bias voltage, therefore a Guard Ring (GR) termination is added at the periphery of the active device to gradually bring the high voltage at the cutline to the ground applied to the innermost GR surrounding the pad, and thus preventing breakdowns.

In particular, high electric fields may develop at the edges of the junctions: for a given geometry, deep implants are expected to develop lower electric fields than shallow implants (see Ref. [10], page 53). Thus, the GR termination, which can be very similar to the standard silicon sensors and meant to work at similar voltages, can profit from the JTE deep implant.

Several groups around the world are working on the development of the LGAD (see Ref. [11, 12, 8]). This paper details the specific fabrication technology developed at Brookhaven National Laboratory (BNL) that targets the detection of MIP's. This paper is structured as follows. In Section 2 a detailed description of the fabrication process is given; in Section 3 the electrical characterization of small pads is presented, while the results of the measurements to characterize the gain performance are the subject of Section 4.

## 2. Fabrication Process

In the following we describe the process developed for the fabrication of the first LGAD prototypes at BNL. The process consists of 7 lithographies and 4 ion-

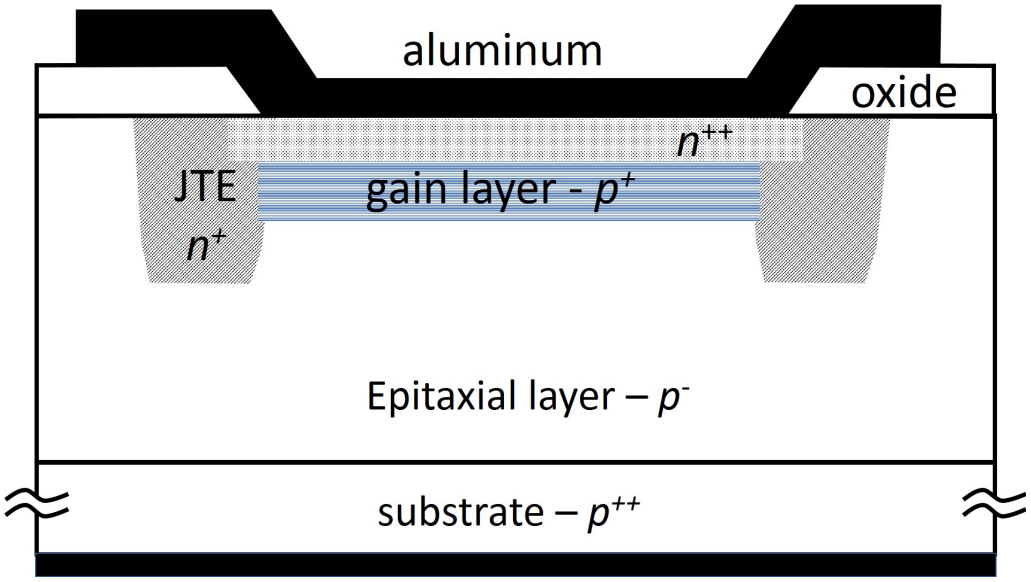


Figure 1: Sketch of the structure of an LGAD (not to scale). Only the active area is shown.

implantations (two of them at high energy). It was carried out with wet etches in the class-100 clean room of the Instrumentation Division at BNL.

The starting material is a (100)-oriented, 4" epitaxial silicon substrate. The epitaxial layer is $p-$type, 50 $\mu$m thick with a doping concentration of about $5 \cdot 10^{13}$ cm$^{-3}$. The substrate on which the epitaxial layer is grown is a heavily doped, 500 $\mu$m thick Czochralski substrate that acts as a ohmic contact and mechanical support. The wafers, after the initial oxidation, undergo a series of steps, as outlined below:

- The first lithographic step is the definition of the JTE (Figure 2a and Figure 3a). The silicon oxide is removed in the areas freed from photoresist, and a high-energy phosphorus implantation follows. The ion implantation is performed at zero degrees of tilt and 45 degrees of twist, to exploit the channelling of ions in the (100) substrate. This makes the implant to penetrate deeper into the silicon crystal, without requiring the use of higher implantation energies. On the contrary, all other implantations are performed at 7 degrees of tilt and 23 of twist, to minimize channeling. A SILVACO TCAD [13] simulation is performed to predict the doping profile of the JTE and it is reported in Figure 4.

- After an additional lithography, the silicon oxide in the active area of the LGAD is removed by wet etching. A re-oxidation follows: a thin screen oxide of about 35 nm is grown, followed by a drive-in in nitrogen (Figure 2b).

- The electron accumulation layer at the silicon to silicon-oxide interface induced by the positive charge into the oxide would short the electrodes together, unless a $p-$type (boron) implant (a patterned "$p-$stop" or an unpatterned "$p-$spray") is not placed in the gaps between them. In this fabrication of LGADs, to insulate the GR structures from each other and from the LGAD pad, a $p-$spray implant is chosen. Differing from a standard $p-$spray, which is uniformly implanted at the beginning of the process, in this production it is patterned so that this boron implant does not interfere with the gain layer

in the active area, which is made of boron, too (Figure 2c and Figure 3b). The parameters are the standard for all $n$-on-$p$ processes at BNL: a dose of $2 \cdot 10^{12}$ cm$^{-2}$ at 100 keV. The $p-$spray is implanted through the thin screen oxide in the GR regions, too. However, being the dose much lower than the GR's and being its energy low enough to keep it within the GR, the $p-$spray is fully compensated by the GR implant.

- In the active LGAD area, the gain layer is implanted. For these prototypes, the energy is chosen so that the implant is not deeper than the JTE (Figure 2d and Figure 3c). This is visible in Figure 4, where the JTE and the doping concentration of the gain layer are compared. Doses from $2 \cdot 10^{12}$ cm$^{-2}$ to $3.5 \cdot 10^{12}$ cm$^{-2}$ have been used to study different gain values. An annealing in nitrogen follows.

- After $n$-plus lithography and photoresist exposure, before the $n$-plus implant, a short wet etching thins down the screen oxide. Subsequently, a high-dose phosphorus implant is performed to make a good ohmic contact (Figure 2e and Figure 3d). A final annealing in nitrogen for the activation of the phosphorus implant is the last thermal cycle of the fabrication.

- A uniform PECVD oxide is grown, then contacts are opened, an aluminum (1% silicon) layer is sputtered on both sides of the wafers and patterned on the front side (Figure 2f). Sintering in forming gas ends the process and no passivation is used for this production.

## 3. Electrical Characterization

A picture of a fabricated wafer is shown in Figure 5. It is populated with single pads of LGADs, of 1x1 mm$^2$, 2x2 mm$^2$, and 3x3 mm$^2$, with same termination structures. Arrays of these pads are also present. Diodes which share the same dimensions and differ from the LGADs only by the absence of the gain layer are also included for reference. Standard test structures for the assessment of the quality of the fabrication batch (and the reproducibility from batch to batch) are inserted. From these, a bulk leakage current of about 1 nA/cm$^2$ is measured as well as good electrical properties, such as contact resistances, sheet resistances etc.

A critical parameter is the gain, which is controlled in this fabrication by the boron dose of the gain layer, since the implantation energy is kept fixed. For optimizing the gain, different wafers were processed at different boron dose values, starting from $2.5 \cdot 10^{12}$ cm$^{-2}$ up to $3.5 \cdot 10^{12}$ cm$^{-2}$, in steps of $0.25 \cdot 10^{12}$ cm$^{-2}$. The doping profile of the activated gain layer (as well as the doping of the epitaxial layer) can be extracted by a capacitance-voltage (C-V) measurement performed on a single pad. Throughout the measurements the GR is kept at ground voltage. Since the pad dimensions are far larger than the substrate thickness, we can obtain an accurate 1-D profile, i.e. not distorted by edge effects. The C-V scans acquired for 1x1 mm$^2$ pads belonging to different wafers are reported in Figure 6. The high capacitance at the lowest bias voltages is due to the incomplete depletion of the gain layer. As soon as the gain layer is depleted and the depletion region starts extending into the much less doped epitaxial layer, the capacitance abruptly drops, creating a *foot* in

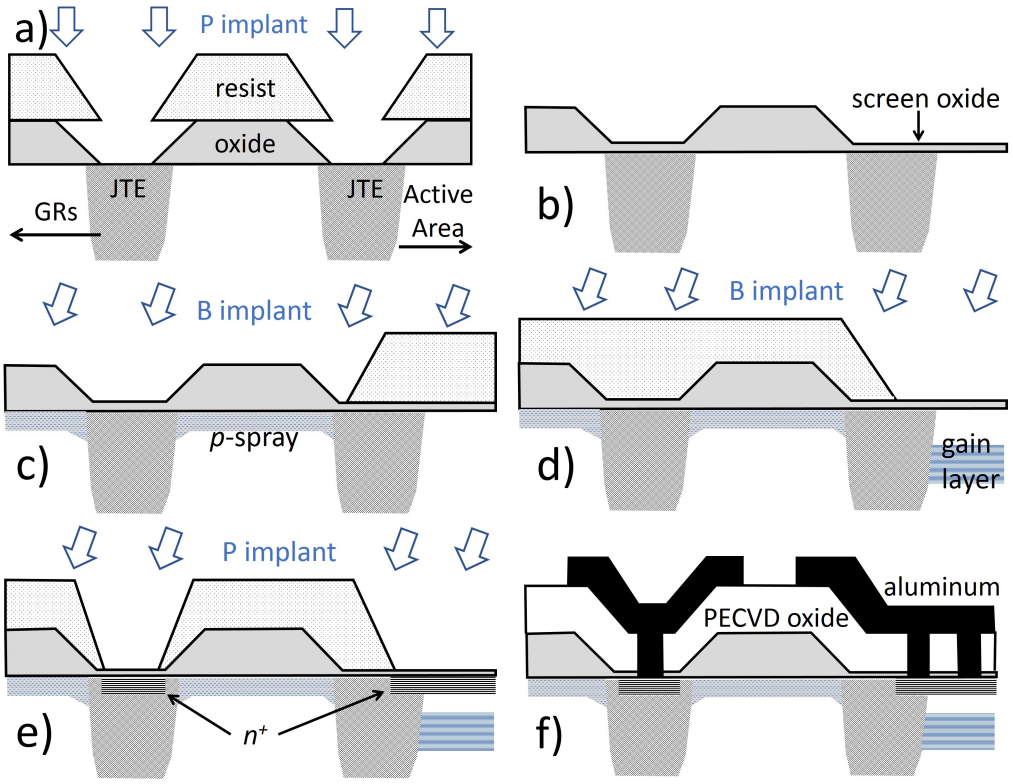


Figure 2: Main steps of the LGAD fabrication process used at BNL (not to scale). a) JTE definition and phosphorus (P) implantation, b) thin-layer re-oxidation, c) *p*-spray boron (B) implantation, d) gain layer boron implantation, e) *n*-plus phosphorus implantation and f) final device, after PECVD oxide growth, contact opening and aluminum sputtering and definition. The arrows indicate the implantation beam and its general direction.

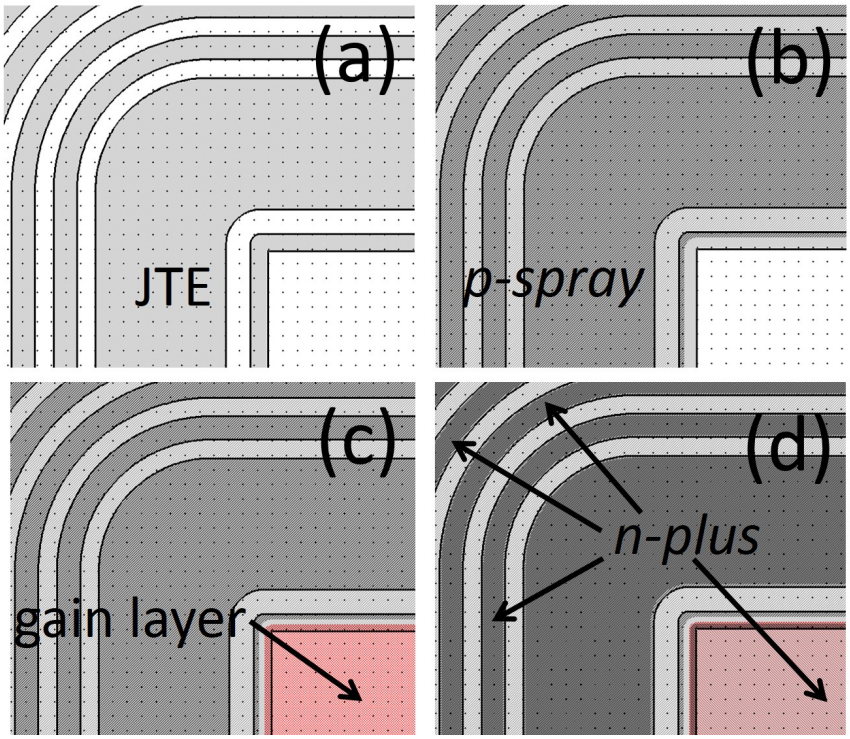


Figure 3: Layouts of corners of LGAD pads, showing various implantation regions: a) shows the JTE structure, b) the p-spray, c) the gain layer and finally d) the $n$-plus implantation. Grid points are 10 $\mu$m apart.

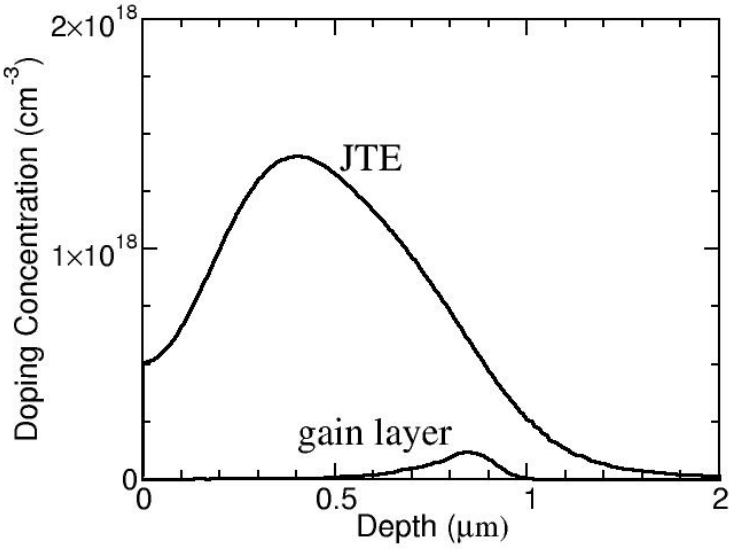


Figure 4: Simulated doping concentration as a function depth for the JTE structure and the gain layer for an implantation dose of $3 \cdot 10^{12}$ cm$^{-3}$.

| Nom. Dose ($10^{12}$ cm$^{-2}$) | Dose from C-V ($10^{12}$ cm$^{-2}$) | Activation Frac. | $V_{BD}$ (V) |
|---|---|---|---|
| 2.50 | 2.3 | 0.92 | 450 |
| 2.75 | 2.5 | 0.91 | 380 |
| 3.00 | 2.7 | 0.90 | 300 |
| 3.25 | 2.9 | 0.89 | 200 |
| 3.50 | 3.2 | 0.91 | 50 |

Table 1: For each value of the nominal implantation dose, the values of the dose extracted from C-V scan, the activation fraction and the breakdown voltage ($V_{BD}$) are reported.

the C-V curve. For increasing values of the gain layer dose, the foot shifts to higher voltage values.

By applying the following formula (see Ref. [14], page 171)

$$N_c(x) = -\frac{C(V)^3}{\epsilon_{si} \cdot q \cdot A^2 \cdot \frac{dC(V)}{dV}} \quad ,$$

with $x = \frac{A \cdot \epsilon_{si}}{C(V)}$ being the depleted thickness at the voltage $V$, $A$ the area of the junction, $\epsilon_{si}$ the dielectric constant of silicon, and $q$ the elementary electrical charge, one can extract the doping concentration $N_c$ of the gain layer as a function of the depth $x$, starting from the metallurgical junction between the $n^+$ and the gain layer itself. If we assume that the distribution of doping concentration is symmetric with respect to its peak in $x$, it is apparent from Fig. 6 that part of the gain layer is compensated by the $n^+$ layer, and thus a fraction of the boron dose is not effective in creating the electric field that produces multiplication. Furthermore, being the gain layer relatively shallow, only the deepest part of the doping profile can be extracted from the results of C-V scan. Numerically integrating in $x$ the distribution of doping concentration from the position of the peak to the substrate, and doubling the result, we can infer the amount of dose that is electrically active. Table 1 reports the values of the dose extracted from the C-V scan, the inferred fraction active dose and the measured breakdown voltage for each value of the nominal implantation dose. The table shows that activation fractions in excess of 0.9 are obtained. However, these values must be considered as a lower limits, because implantations are known to be retrograde: higher doping concentrations are expected at depth values lower than the peak of the doping profile. This can be appreciated in the example of the simulated profiles reported in Figure 4.

Samples of the current-voltage characteristics (I-V), as measured on 1x1 mm$^2$ LGADs belonging to wafers implanted with different gain layer doses, are shown in Figure 7. The gain layer implantation dose strongly affect the breakdown voltage (reported in Table 1), and the amount of the pad current, which is merely the leakage current augmented by the gain. However, other methods are employed to measure the gain: a Charge Sensitive Pre-Amplifier (CSA) was used, as detailed in the following section.

## 4. Gain Measurements

A few 3x3 mm$^2$ LGAD pads were cut out from various wafers and assembled to test-boards by gluing and wire-bonding, to make electrical connection to the input of the CSA. For calibration purposes, diodes fabricated in the same wafers

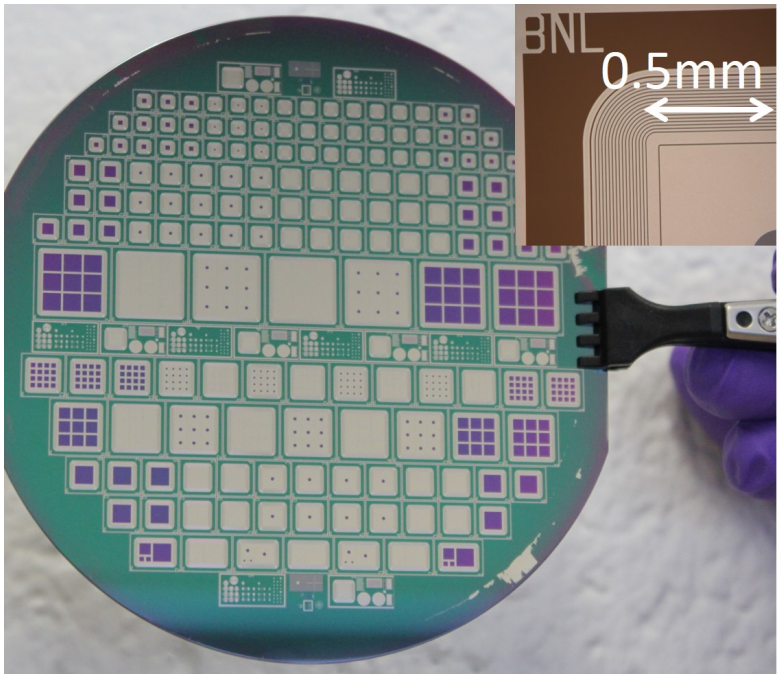


Figure 5: Photograph of a 4" wafer populated with single LGAD pads and arrays of LGAD pads. The inset on the top-right corner shows a close-up of an LGAD structure.

were mounted on the same test-boards. Diodes differ from the LGADs only for the absence of the gain layer, while they share all other properties such as dimensions and, thus, capacitance (18 pF at full depletion regime). The CSA is a single-channel model, developed at BNL, whose input capacitance is in the order of 20 pF. The output signal is fed to an AMPTEK PX5 [15], for spectra acquisition. Finally, either a gamma ray $^{241}$Am or an X-ray $^{55}$Fe source shines over the devices.

The former has the most energetic line at 60 keV generating about $16.6 \cdot 10^3$ electron/hole pairs ($e^-/h^+$) in silicon, while the latter has a line at 6 keV which thus creates one tenth of the charge and about half of average number of $e^-/h^+$ generated by a MIP in 50 $\mu$m of silicon ( $4 \cdot 10^3$ $e^-/h^+$).

Examples of spectra acquired with this set-up are shown in Figure 8. As compared to the spectrum acquired with the diode, for low implantation doses in the gain layer (thus low gain), the signal-to-noise ratio increases and the low-energy peaks from the $^{241}$Am gamma ray spectrum are visible. On the contrary, by increasing the implantation dose (thus high gain), the 60 keV peak of the spectrum clearly moves to higher channel numbers and it becomes far broader, while the low-energy peaks become indistinguishable.

In this set-up, the $^{55}$Fe peak is invisible if acquired either with the diode or at the low gains, and can only be seen at the high gains. Figure 8 shows the $^{55}$Fe spectrum for a dose of $3 \cdot 10^{12}$ cm$^2$ (i.e. high gain), for different bias voltages.

The 60 keV and the 6 keV peak positions are acquired for different values of the bias voltage and are compared to the peak position using the diode as detector. The ratio between the peak positions for the cases of the LGAD and the diode is a measure of the LGAD gain. A summary of the LGAD gain values acquired for different bias voltages is shown in Figure 9.

Figure 9 shows that the gain is higher when measured by using the $^{55}$Fe source, likely due to a charge self-shielding effect that comes into play for high values of

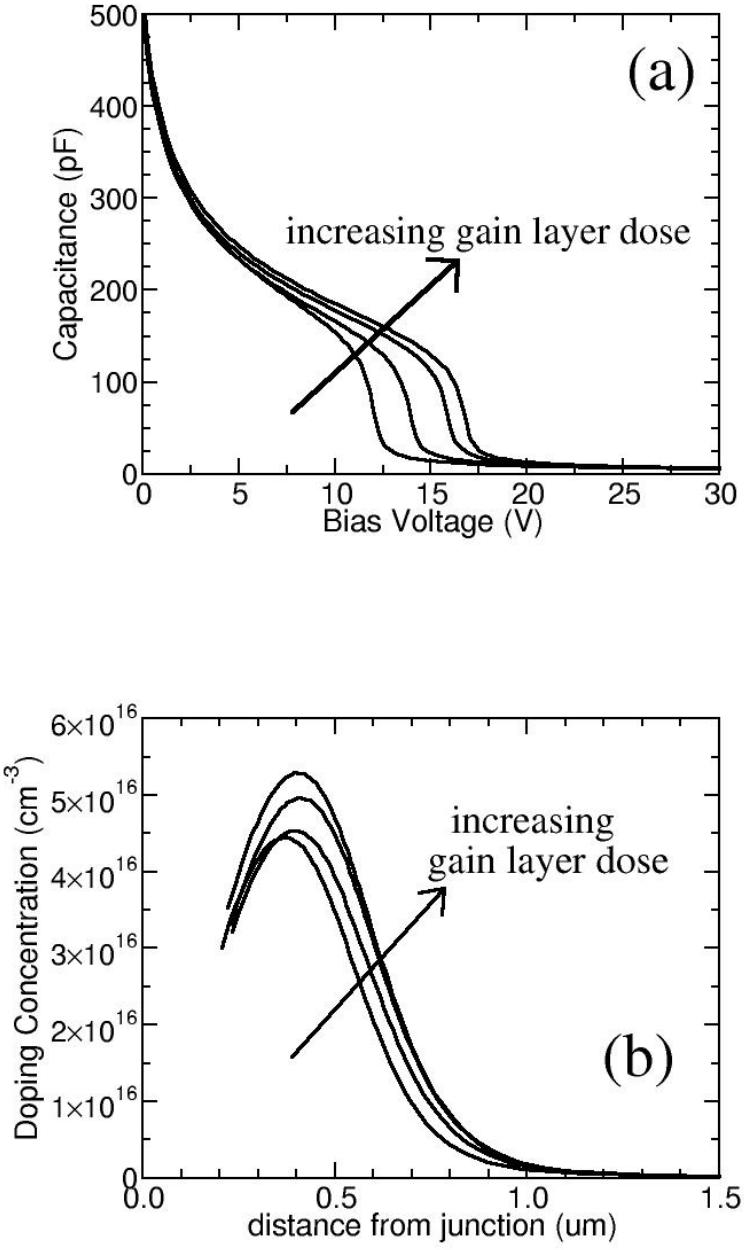


Figure 6: Top: Capacitance as a function of bias voltage for 1x1 $mm^2$ LGAD pads. The various curves are for LGAD pads fabricated with different doping doses of the gain layer, spanning from $2.5 \cdot 10^{12}$ $cm^{-2}$ up to $3.25 \cdot 10^{12}$ $cm^{-2}$, in steps of $0.25 \cdot 10^{12}$ $cm^{-2}$ ($f = 10$ kHz). Bottom: Doping concentration of the gain layer as a function of the distance from the junction, as extracted from the C-V scans on the top. The diagonal arrows point towards the direction of increasing gain layer doses.

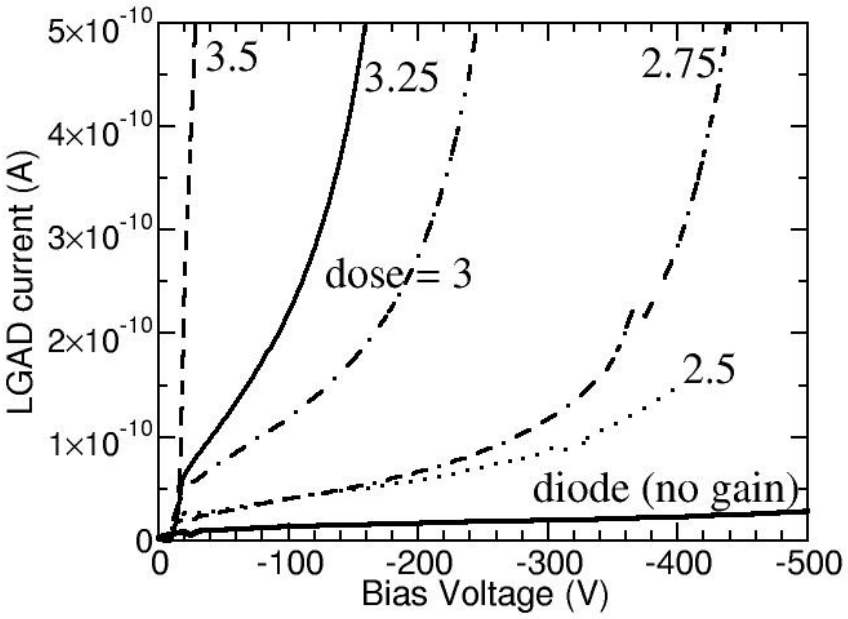


Figure 7: Examples of I-V characteristics for 1x1 $mm^2$ LGAD pads fabricated in wafers implanted with different gain layer doses (in units of $10^{12}$ $cm^2$). For reference the current of a 1x1 $mm^2$ diode, i.e. with no gain, is shown. In these measurements the GR is grounded.

generated charge.

While this production spans a wide range of gains, a maximum gain of 20 is observed.

## 5. Conclusions

Fast-timing detectors have attracted world-wide interest for applications in high-energy collider physics as well as in photon science and imaging. Specifically, silicon-based detectors with internal gain have made significant progress in recent years. The technology for the fabrication of Low Gain Avalanche Detectors has been developed at BNL for the detection of minimum ionizing particles. This paper details the steps of the specific fabrication process developed at BNL. The prototypes show low leakage currents, good electrical characteristics and, most importantly, gain values in a range of 2 to 15, optimal for timing detectors at particle colliders. Further optimization of the fabrication process could increase the gain to even higher values.

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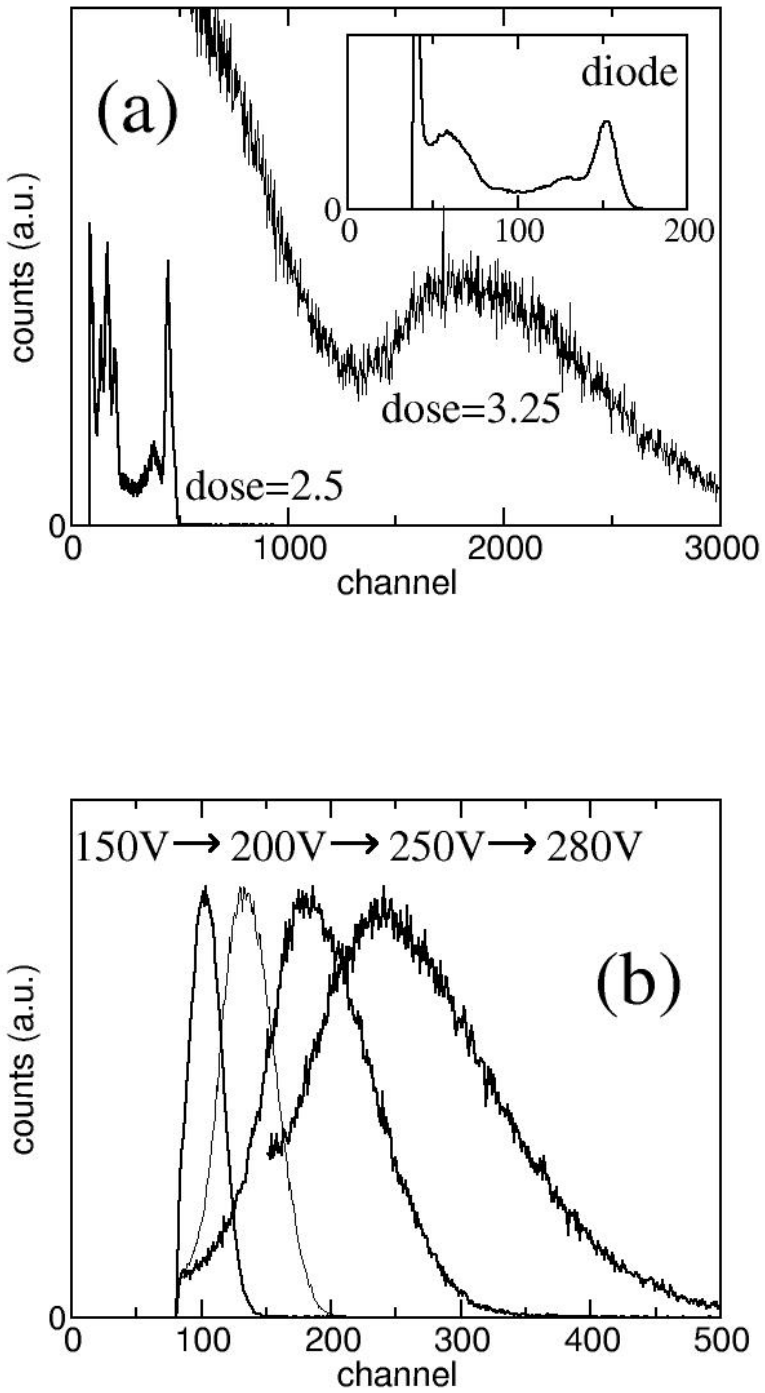


Figure 8: (a) The $^{241}$Am spectra acquired with LGADs featuring a gain layer dose of either $2.5 \cdot 10^{12}$ cm$^2$ or $3.25 \cdot 10^{12}$ cm$^2$. In the inset, the same spectrum acquired by a diode (gain=1). (b) The $^{55}$Fe spectra aquired with LGADs featuring a gain layer dose of $3 \cdot 10^{12}$ cm$^2$, for different bias voltages. The $x$-axis shows the PX5 ADC channel number, the $y$-axis shows the counts per channel. The counts for each spectrum are normalized for an easier comparison of the spectra.

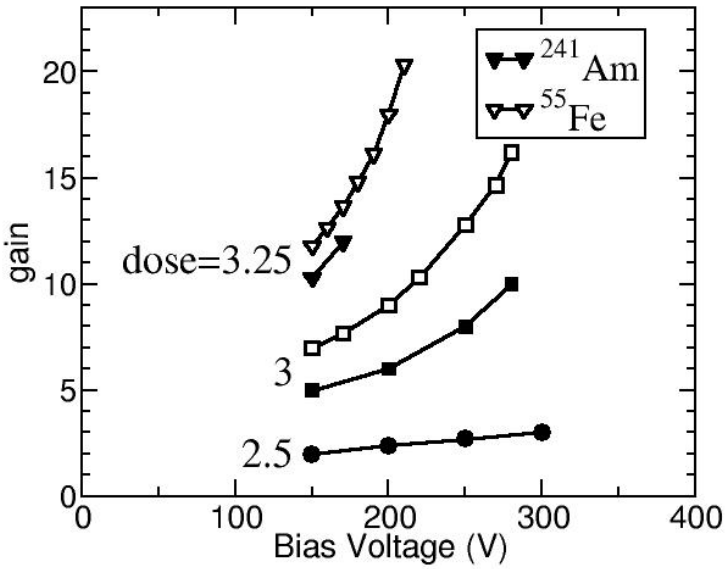


Figure 9: Gain values measured from either the $^{241}$Am 60 keV (solid markers) or the $^{55}$Fe 6 keV (empty markers) peak positions. Measurements are shown for three LGADs differing for the values of the implant doses of their gain layer (in units of $10^{12}$ cm$^2$).

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