Experiment 10

American International University- Bangladesh

Faculty of Engineering (EEE)

Digital Electronics Laboratory

Department of EEE and CoE Undergraduate Program

Laboratory Title: Design of sequential circuits using logic families

Experiment Number: 10 **Due Date: 23 /11/2021 Semester: Fall 2021-2022**

Subject Name: DIGITAL ELECTRONICS LAB [C]

Declaration and Statement of Authorship:

I/we hold a copy of this report, which can be produced if the original is lost/ damaged.

1. This report is my/our original work and no part of it has been copied from any other student's work or from any other source except where due acknowledgment is made.

2. No part of this report has been written for me/us by any other person except where such collaboration has been authorized by the lecturer/teacher concerned and is acknowledged in the report.

I/we understand that:

7. Plagiarism is the presentation of the work, idea, or creation of another person as though it is your own. It is a form of cheating and is a very serious academic offense that may lead to expulsion from the University. Plagiarized material can be drawn from, and presented in, written, graphic and visual form, including electronic data, and oral presentations. Plagiarism occurs when the origin of the material used is not appropriately cited.
8. Enabling plagiarism is the act of assisting or allowing another person to plagiarize or to copy your work

Group Number (if applicable): 02 **Group Submission**

No	Name	Student ID	Dept
01	Ariff, Umar Faruque Ibne	18-36115-1	CSE
02	Bhuiyan, Md Rayhan	18-37285-1	CSE
03	Ahamed, Fardit	18-36119-1	CSE
04	Anika, Asma Sadia	18-36087-1	CSE
05	Fahim, Saimon Haque	18-36509-1	CSE

Submitted To:

MD. SHAHRIAR PARVEZ
Lecturer
Faculty of Engineering
Department of EEE

Title:

Open Ended Lab Experiment Name: Design of sequential circuits using logic families using 555 timers.

Objective:

Design a sequential circuit that utilizes digital gates and implement the design with a logic family of your choice. The design goal is to investigate the circuit output while generating the required input clock signals.

Equipment:

1. 3 probe (red, green, yellow)
2. DCD_hex_Blue (For Output)
3. 3 JK_FF_NEGSR (JK flipflop)
4. Or Gate.
5. 2 Interactive Digital Constant
6. Digital Clock.
7. Ground.

Procedure:

Since the Decade counter 4017 outputs a 10-bit decoded output, where only 1-bit is set high for a particular output pattern, in a cyclic manner, it can be used to generate a sequence such as the one needed for a TLC. For example, the following circuit outputs Green for 4 clock cycles, Yellow for 1 clock cycle and Red for 4 clock cycles. To do that D1 (Pin3), D2 (Pin2), D3 (Pin4), and D4 (Pin7) have been connected to the Green output, D5 (10) has been connected to Yellow output and D6 (Pin1), D7 (Pin5), D8 (Pin6), and D9 (Pin9). The D10 (Pin 11) output can be left unconnected for this example design.

Data Table:

Present State			Next State									Output Transistor		Flip Flop Input	
X3	X2	X1	X_3	X_2	X_1	J_2	K_2	J_1	K_1	J_0	K_0	X_N	X_{N+1}	J	k
0	1	1	1	0	1	1	x	x	1	x	0	0	0	0	x
1	0	1	1	1	1	x	0	1	x	x	0	0	1	1	x
1	1	1	1	1	0	x	0	0	0	x	x	1	0	x	1
1	1	0	0	0	1	x	1	x	1	1	x	1	1	x	0
0	0	1	0	1	1	0	0	1	x	x	0				

k-map:

X_3X_2 \ X_1	0	1
00	x	x
01	x	x
11	1	x
10	x	x

J_0

X_3X_2 \ X_1	0	1
00	x	1
01	x	x
11	x	x
10	x	1

J_1

X_3X_2 \ X_1	0	1
00	x	0
01	x	1
11	x	x
10	x	x

J_2

X_3X_2 \ X_1	0	1
00	x	0
01	x	0
11	x	1
10	x	0

K_0

X_3X_2 \ X_1	0	1
00	x	x
01	x	1
11	1	0
10	x	x

K_1

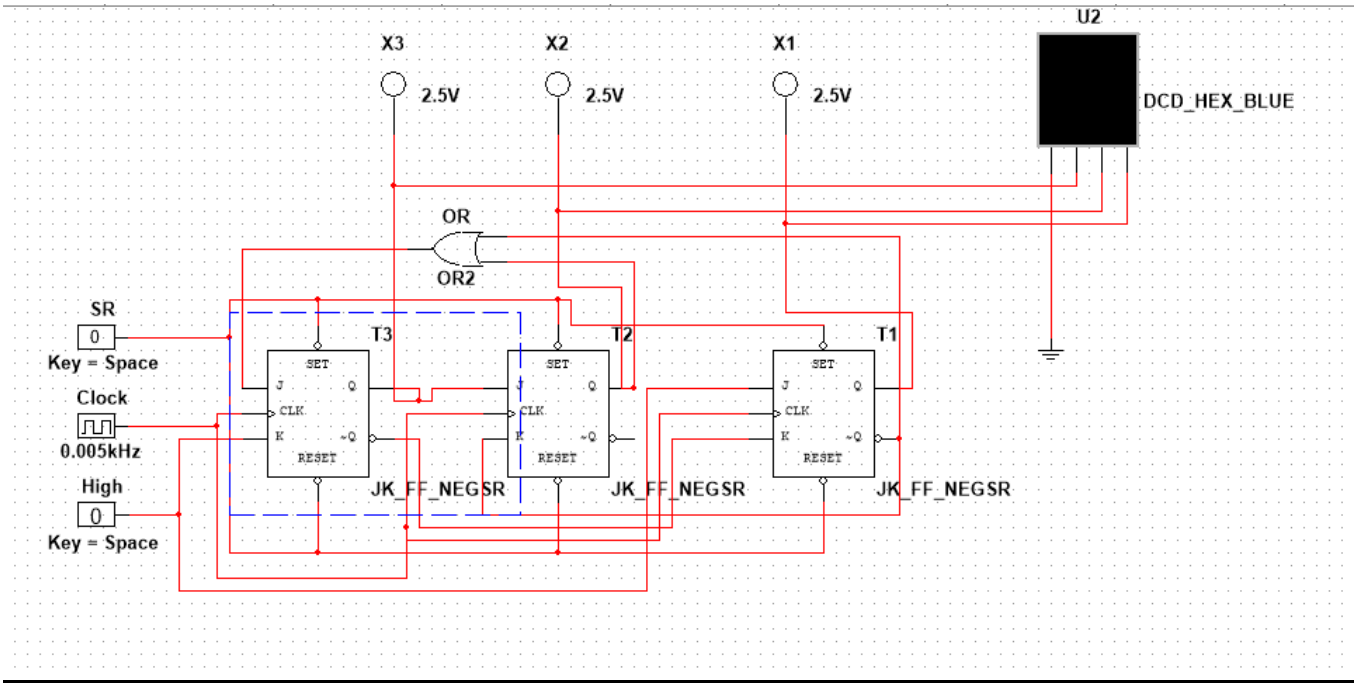
X_3X_2 \ X_1	0	1
00	x	x
01	x	x
11	1	0
10	x	0

k_2

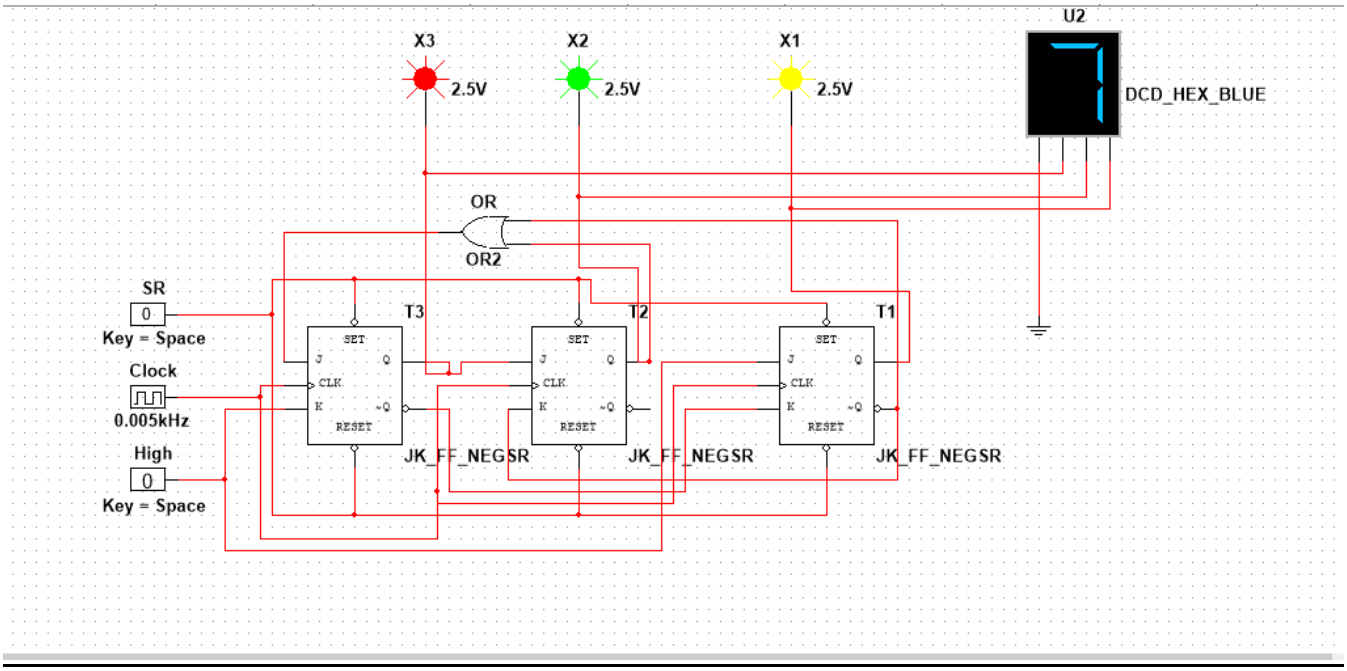
$j_0 = X_1 / X_3$, $k_0 = X_3 . X_2$,

$J_1 = 1$, $k_1 = X_3 / X_1$, $J_2 = X_2$, $k_2 = X_1$

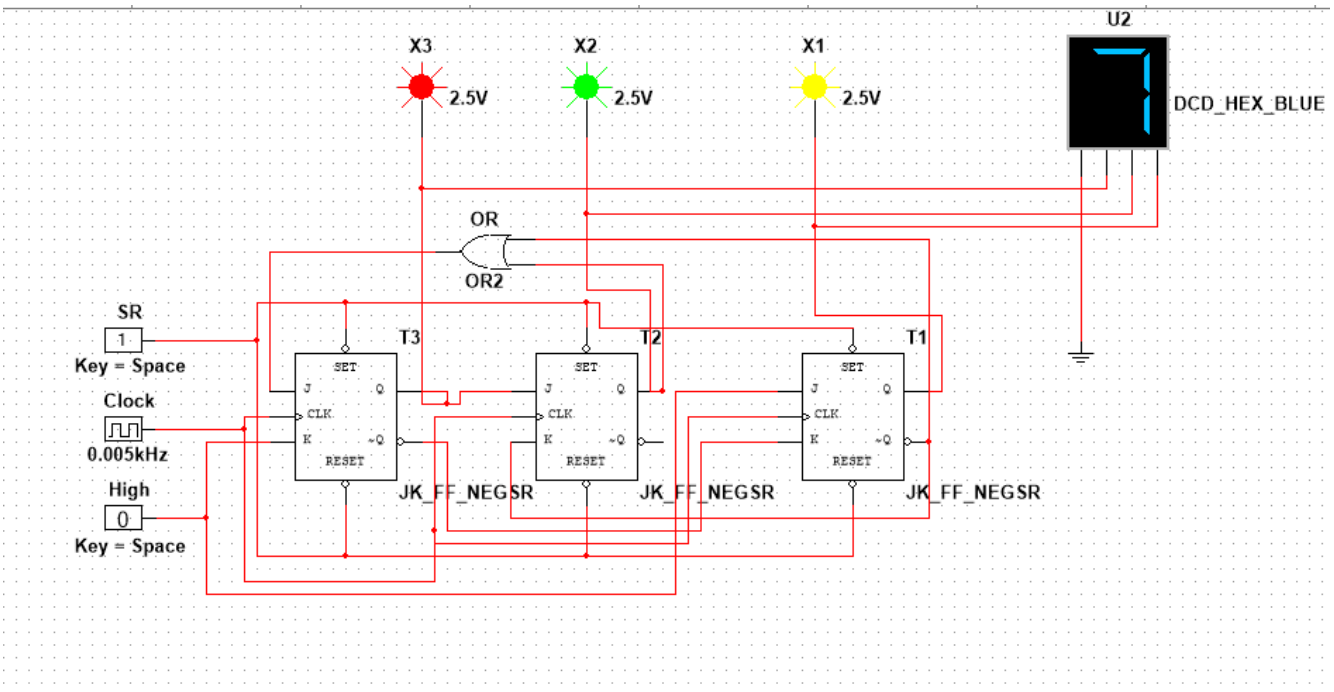
Circuit Diagram:



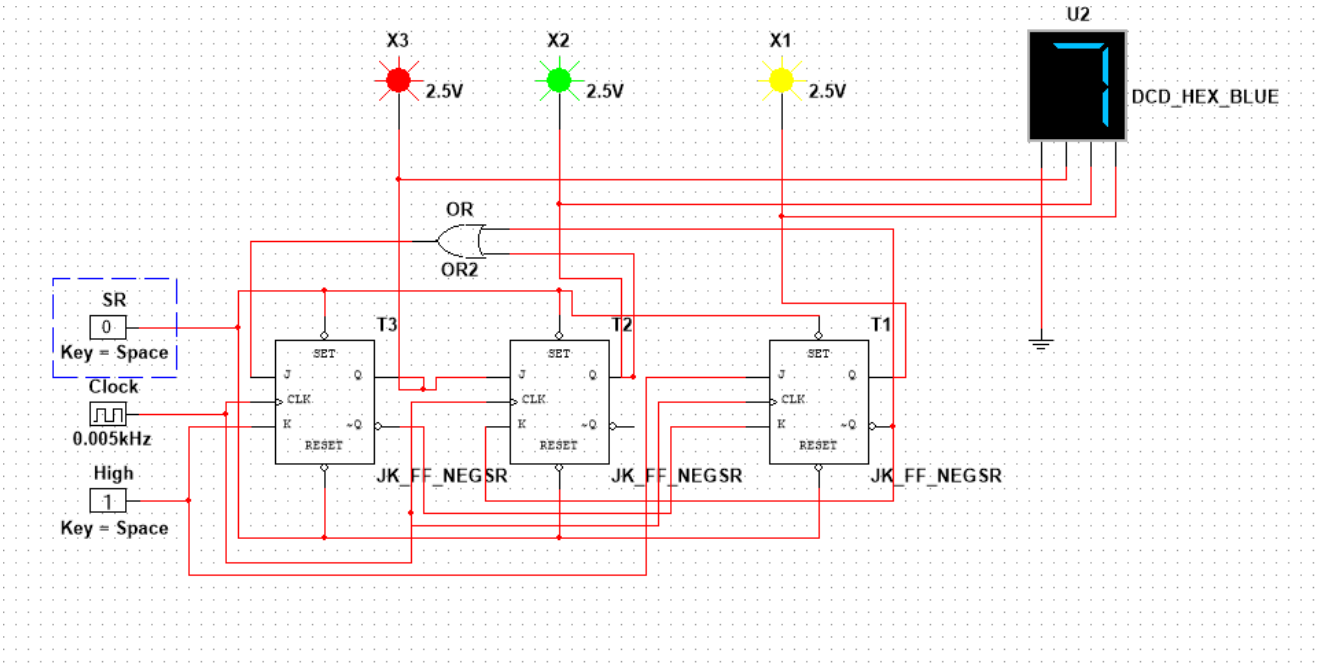
Simulation Screenshots:



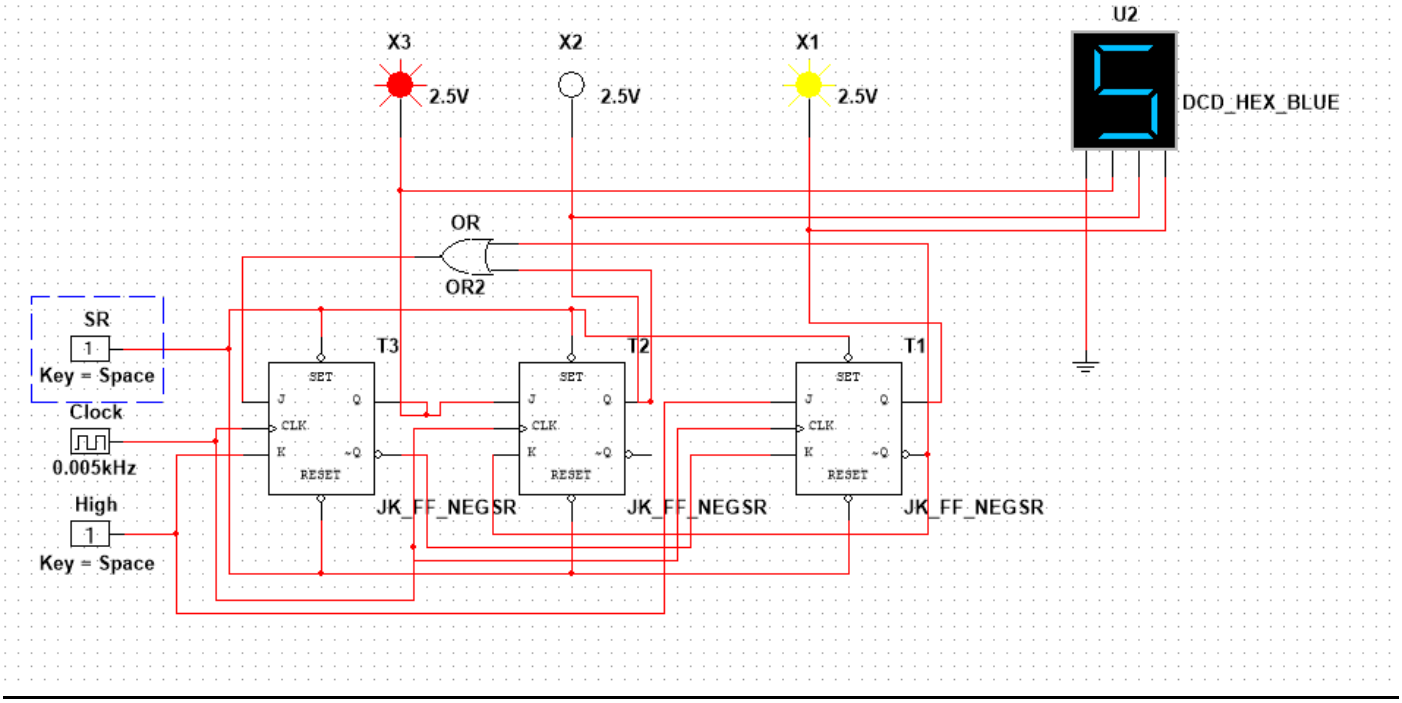
For 00

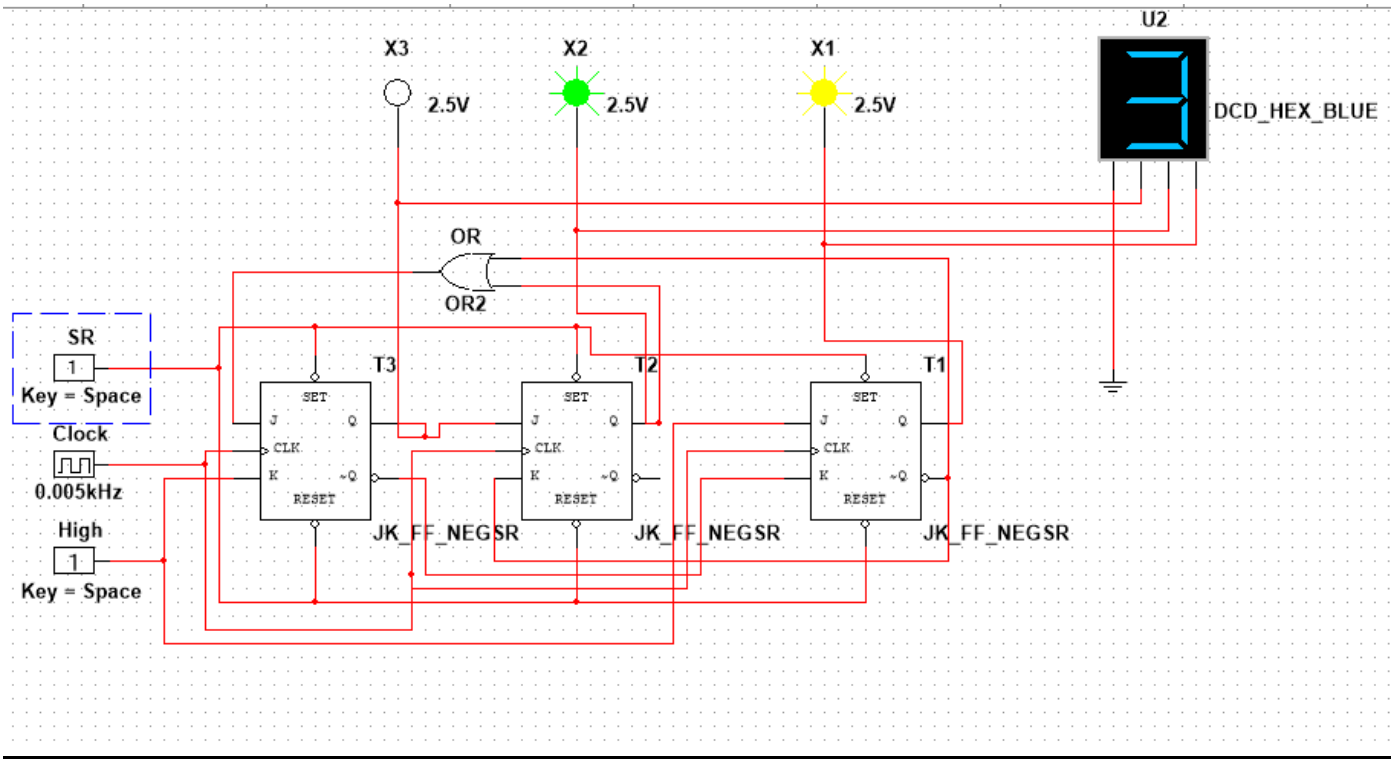


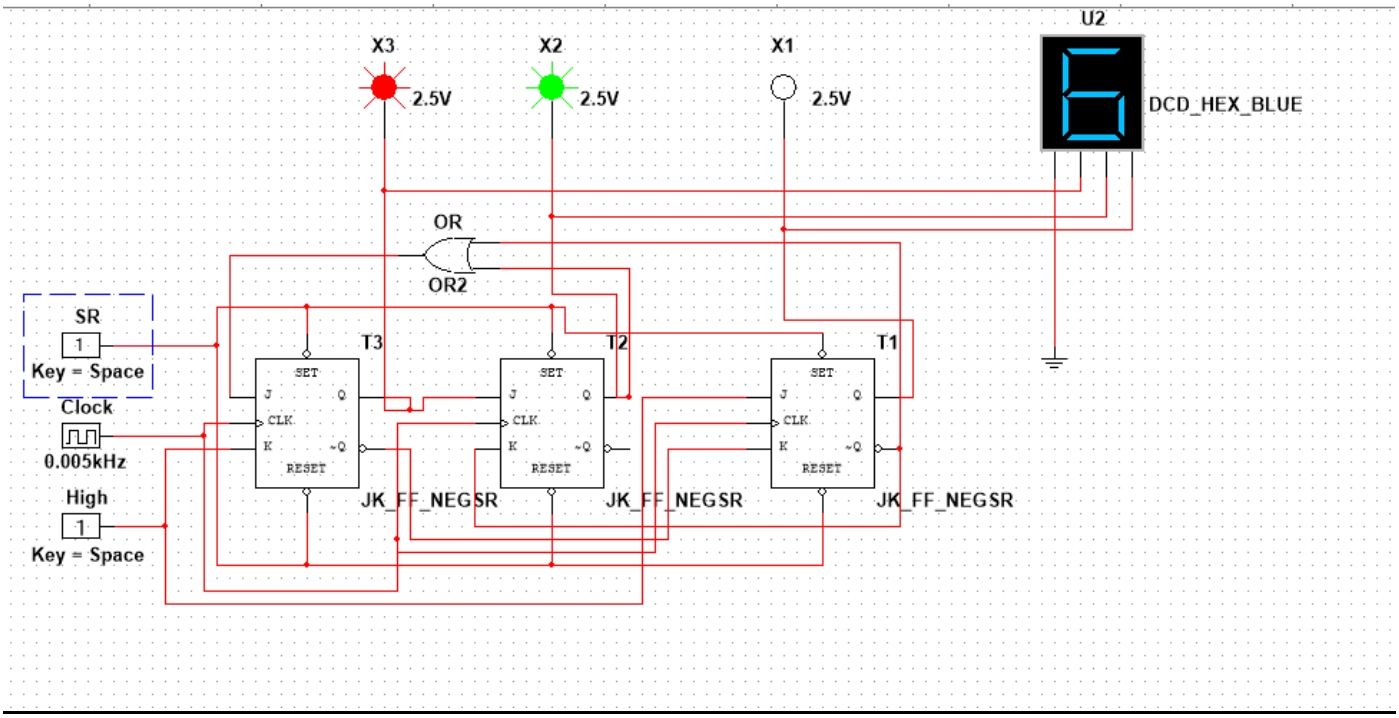
For SR 1

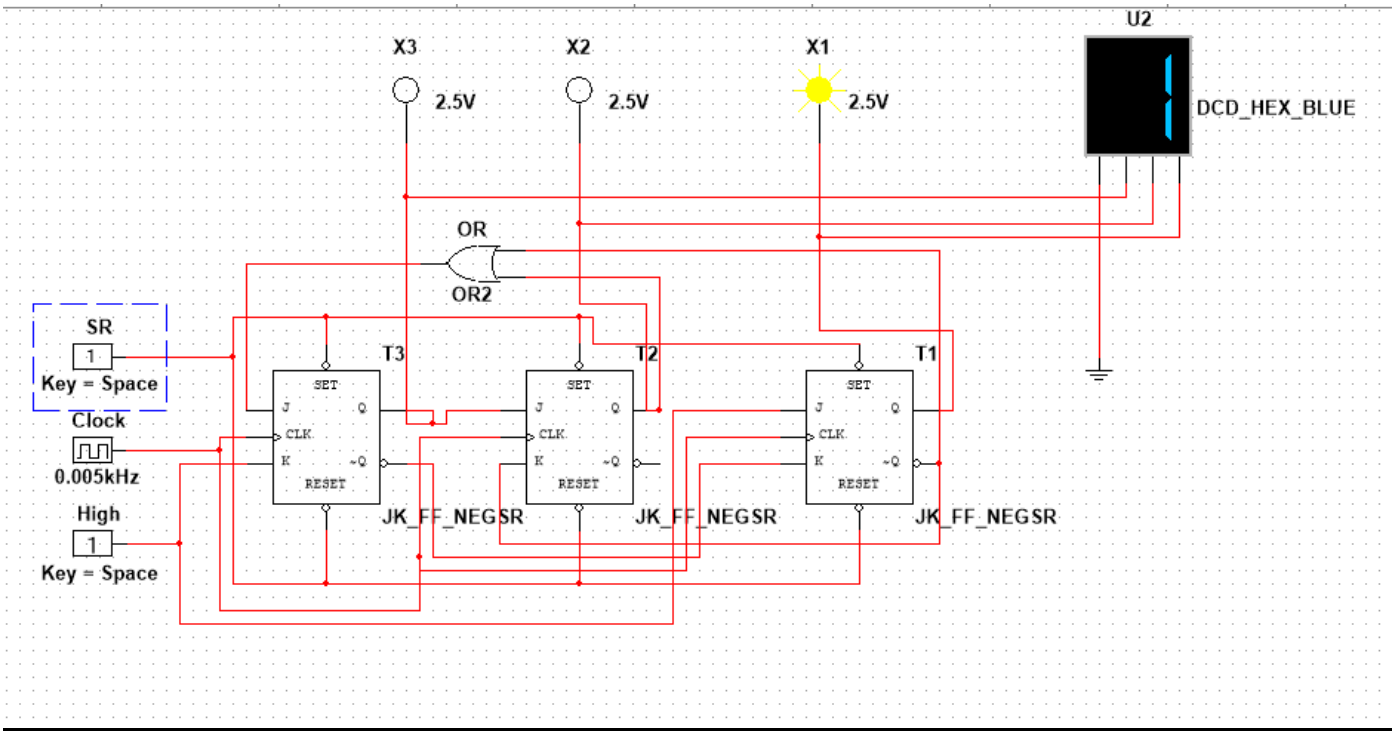


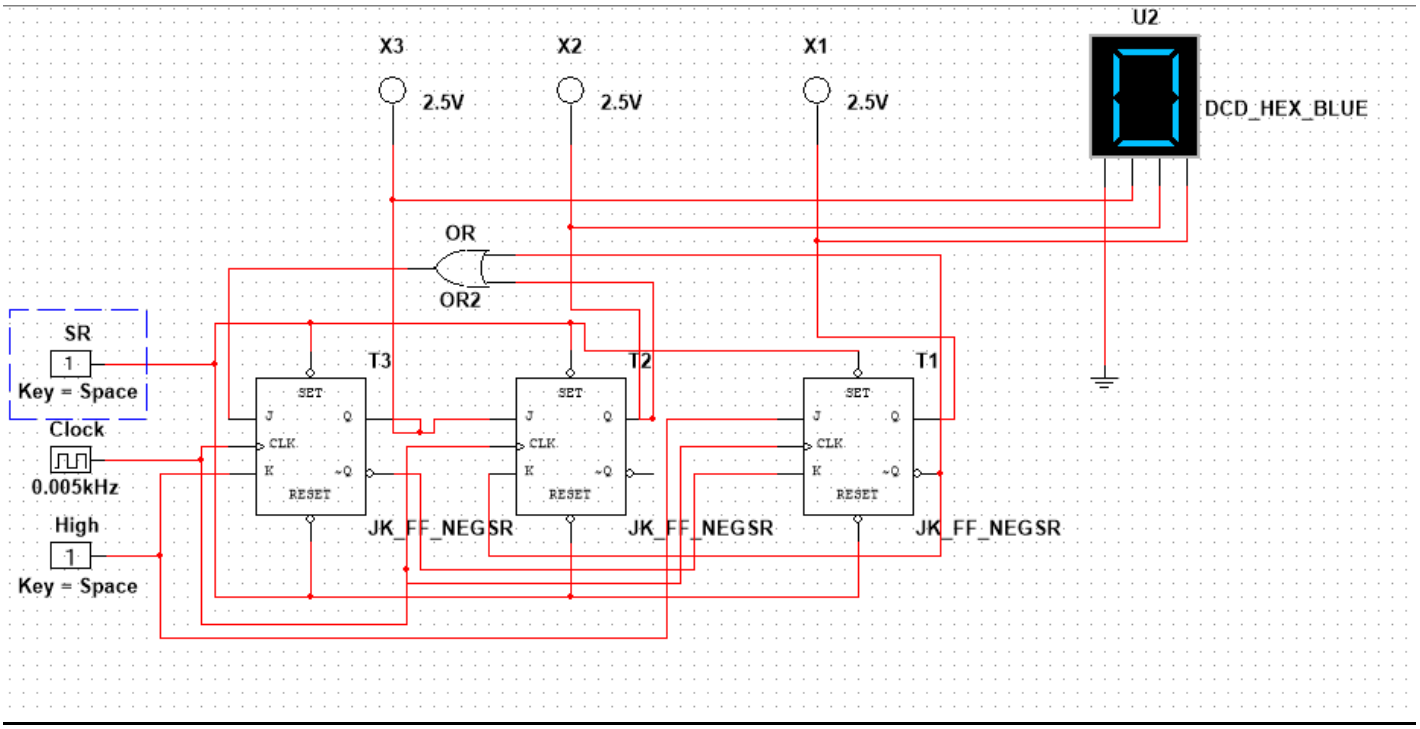
For High 1


U2
X3
X2
X1
2.5V
2.5V
2.5V
DCD_HEX_BLUE
OR
OR2
SR
1
Key = Space
Clock
0.005kHz
High
1
Key = Space
T3
T2
T1
SET
J
Q
CLK
K
~Q
RESET
JK_FF_NEGSR
JK_FF_NEGSR
JK_FF_NEGSR


U2
X3
X2
X1
2.5V
2.5V
2.5V
DCD_HEX_BLUE
OR
OR2
SR
1
Key = Space
Clock
0.005kHz
High
1
Key = Space
T3
T2
T1
SET
J
Q
CLK
K
~Q
RESET
JK_FF_NEGSR
JK_FF_NEGSR
JK_FF_NEGSR


U2
X3
X2
X1
2.5V
2.5V
2.5V
DCD_HEX_BLUE
OR
OR2
SR
1
Key = Space
Clock
0.005kHz
High
1
Key = Space
T3
T2
T1
SET
J
Q
CLK
K
~Q
RESET
JK_FF_NEGSR
JK_FF_NEGSR
JK_FF_NEGSR


U2
X3
X2
X1
2.5V
2.5V
2.5V
DCD_HEX_BLUE
OR
OR2
SR
1
Key = Space
Clock
0.005kHz
High
1
Key = Space
T3
T2
T1
SET
J
Q
CLK
K
~Q
RESET
JK_FF_NEGSR
JK_FF_NEGSR
JK_FF_NEGSR



For 11

Result and Data Analysis:

For SR=1 and high = 1

After running the experiment we will get our first value 0. For 0 all probes will be off then we will get the second value 5.

For 05, the red and yellow probe will blink. Then we will get our 3rd value 03. For 03 green and the yellow probe will blink. Then we will get our 4th value 06. Red and Green probe will blink. Then we will get our last value 01. For 01, the yellow probe will blink.

For SR=0 and high =0, SR=1 and high=0, SR=0 and high =1

For these 3 cases red-green, and the yellow probe will blink all the time.

Discussion:

Our Experiment no 10 is a performance based experiment which we implemented. In this experiment there are many calculative part and also simulative part. This experiment is based on an irregular synchronous counter design with 555 timer. And in this experiment my sequence is 35761. I attached my calculated part which includes 5 step. 1st arrange the sequence into present state and next state

then calculated them based on rules of JK flip-flop in the jn, kn table. Then create the k-map for those combinations and grouped them. After that we find the equation. Then we draw the circuit diagram according to our equation then implemented them is Multisim. We put the calculated values into the 555 timer. After implementing the circuit into Multisim we saw that in LED Hex display irregular counter shown. In the oscillator we couldn't saw any wave so that we can measure the time difference. We didn't face any difficulties while doing the experiment. From this lab experiment we get to learn about how 555 Timer ICs and irregular counter designs. We also noticed the differences between the regular counter and irregular counter.