Design and Implementation of Ternary Logic Circuits for VLSI Applications

G. Thrishala, K.Ragini

Abstract: ***This paper mainly concentrates on the design and implementation of ternary logic circuits. The ternary numeral system has its base as 3. Ternary logic will use three symbols, which are, 0,1 and 2. The ternary logic has significant merits over binary logic in designing digital circuits. In this paper, it is proposed to implement a half adder circuit using ternary 3 to 1 multiplexer. The main objective of the work is, to design and implement ternary logic circuits and to analyse the function of the ternary combinational circuits using mentor graphics tool in 90nm technology. This paper also compares the ternary half adder design using k-map method with the proposed ternary half adder using multiplexer in terms of power dissipation, propagation delay and transistor count.***

Keywords: Ternary logic, MVL (Multi-Valued Logic).

I. INTRODUCTION

MVL (Multi-Valued Logic) is also called as Multiple-Valued, Multi-Valued logic. MVL that is, Multi-Valued Logic is termed as a technique that has more than two possible states or two truth values. A two-valued logic can be extended to a n-valued logic, that is, for example, in a three valued logic i.e., base or radix as three, it is termed as ternary logic and a quaternary logic i.e., radix as four is used for four valued logic and so on. Such a three valued logic with logic symbols as 0,1 and 2 and four valued logic has logic states of 0,1,2 and 3.

The ternary numeral system has its base or radix as 3 [1]. Radix generally defined as the number of unique digits or unique symbols that can be expressed using a single digit. In a binary system, the two logic symbols 0 and 1 are used to represent a value, and coming to the ternary system, the three logic symbols (0, 1 and 2) are used. The bipolar notation is one of the methods in the ternary logic system which is denoted with symbols -1, 0, 1. In this paper, the notation used is 0,1 and 2.

The ternary logic system gives the meaning of three-valued switching. Three valued logic system or ternary logic system has many benefits when compared with the binary logic system in designing digital circuits. reduction in chip area can be achieved, and more importantly, easy error detection and error correction codes can be employed.

For instance, more data can be transmitted over an arrangement of lines in a given length, diminishing in the complexity of interconnections is observed, decrease in chip area can be accomplished, and more significantly the error detection and error correction of codes can be accomplished.

The ternary logic system has some significant merits over the binary logic system [2,3]. To implement the different logic functions, the decrease in the number of interconnections in a circuit is observed, in this way, the chip area has been reduced, and importantly more data can be transmitted and lesser memory is required. Apart from this, at very higher speeds, the serial and some serial-parallel operations are carried out. It's been used in applications like areas of communications and digital signal processing.

II. METHODOLOGY

In this section, the ternary building blocks like ternary inverters, ternary logic gates, ternary decoder, ternary multiplexer, and half adder circuits are designed.

A. DESIGN AND IMPLEMENTATION TERNARY INVERTER:

STI (simple ternary inverter), PTI (positive ternary inverter) and NTI (Negative ternary inverter) are the three basic ternary elements.

$$STI = X_i = 2 - X$$

$$PTI,\ NTI = X_i = \begin{cases} 2 - \mathrm{i} \rightarrow \mathrm{X} = \mathrm{i} \\ \mathrm{i} \rightarrow \mathrm{X} \neq \mathrm{i} \end{cases}$$

Where 'i' takes the value of '2' for PTI and '0' for NTI.

i. STI (SIMPLE TERNARY INVERTER):

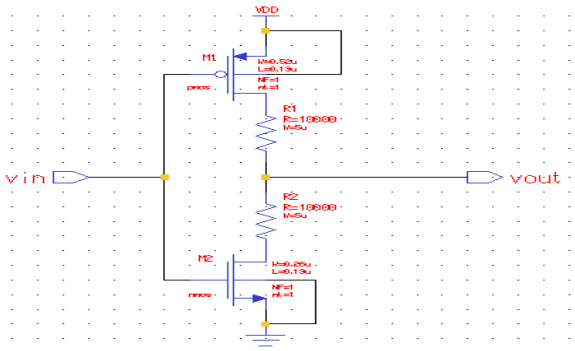

Fig 2.1: Schematic of simple ternary inverter

The circuit diagram of a simple ternary inverter is shown in Figure 2.1. The simple ternary inverter consists of two MOS transistors and two resistors.

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The working of STI is, if the input voltage Vin is 0volts (logic 0), then NMOS becomes off and PMOS becomes on, as a result, there will be no flow of current in resistors and the output becomes logic 2(i.e., 1.8 volts).
On contrary, if the input voltage is 1.8 volts (logic 2), then NMOS becomes turned on and PMOS is turned off, which impacts as, there will be no flow of current in the resistors and the output becomes logic 0(i.e., 0 volts).
And if the input voltage is 0.9volts (logic 1), which is equal to VDD/2 voltage level, both PMOS and NMOS become turned on and consequently current could flow in both the resistors. The resistors R value is 1 mega ohm are chosen such that it should be much larger than the resistance of the turned-on transistors and they are used for less power dissipation. The output waveforms of simple ternary inverter are shown in Fig 2.2.

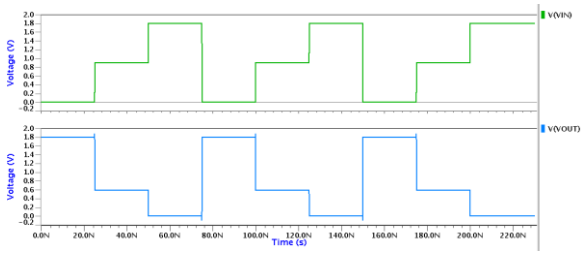

Fig 2.2: Transient analysis of simple ternary inverter

The circuit is supplied with different VDD voltage values that are 0V, 0.9V and 1.8V is required in order to detect three different logic levels which are 0, 1 and 2 for the input signal. The graph of voltage versus time in Fig 2.2 for every step of the input for each interval is set at 25ns. For the first interval between 0 to 24.99ns, the input is 0 V (logic 0) then it is followed by the second interval between 25ns to 49.99ns as the input is 0.9 V (logic 1). Then, the last interval is between 50ns to 75.99n as the input voltage is 1.8 V (logic 2).

ii. PTI (POSITIVE TERNARY INVERTER):

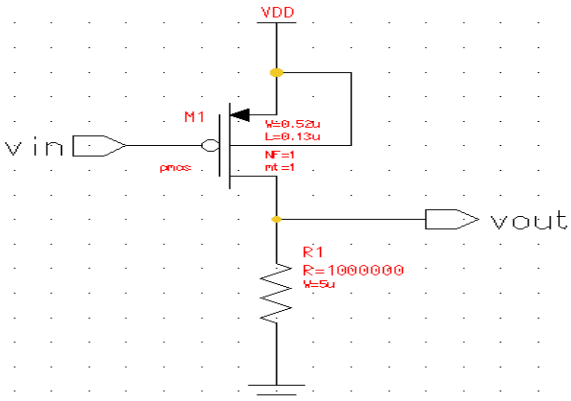

Fig 2.3: Schematic of positive ternary inverter

The schematic of a positive ternary inverter is shown in Fig 2.3. In the case of PTI, when input Vin reaches to 0 volts (logic 0) then the output is 1.8 volts (logic2) because at this time PMOS is turned on, since this path acts like a close path and the total voltage drop appears at the output terminal is 1.8 volts**.** When input Vin=0.9 volts or (logic 1) then output equals 1.8 volts or appeared as a logic 2. When input appears as 1.8 volts or as a logic 2 the PMOS gate to source terminal is open. As a result, the output appears as 0 volts (logic 0) can be observed in Fig 2.4.

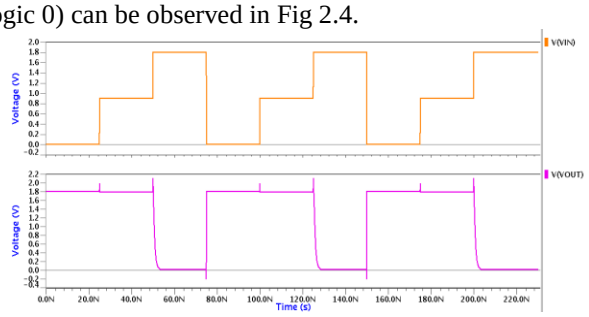

Fig 2.4: Transient analysis of positive ternary inverter.

iii. NTI (NEGATIVE TERNARY INVERTER):

The circuit diagram of the negative ternary inverter is shown in Figure 2.5 and the output waveforms of the negative ternary inverter are shown below in Figure 2.6.

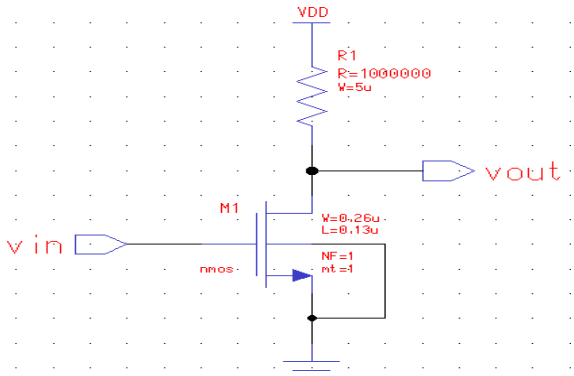

Fig 2.5: Schematic of negative ternary inverter

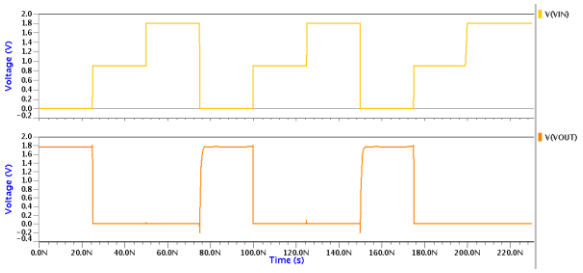

Fig 2.6: Transient analysis of negative ternary inverter

When Vin =0.9v or 1.8v, NMOS is ON. Current will always conduct when there will be a channel i.e., Vgs>Vt (threshold voltage), gives the voltage of the circuit. So, output as low as 0 volts (logic 0) up to 1.8v can be observed in fig 2.6.

B. TERNARY GATES:

Using ternary inverters, the ternary logics gates are implemented. Like Binary NAND and NOR gates, ternary NAND and NOR gates can also be implemented. Here are some simple ternary NAND, T- NOR, T-AND and T-OR gates are designed and implemented using resistors. The truth table of ternary logic gates like ternary NAND, ternary NOR, ternary AND, ternary OR and ternary EX-OR are given in Table 1.

Table 1: Truth table of ternary input logic gates.

A	B	T-NAND	T-NOR	T-AND	T-OR	T-EXOR
0	0	2	2	0	0	0
0	1	2	1	0	1	1
0	2	2	0	0	2	2
1	0	2	1	0	1	1
1	1	1	1	1	1	1
1	2	1	0	1	2	1
2	0	2	2	0	2	2
2	1	1	1	1	2	1
2	2	0	0	2	2	0

i. TERNARY NAND GATE:

The circuit diagram of ternary NAND(T-NAND) gate is shown in fig 2.7.

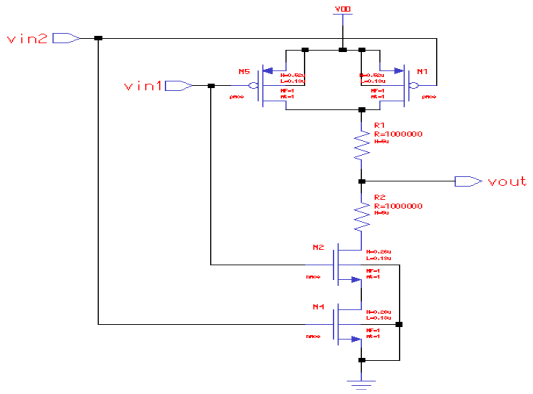

Fig 2.7: Schematic of ternary NAND gate.

ii. TERNARY AND GATE:

The circuit diagram of ternary AND(T-AND) gate is shown in fig 2.8.

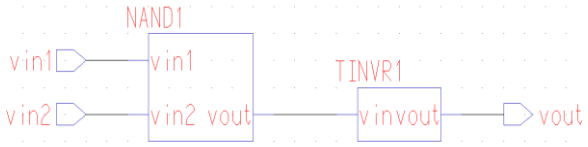

Fig 2.8: Schematic of ternary AND gate.

iii. TERNARY NOR GATE:

The circuit diagram of ternary NOR(T-NOR) gate is shown in fig 2.9.

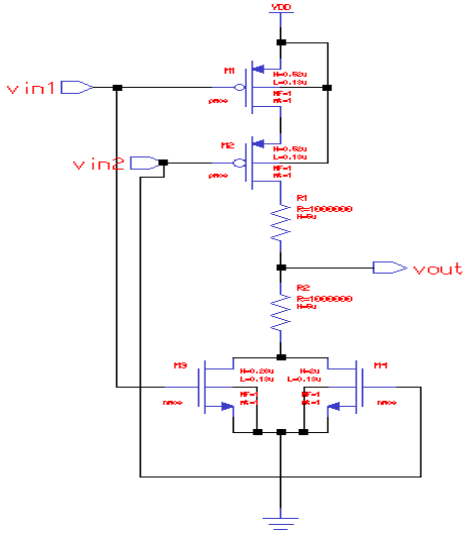

Fig 2.9: Schematic of ternary NOR gate.

iv. TERNARY OR GATE:

The circuit diagram of ternary OR(T-OR) gate is shown in fig 2.10.

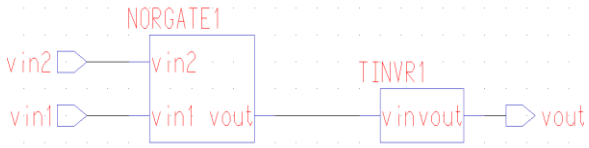

Fig 2.10: Schematic of ternary OR gate.

C. TERNARY DECODER (one to three decoder):

In ternary decoder circuit, we use two negative ternary inverters, one positive ternary inverter and a negative ternary NOR(NT-NOR) gate. The circuit diagram of ternary decoder is shown in Figure 2.11.

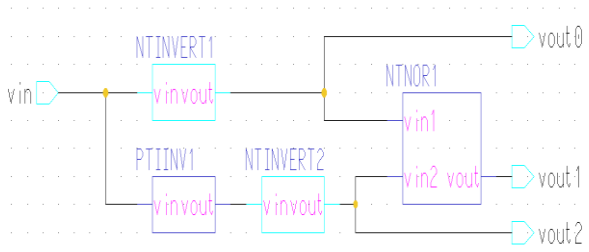

Fig 2.11: Schematic of ternary decoder.

The working of ternary decoder is, if vin = 0volts(logic 0), the NTI inverter gives output as 2 ,then, vout0 = 2, PTI inverter also gives output as 2 for the input 0, and input of NTI becomes 0 and output is 2 implies vout2=0,and then NT-NOR inputs are as 0 and 2 then output is 0 that is vout1 is 0.

Similarly , if vin = 0.9 volts (logic 1) , the NTI inverter gives output as 0 ,then , vout0 = 0, PTI inverter also gives output as 2 for the input 0 ,and input of NTI becomes 0 and output is 2 implies vout2=0,and then NT-NOR inputs as 0 and 0 then output is 2 that is vout1 is 2.

For vin =1.8 volts(logic 2), the NTI inverter gives output as 0 ,then , vout0 = 0, PTI inverter also gives output as 0 for the input 2 ,and input of NTI becomes 2 and output is 2 implies vout2=0,and then NT-NOR has inputs as 0 and 2 then output is 0 that is vout1 is 0 are observed in Fig 2.12. The truth table of ternary decoder is shown in Table 2.

Table 2: Truth table of ternary decoder.

Vin	Vout0	Vout1	Vout2
0	2	0	0
1	0	2	0
2	0	0	2

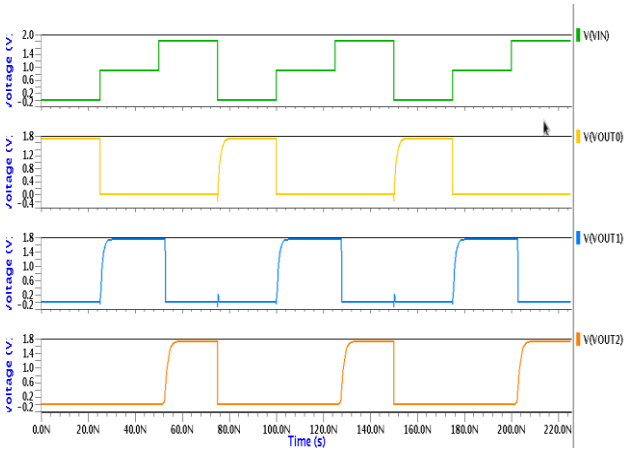

Fig 2.12: Output waveforms of ternary decoder

D. TERNARY MULTIPLEXER:

In this ternary multiplexer circuit, a ternary one to three decoder, three AND gates, and a three-input ternary OR gate. The truth table of ternary multiplexer is shown in Table 3 and the circuit diagram of ternary multiplexer is shown in Fig 2.13.

Table 3: Truth table of 3 to 1 multiplexer

Vin	Vout
0	S0
1	S1
2	S2

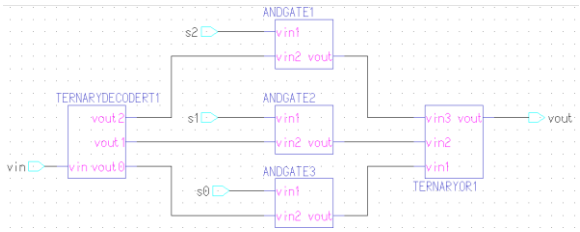

Fig 2.13: Schematic of ternary multiplexer

In working of ternary multiplexer, if vin (select line) = 0, the ternary decoder output gives vout0 as 2, vout1 as 0 and vout2 as 0. Now, input of AND gate becomes s0 and vout0, as vout0 is 2 then output follows the s0 and similarly for input vin =0.9 (logic 1), it follows output as s1 and for vin=1.8(logic 2) it follows output as s2 can be observed in Fig 2.14.

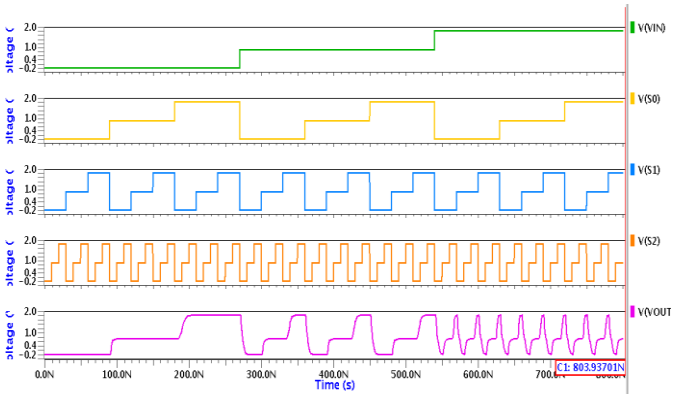

Fig 2.14: Output waveforms of ternary multiplexer.

The Table 4 illustrates about the ternary decoder and ternary multiplexer circuit in terms of propagation delay and power dissipation. Ternary decoder needs only 7 transistors to implement the circuit and has power dissipation of 10.05µ Watts and propagation delay of 3.32ns. Ternary multiplexer has power dissipation of 10.9µ Watts and propagation delay of 2.95ns.

Table 4: Ternary circuits in terms of propagation delay and power dissipation

Ternary circuit	Propagation delay(ns)	Power dissipation(µW)
ternary decoder	3.32	10.05
ternary 3:1 multiplexer	2.95	10.90

E. TERNARY HALF ADDER USING K-MAP METHOD:

Half adder circuit using k-map method consists of two ternary decoders, eight NAND gates, two 3-input NAND gates and one STI (simple ternary inverter) and the schematic of ternary half adder circuit is shown in Fig 2.15.

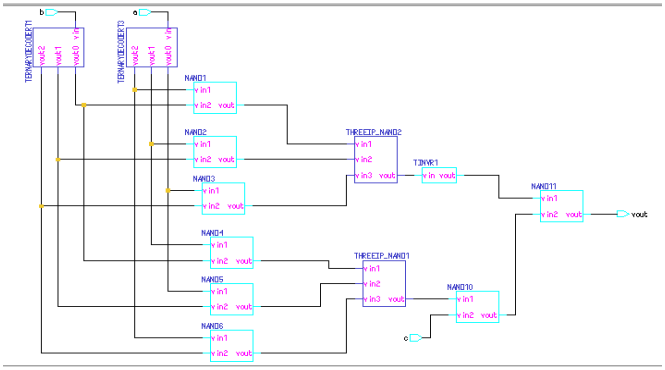

Fig 2.15: Schematic of ternary half adder circuit using k-map method.

III. PROPOSED METHOD

A. DESIGN AND IMPLEMENTATION OF PROPOSED TERNARY HALF ADDER:

The circuit diagram of proposed ternary half adder is shown in Fig 3.1 and the truth table values of a ternary half adder is given in Table 5.

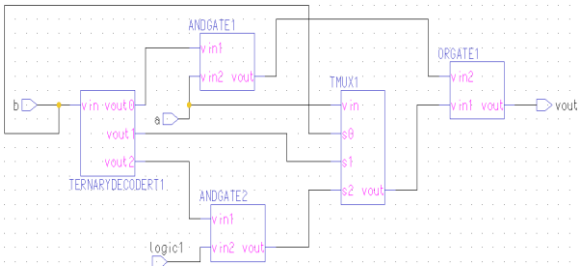

Fig 3.1: Schematic of proposed ternary half adder.

The working of proposed ternary half adder circuit is, if a=0 and b= 0 then output of decoder is vout0 as 2, vout1 as 0 and vout2 as 0. AND gate 1 gives output as 0 since one of the inputs a=0, AND gate 2 outputs as 0 since vout2 is 0. And then, the ternary multiplexer select line is 0, then it follows the output same as the s0. Now OR gate has input combinations of 0 and 0, then output of the half adder circuit is 0. Similarly, for all combinations of a and b, it outputs according to the circuit and these can be observed in Fig 4.1.

Table 5: Truth table of proposed ternary half adder

a	b	Sum	carry
0	0	0	0
0	1	1	0
0	2	2	0
1	0	1	0
1	1	2	0
1	2	0	1
2	0	2	0
2	1	0	1
2	2	1	1

IV. RESULTS

The output waveforms of proposed ternary half adder circuit are shown in Fig 4.1.

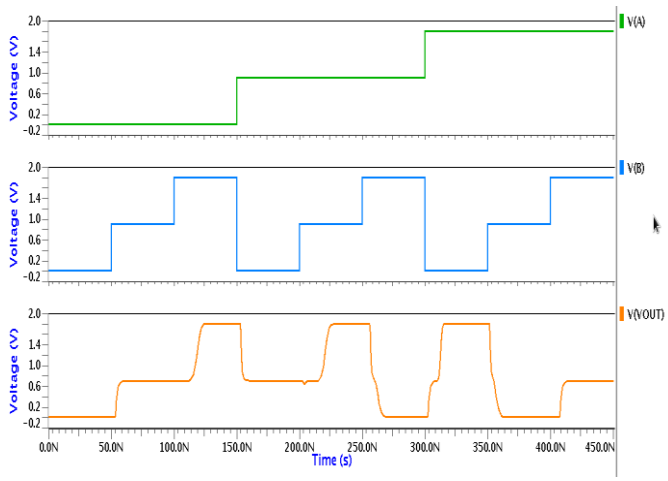

Fig 4.1 Output waveforms of proposed ternary half adder.

The comparison results of ternary half adder circuits in terms of propagation delay, power dissipation and transistor count are shown in Table 6.

Table 6: Comparison of ternary half adder circuits.

Ternary half adder circuit	**Propagation delay(ns)**	**Power dissipation(μW)**	**Transistor count**
Ternary half adder circuit using k-map method	23.57	22.70	66
Proposed ternary half adder	3.71	21.5	56

V. DISCUSSION

PTI and NTI are the inverters which produce only two levels at the output can be called as binary inverters where as STI, which generates three logic levels at the output can be called as ternary logic.

From Table 6, it is observed that the number of transistors is less in the proposed ternary half adder circuit when compared to the ternary half adder circuit using the k-map method. The power dissipation is slightly less in the proposed ternary half adder circuit that is 21.5 micro watts and whereas in ternary half adder using k-map has power dissipation as 22.7 micro watts. And the propagation delay for the proposed half adder circuit is 3.71ns, that is there is a tremendous decrease in the delay of the circuit.

VI. CONCLUSION

The proposed designs have a much lower propagation delay compared to existing design of a half adder circuit, furthermore, they lead to significant reductions in the component count as well as in the power dissipation of the circuit. We can conclude that, proposed design has improved the propagation delay and reduction in transistor count.

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Dr.K.Ragini, working as Professor in ECE Department of G.Narayanamma Institute of Technology& Science(For Women). She has 23 Years of Teaching Experience. Completed her Ph.D. from JNTUH in 2013. She had published papers in 35 reputed journals. As an FDP Coordinator, she had organized more than 10 workshops. She Received “Women Achiever” Award from Accenture on women's day 2017, ‘Academic Excellence Award’ in GNITS in 2007. Authored 2 Books: 1. Variable Threshold MOSFETS, Research India Publications 2. Variable Threshold MOSFET Applications Research India Publications. She has actively participated in various Research activities and received a funding of 4.8 lakhs from AICTE.