EEE 304 Idea Analysis

Smart Traffic System

Objective

Well defined and organized Traffic System helps reduce traffic jams and people's suffering on the road and can save valuable time. Keeping all in mind a four-way road traffic signal system is developed in this project using Digital Logic Circuits.

Introduction

In this project, modeling of smart traffic system of four-way four-lane road along with pedestrian crossing has been implemented using PWM generator, ring counters, and logic gates.

The layout of the road has a symmetrical top view with a roundabout at the junction of the four roads. All roads are divided by road-divider Islands and each side of the roads has dual lanes.

In this scheme, **transport passing and pedestrian crossing**, both have been implemented **without completely stopping all the roads** for a single second and it was ensured that the rush of the passing transports or cars can be minimized efficiently.

System Notations

Roads: Four Roads have been marked as **A, B, C, D.**

Pedestrian Paths:

a) If anyone stands on Road A Island facing towards the roundabout, then the path **from his/her standing island to his/her right-hand side footpath of Road A** is marked as Pedestrian path **IA**.
b) The path **from his/her standing island to his/her left-hand side footpath of Road A** is marked as Pedestrian path **IA/**.
c) Similar definition is taken for pedestrian paths **IB, IB/, IC, IC/, ID, ID/.**

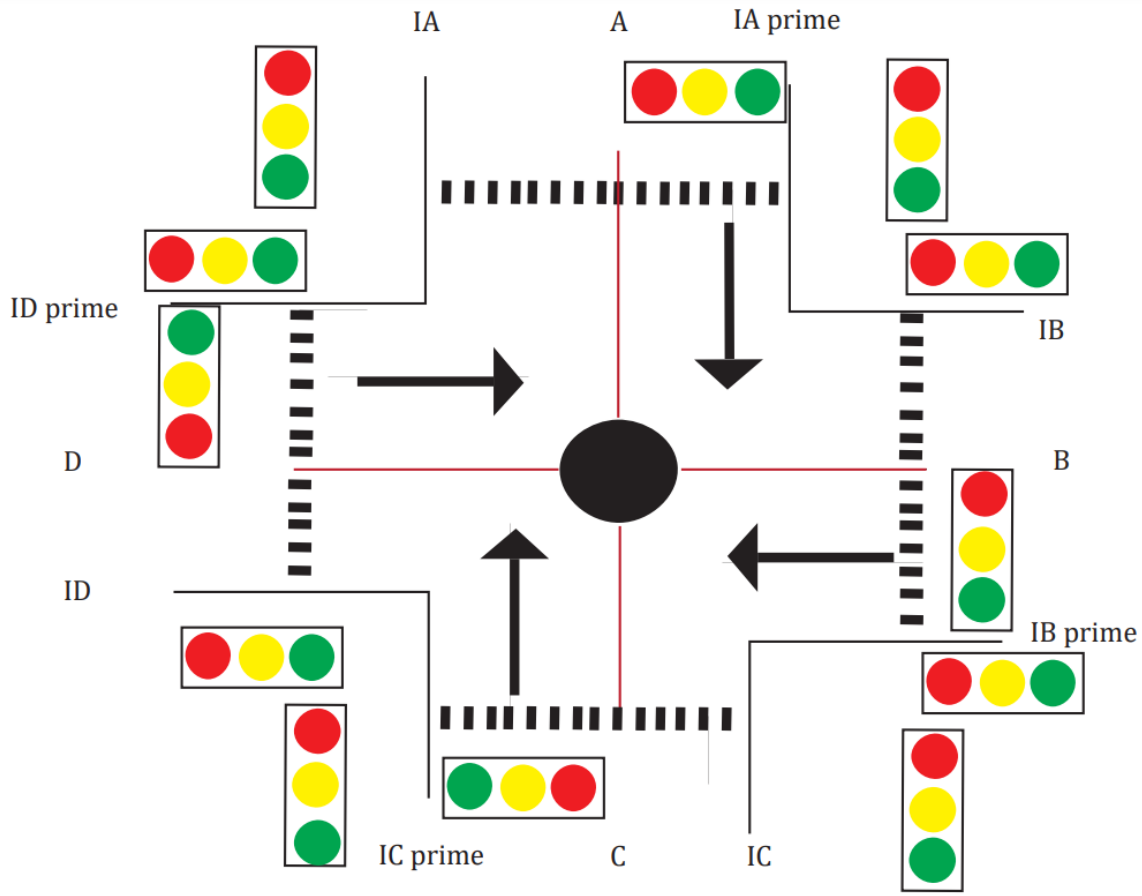


Figure: Four Way Smart Traffic Control System with Pedestrian Control

System Function

The system works in a cyclic order.

The first trigger is for road A. At first, Transports will come out of Road A and enter into Road **B, C, D**. At this time, outgoings from Road **B, C, D** remain off.

At this time-the pedestrian path, **IA** is free for the pedestrians of this portion of the road.

After that, the yellow light of Road A would give a signal for the outgoing transports of road A that, now they have to stop and wait. At the same time, the yellow light of Road B would give a signal for the outgoing transports of road B that, they would start soon.

After that, outgoing transports of road A are stored for the next three triggers of this cycle, and at the same time, Pedestrian path **IA**/ is free, and the pedestrians can move from the island to **A**/ side and vice versa.

This is the first trigger of a cycle.

A similar operation will happen for roads **B, C, D**. After the completion of the trigger of road D, one cycle will be complete.

So, one point is to be noted that, the pedestrians would cross the road halfway, not the entire road at a time.

Also, for the pedestrians, not all the four roads are completely stopped for a moment and it is a very important issue because there is always a rush near a four road junction in a megacity.

Logic Analysis and Circuit Synthesis

Logic and Timing of Operations:

Trigger	Signal	Duty Cycle Per Trigger	Start Time (sec)	End Time (sec)	A	B	C	D	IA	IB	IC	ID	IA/	IB/	IC/	ID/
A1	PA1	(0 to 62.5)%	0	22.5	Green	Red	Red	Red	Green	Red	Red	Red	Red	Green	Green	Green
A2	PA2	(62.5 to 87.5)%	22.5	31.5	Green	Red	Red	Red	yellow	Red	Red	Red	Red	Green	Green	Green
A3	PA3	(87.5 to 100)%	31.5	36	yellow	yellow	Red	Red	Red	Red	Red	Red	Red	yellow	Green	Green
B1	PB1	(0 to 62.5)%	36	58.5	Red	Green	Red	Red	Red	Green	Red	Red	Green	Red	Green	Green
B2	PB2	(62.5 to 87.5)%	58.5	67.5	Red	Green	Red	Red	Red	yellow	Red	Red	Green	Red	Green	Green
B3	PB3	(87.5 to 100)%	67.5	72	Red	yellow	yellow	Red	Red	Red	Red	Red	Green	Red	yellow	Green
C1	PC1	(0 to 62.5)%	72	94.5	Red	Red	Green	Red	Red	Red	Green	Red	Green	Green	Red	Green
C2	PC2	(62.5 to 87.5)%	94.5	103.5	Red	Red	Green	Red	Red	Red	yellow	Red	Green	Green	Red	Green
C3	PC3	(87.5 to 100)%	103.5	108	Red	Red	yellow	yellow	Red	Red	Red	Red	Green	Green	Red	yellow
D1	PD1	(0 to 62.5)%	108	130.5	Red	Red	Red	Green	Red	Red	Red	Green	Green	Green	Green	Red
D2	PD2	(62.5 to 87.5)%	130.5	139.5	Red	Red	Red	Green	Red	Red	Red	yellow	Green	Green	Green	Red
D3	PD3	(87.5 to 100)%	139.5	144	yellow	Red	Red	yellow	Red	Red	Red	Red	yellow	Green	Green	Red
		Total Cycle Time	2 Min 24 Second													

Synthesis of Signals:

The signals are generated from the **logical** column operation of the above table using 7432 IC.

The signals are given below:

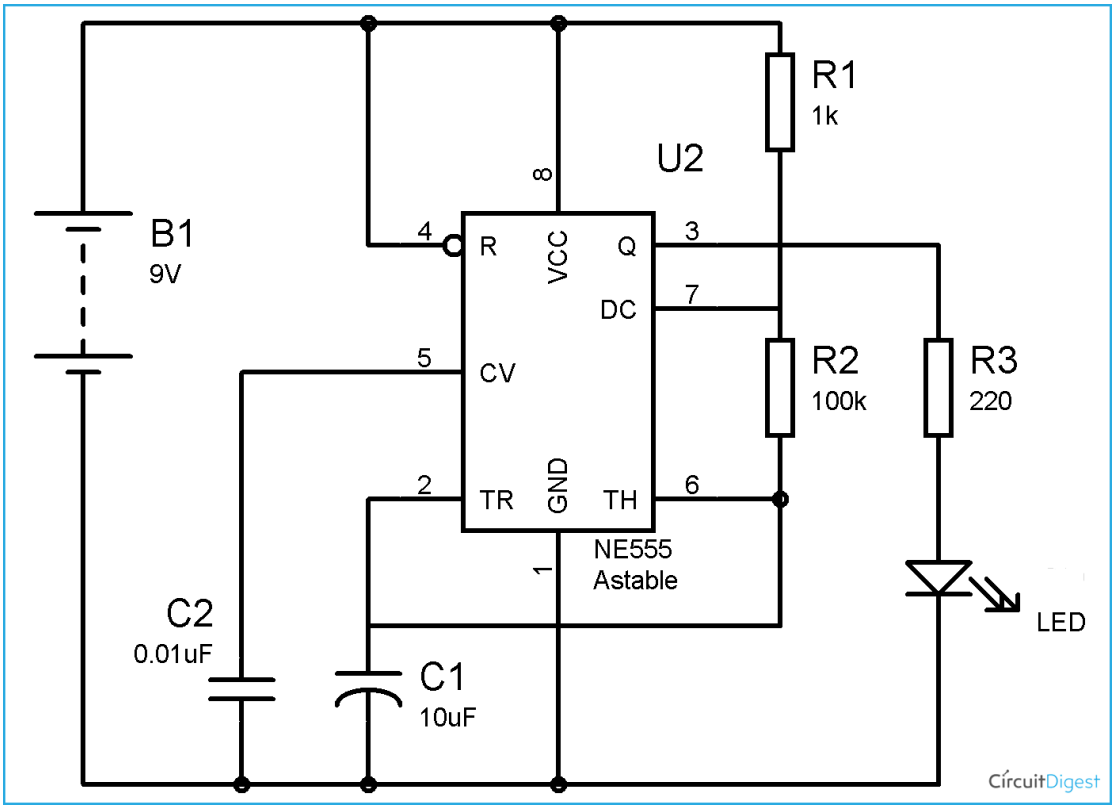
Road Branch	Red Signal	Yellow Signal	Green Signal
Road A	PB1+PB2+PB3+ PC1+PC2+PC3+ PD1+PD2= **A Road Red**	PD3+PA3= **A Road Yellow**	PA1+PA2
Road B	PC1+PC2+PC3+ PD1+PD2+PD3+ PA1+PA2 = **B Road Red**	PA3+PB3= **B Road Yellow**	PB1+PB2
Road C	PD1+PD2+PD3+ PA1+PA2+PA3+ PB1+PB2= **C Road Red**	PB3+PC3= **C Road Yellow**	PC1+PC2
Road D	PA1+PA2+PA3+ PB1+PB2+PB3+ PC1+PC2= **D Road Red**	PC3+PD3= **D Road Yellow**	PD1+PD2
Pedestrian IA	**A Road Red+ A Road Yellow**	PA2	PA1

Pedestrian IB	**B Road Red+ B Road Yellow**	PB2	PB1
Pedestrian IC	**C Road Red+ C Road Yellow**	PC2	PC1
Pedestrian ID	**D Road Red+ D Road Yellow**	PD2	PD1
Pedestrian IA/	PA1+PA2+PA3	PD3	**A Road Red**
Pedestrian IB/	PB1+PB2+PB3	PA3	**B Road Red**
Pedestrian IC/	PC1+PC2+PC3	PB3	**C Road Red**
Pedestrian ID/	PD1+PD2+PD3	PC3	**D Road Red**

Generation of PWM and Trigger Signals $P_{road\_name(i)}$

- **PWM generation by Astable operation of 555 timer**

  The PWM signal is generated by the circuit of the following figure.



For greater than 50% duty cycle, the formulae of Duty cycle and frequency are:

$$f = \frac{1.44}{(R_1+2R_2)C_1} \text{.....(i)}$$

$$D = \frac{(R_1+R_2)}{(R_1+2R_2)} \times 100\% \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\text{(ii)}$$

The Duty cycle is not important here (the reason behind it will is explained in the next section).

The period is adjusted to 4.5 second.

$C_1 = 1000\ uF$ (Practically, 800 uF value can be achieved)

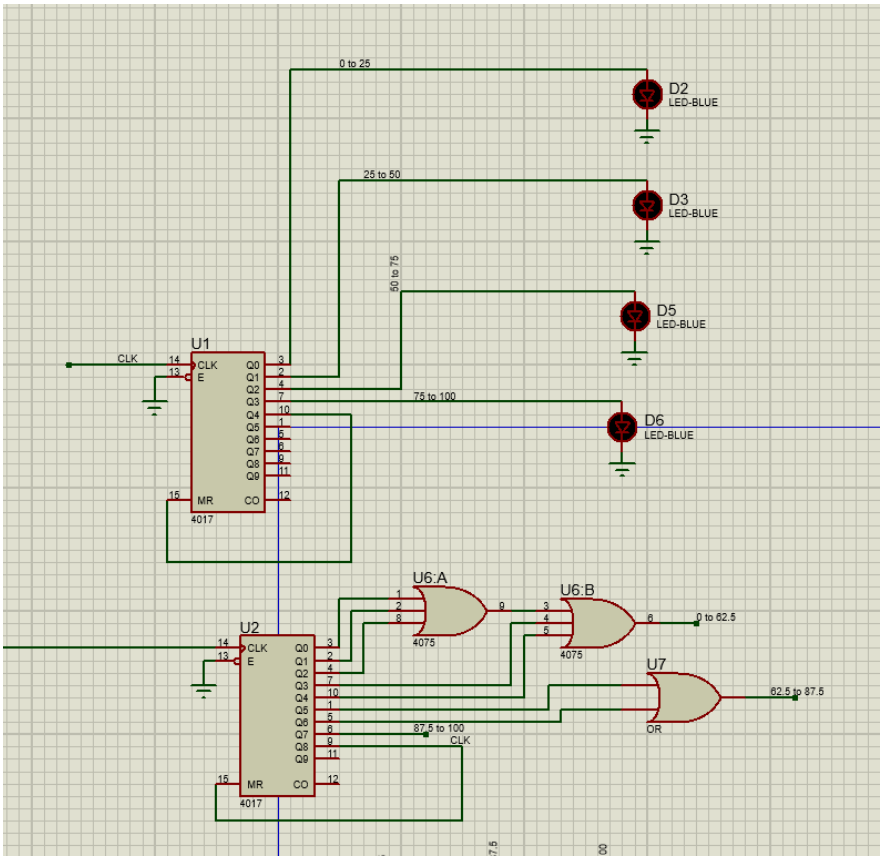
$R_1 = 2000\ ohm$

$R_2 = 3000\ ohm$

Evaluating equation (i) with practical values, the answer is **Period $T_{calculated}$= 4.44 sec.**

Placing an led from the output pin to the ground, and counting with stop-watche, the real value of a period is found to be **$T_{practical}$= 4.5 sec**.

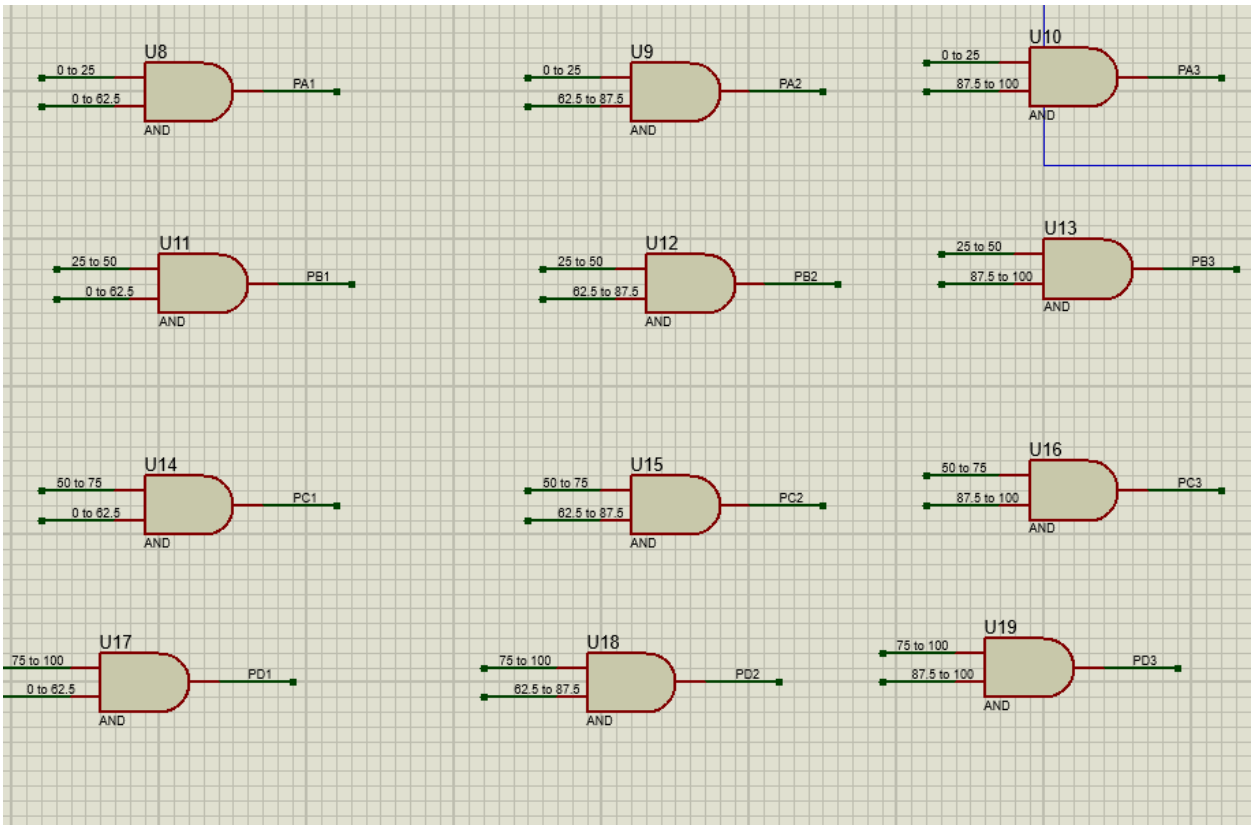
- **<u>Trigger Signal Generation by Ring counter (IC 4017)</u>**



Ring counter shifts the input pulses from output Q_0 to successive outputs with just a completion of a period of the PWM and resets at the pin with which the **Reset Pin 15** is connected to. **This is why the duty cycle is not important here.**

Pin 14 takes the **positive edge** of the clock signal as trigger.

In the above figure, the upper ring counter **U1** is used for activating each roads A, B, C, D, and the lower counter **U2** is used for each trigger. Most importantly, after a full set of triggers, the **trigger counter U2** resets, and at the same time, the **activating counter U1**changes its output signal.



Finally, using 7408 IC, trigger signals are generated.

These signals are combined according to the logic of table 2 .

System Performance

The traffic system is defined by **the percent running time of transports** and **the percent time of pedestrian road crossing.**

In terms of above parameters, the system performance can be evaluated from the Logic Table.

A) The transport of any road runs total $\frac{87.5\%}{400\%} \times 100\% = 21.875\%$

B) The Pedestrians have the **best and worst** efficiencies that can be calculated.
   - Best efficiency arises when a pedestrian comes from road IA, stops for a small time, and then crosses IA/. They have to wait only **13.5 second.** So, running efficiency is $\frac{144-13.5}{144} \times 100\% = 90.625\%$
   - Worst efficiency arises when a pedestrian comes from road IA/ as soon as the green light is on, stops for a long time, and then crosses IA. They have to wait **1 minute, 16.5 second.** So, running efficiency is $\frac{144-76.5}{144} \times 100\% = 46.875\%$