ITM UNIVERSITY
GWALIOR • MP • INDIA
"CELEBRATING DREAMS"

Roll No.....

2nd Midterm Examinations June 2022

(B.Tech.- CSE)

(Computer system Organisation)

(CSL0458)

Time 1:30 hrs **Max. Marks 30**

Note: Attempt all questions. All questions carry equal marks

Q.1	a	What do mean by handshaking? How data is transfer by source initiated data transfer using handshaking.	3
	b	How many chips of size 64X8 are required to design a memory of size 512x16.	3
		OR	
	a	What is associative memory? Explain the concept of match-logic for associative memories.	3
	b	What are the different modes of data transfer. How asynchronous data transfer handles the data transfer is a packet is to be sent over the channel?	3
Q.2		A Processor receives a signal on INTR input for reading the data from the keyboard. How this will be handled by the processor.	6
		OR	

Q.2 The logical address generated by a processor is of 32 bits and has to be mapped to 16 bit Physical address. What can be concluded about the size of the Primary and Secomdary memory of the machine.Data that can be stored in each memory location is of 1 byte. Compute the width of address and data bus for Logical and physicalmemory both. 6

Q.3 What is Virtual Memory? How it is implemented? What happens when the required page is not found in the memory? 6

OR

Q.3 All the intrerrupts coming to the system are to be processed but priority of each of them has to be considered and all must be processed serially with respesct to their priorities. What mechniasm does CPU uses to resolve this? 6

Q.4 How many Registers does the Universal Asynchrounour Receiver Transmitter has? Explain function of each register. 6

OR

Q.4 Perform the Multiplication 7X3 using Booth's Multiplication Algorithm. 6

Q.5 Design a memory of size 1K*16 using a RAM IC of 128*16. Draw the memory map and clearly connect all the components with CPU. 6

OR

Q.5 Design a 4x4 FIFO Buffer for Serial transmission of data from Imput to Output using SR Flip Flop. 6