BRAC UNIVERSITY

VLSI DESIGN

CSE460L (Summer 2023)

SECTION: 07

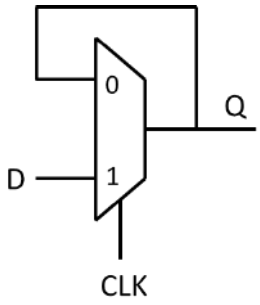
Time: 20 minutes

Name: **Student ID:**

Problem **[10]**

You have to design a D latch in DSCH2 using a 2 to 1 Multiplexer as shown in the following figure. D and Q are the latch's data input and output, respectively. The MUX's selector pin is a clock signal (CLK). You are not allowed to use gates (made using CMOS) other than **NAND and NOT** to implement the MUX.

[Hints: You may use the expression $\overline{\overline{(sA)}.\overline{(sB)}}$ *to implement the MUX using CMOS NAND and NOT logic only, with A and B being the two inputs to the MUX and s being the selection pin.]*



Note: You may use blocks/sub-circuits made using CMOS technology but **cannot use readily available logic gates.** In a timing diagram, show the simulated input and output waveforms. You may synchronize the inputs with clocks.

Name: Farhan Akbor Khan
ID: 20301230
Section: 07
Lab Assignment: 01
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