CSE460L: VLSI Design
Lab Assignment 2 (Summer 23)
Section: 07
Time: 30 mins

Problem:

Consider the boolean logic function below:

$$F = \overline{A + (\overline{B}.(C + \overline{D}))}$$

(a) Compile a **structural** Verilog Code for the function using Quartus.
(b) Prepare a vector waveform file (.vwf) using clock signals of appropriate periods required to produce all 16 combinations of the input variables and generate the simulation report.
(c) Compile a **behavioral** Verilog Code for the function using Quartus.
(d) Prepare a vector waveform file (.vwf) using clock signals of appropriate periods required to produce all 16 combinations of the input variables and generate the simulation report.
(e) Comment on whether both of the simulation reports are identical or not.

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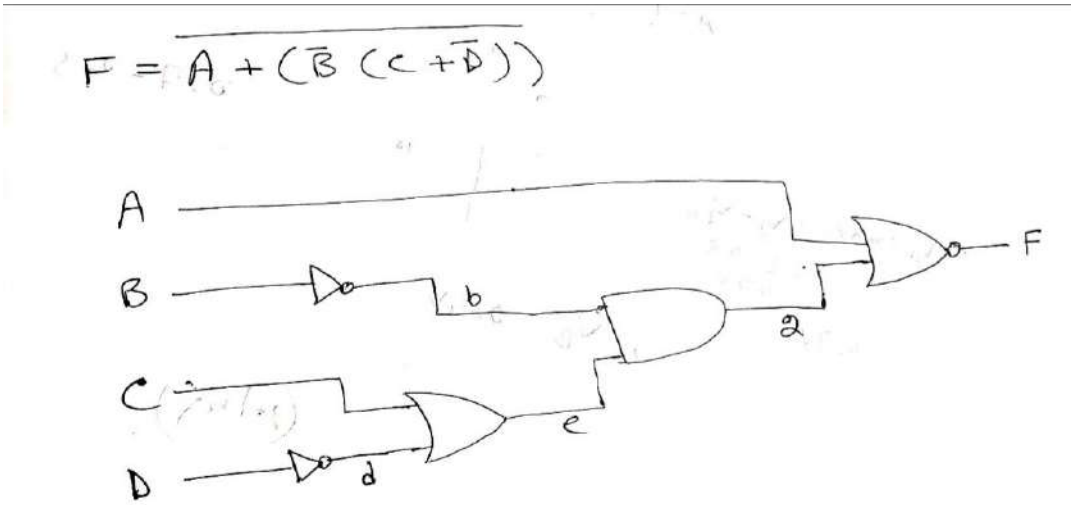
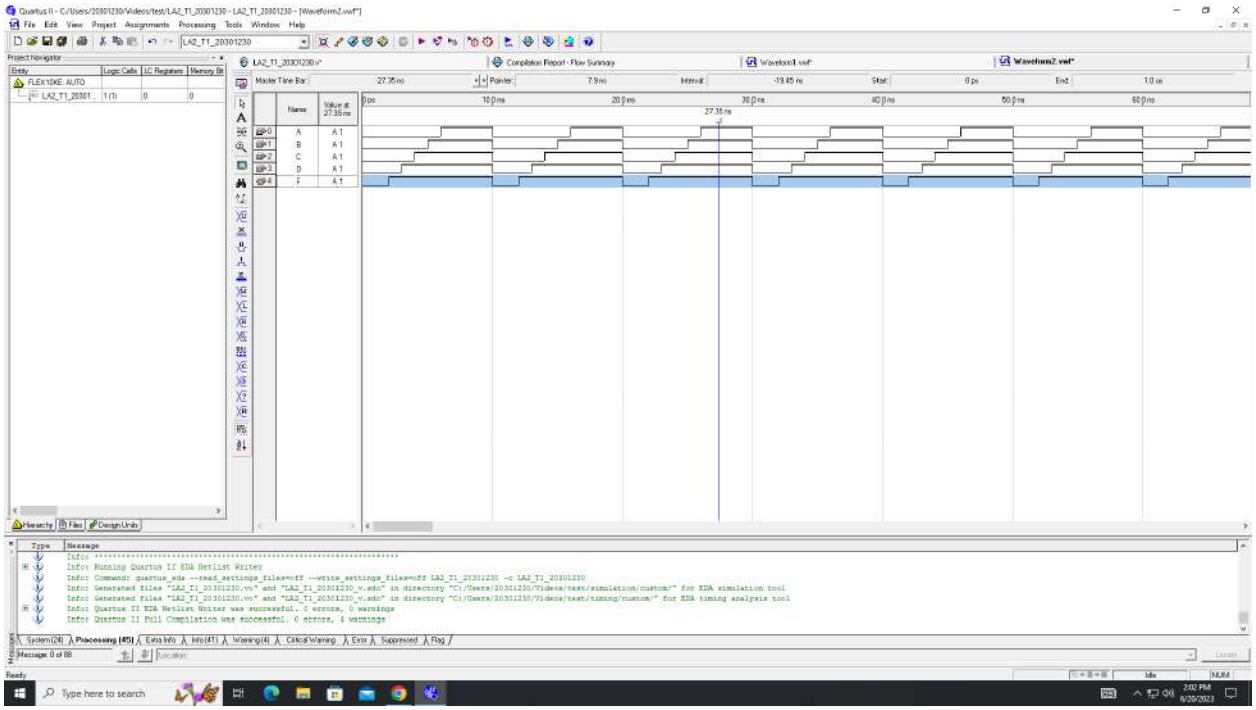


a)

```
module LA2_T1_20301230(A,B,C,D,F);
   input A,B,C,D;
   output F;
   wire b,d,e,g;
   not(b,B);
   and (g, b, e);
   or (e, C, d);
   not (d, D);
   nor (F, A,g);

endmodule
```

b)

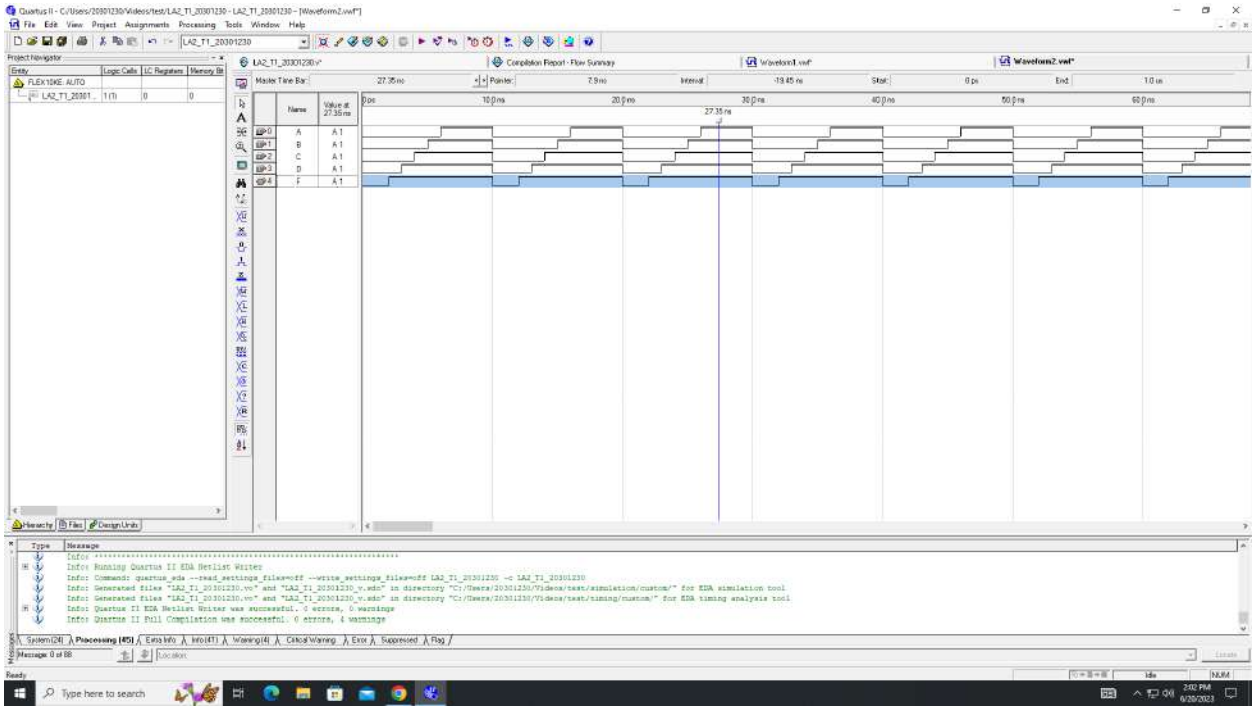


c)

```
module LA2_T1_20301230(A,B,C,D,F);
    input A,B,C,D;
    output F;
    wire B_sum;
    assign B_sum= C+ ~D;
    assign F= ~(A+(~(B) * B_sum));

endmodule
```

d)



e)

Both are the same if the clock cycles are the same.