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Section: 07

Lab03

CSE460

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Code:

```
module mux4to1_4bit_20301230 (a,b,c,d,sel,out);
    input [0:3]a,b,c,d;
    input [0:1]sel;
    output [0:3]out;

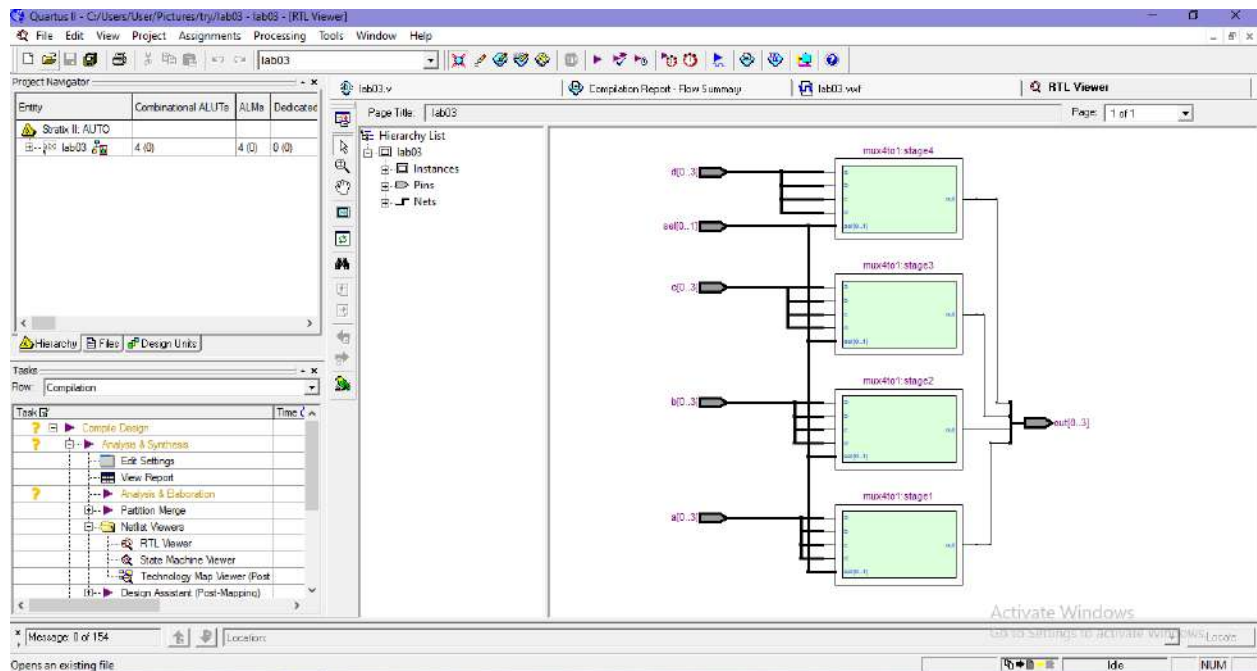
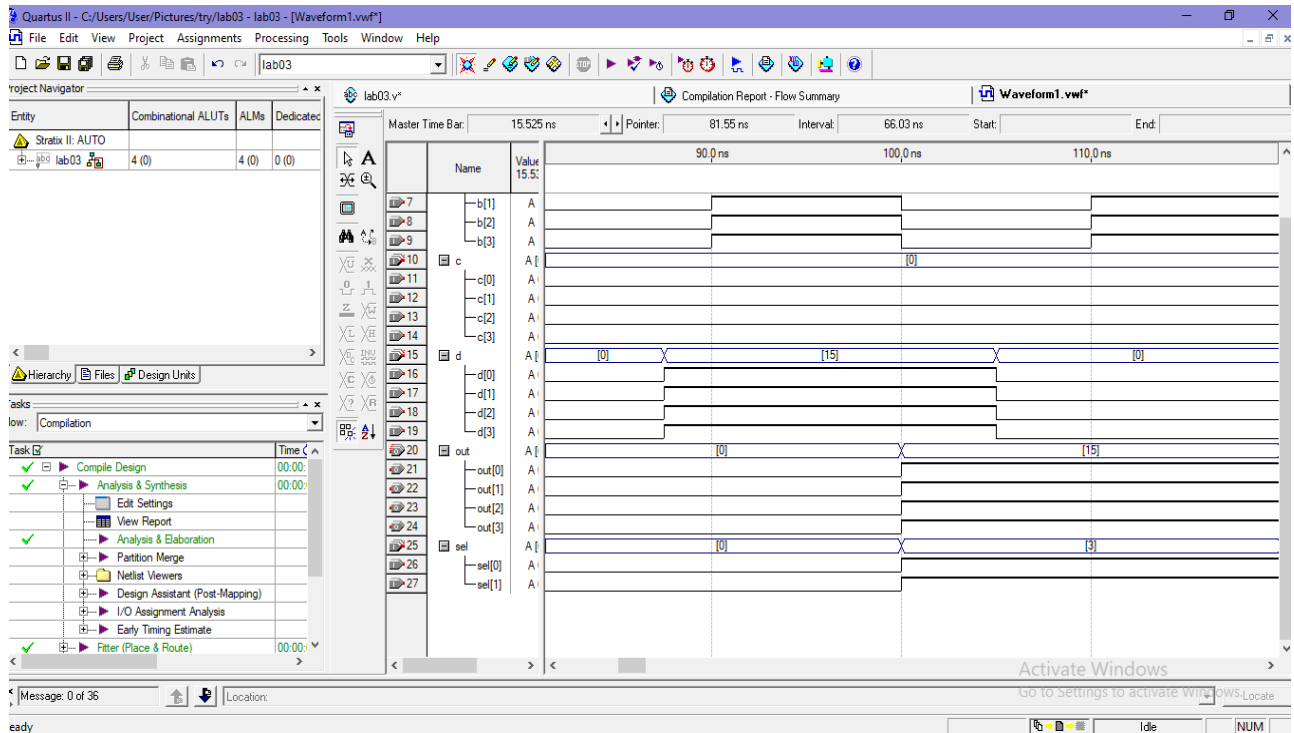
    mux4to1 stage1(a[0],a[1],a[2],a[3],sel,out[0]);
    mux4to1 stage2(b[0],b[1],b[2],b[3],sel,out[1]);
    mux4to1 stage3(c[0],c[1],c[2],c[3],sel,out[2]);
    mux4to1 stage4(d[0],d[1],d[2],d[3],sel,out[3]);

endmodule

module mux4to1 (a,b,c,d,sel,out);
    input a,b,c,d;
    input [0:1] sel;
    output out;

    assign out =(a^(~sel[0])^(~sel[1])) || (b^(sel[0])^(~sel[1])) || (c^(~sel[0])^(sel[1])) ||
    (d^(sel[0])^(sel[1]));

endmodule
```



Alter using Case:

Code:

```
module mux4to1_4bit_20301230(a,b,c,d,sel,out);
    input [3:0] a,b,c,d;
    input [1:0] sel;
    output reg [3:0] out;

    always @(a or b or c or d or sel)
    begin
        case(sel)
            2'b00: out <= a;
            2'b01: out <= b;
            2'b10: out <= c;
            2'b11: out <= d;
        endcase
    end
endmodule
```

