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Section: 07
Lab Test 04
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```
module farhan_20301230(w, clk, reset, z);
	input w, clk, reset;
	output reg z;

	reg current_state, next_state;

	parameter A = 1'b0, B = 1'b1;

	always @(posedge clk, posedge reset)
	begin
		if(reset == 1)
		begin
			current_state = A;
			next_state = A;
			z = 0;
		end
		else
			current_state = next_state;
			case(current_state)
				A:
				begin
					if(w == 0)
					begin
						next_state = A;
						z = 0;
					end
					else
					begin
						next_state = B;
						z = 1;
					end
				end
				B:
				begin
```

```
                    if(w == 0)
                    begin
                        next_state = B;
                        z = 1;
                    end
                    else
                    begin
                        next_state = B;
                        z = 0;
                    end
                end
            endcase
        end

    endmodule
```