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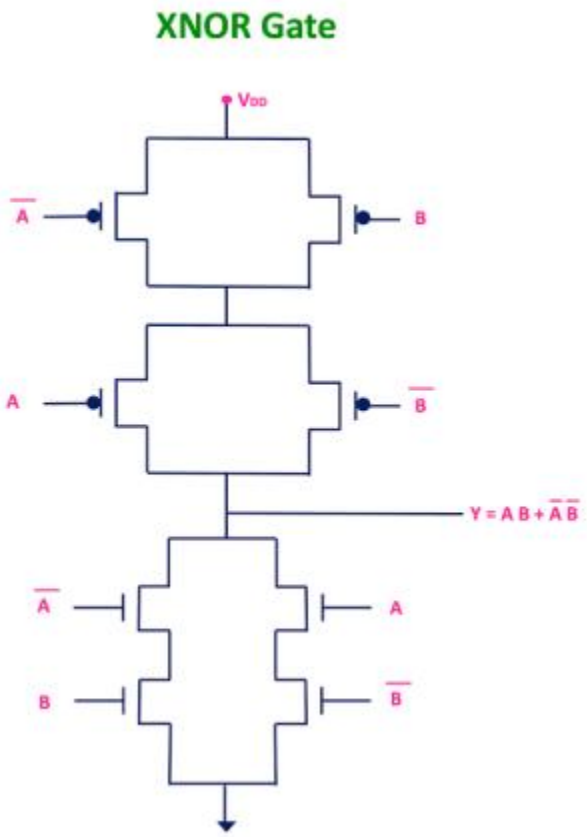
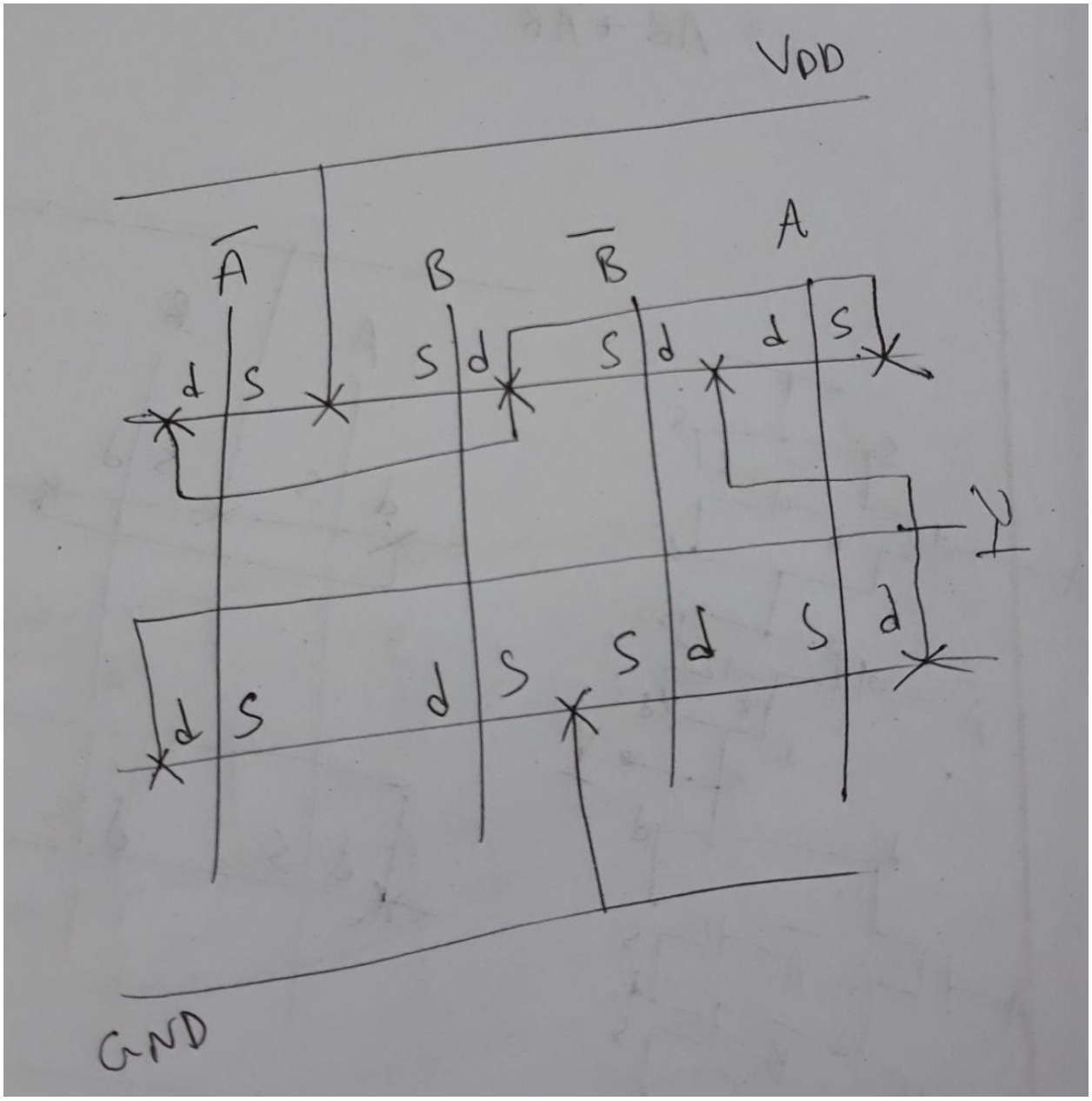
Section: 07
Lab Test - 06
CSE460 (Summer-23)
Date: 15 - 08 -2023

Question: Implement the layout of the following circuit using Microwind. You are supposed to design it manually (not using verilog) and must show that there are no DRC errors. Also, you have to show the waveforms of the circuit you've generated.

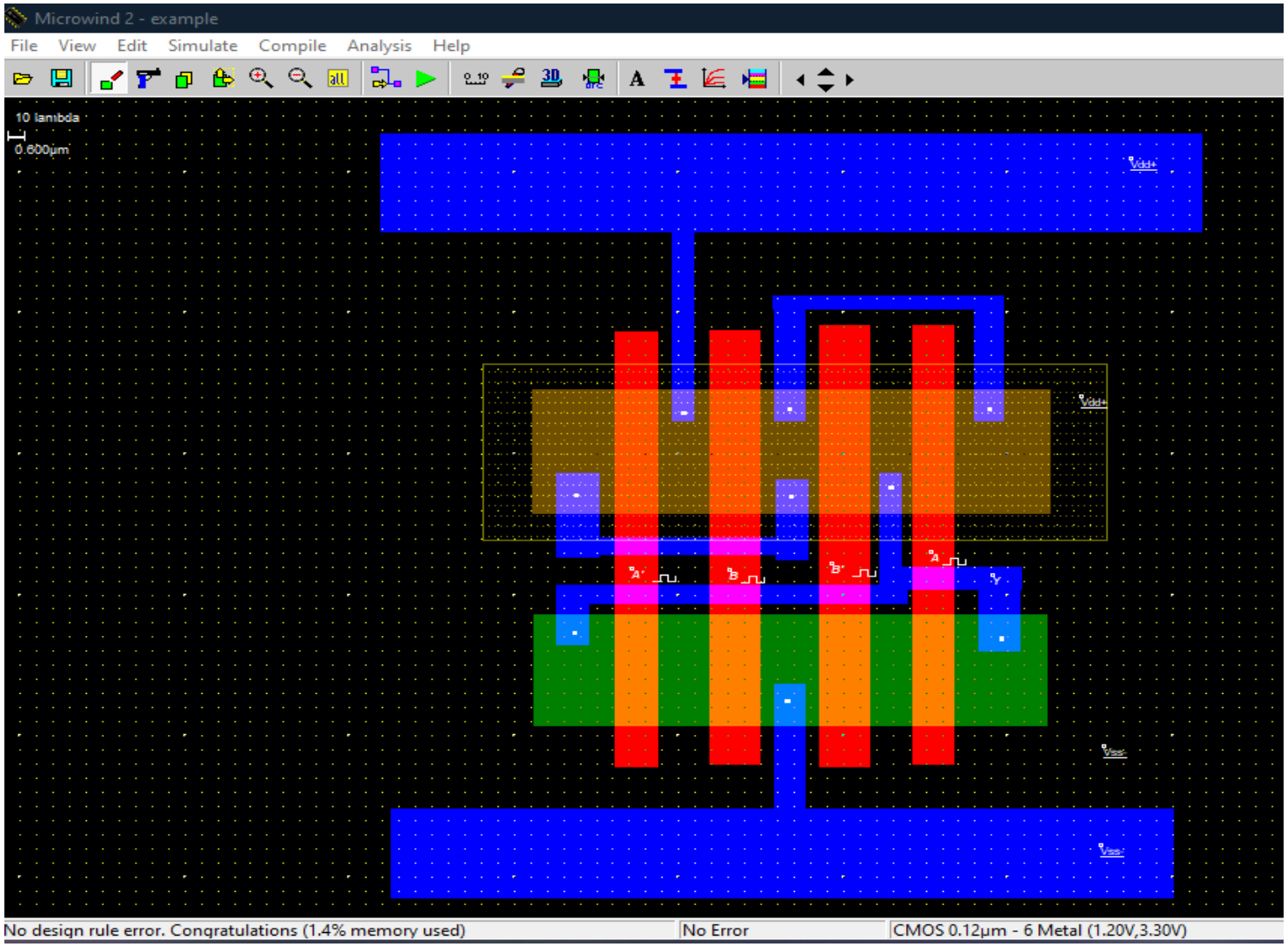


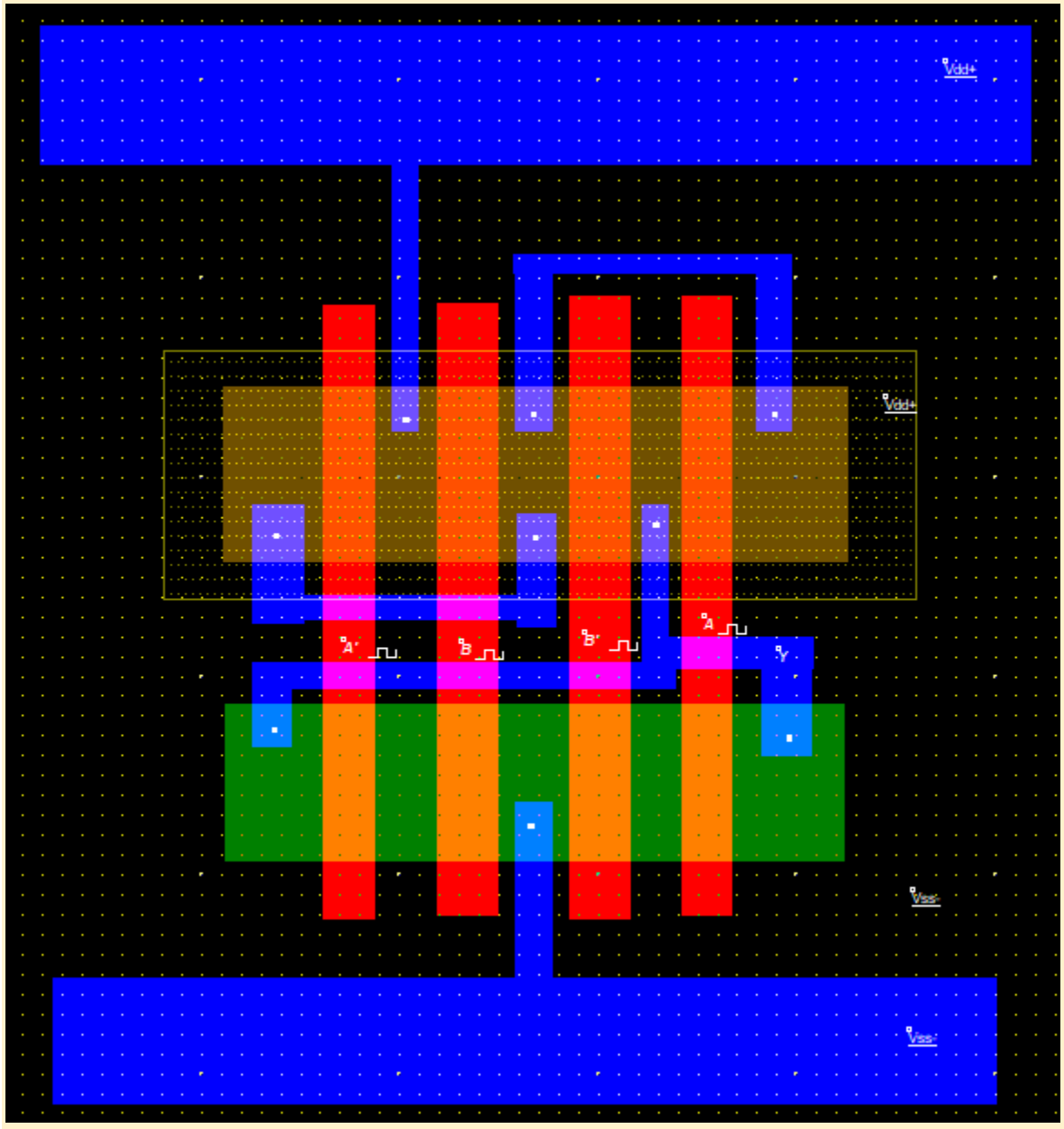
Answer:

Stick Diagram For above X-Nor Gate

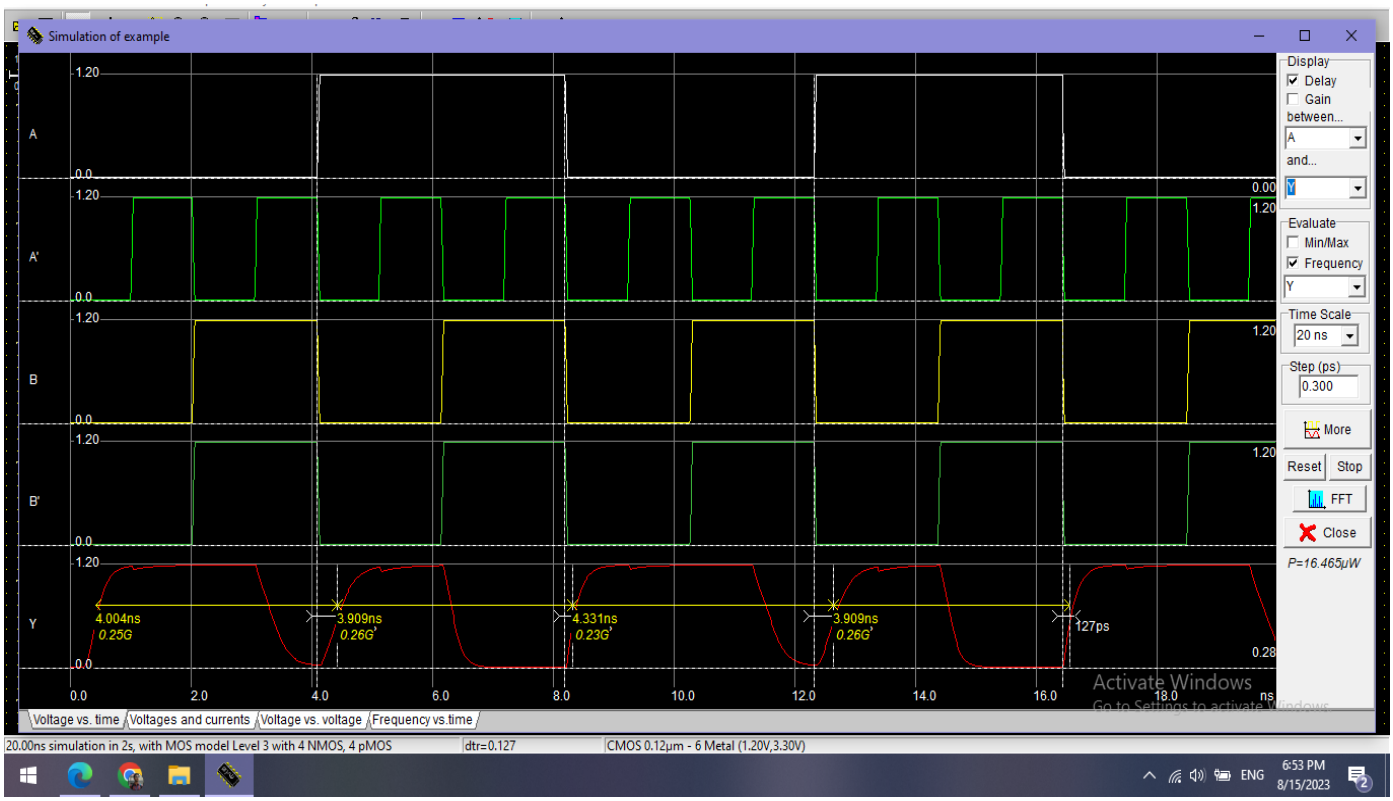


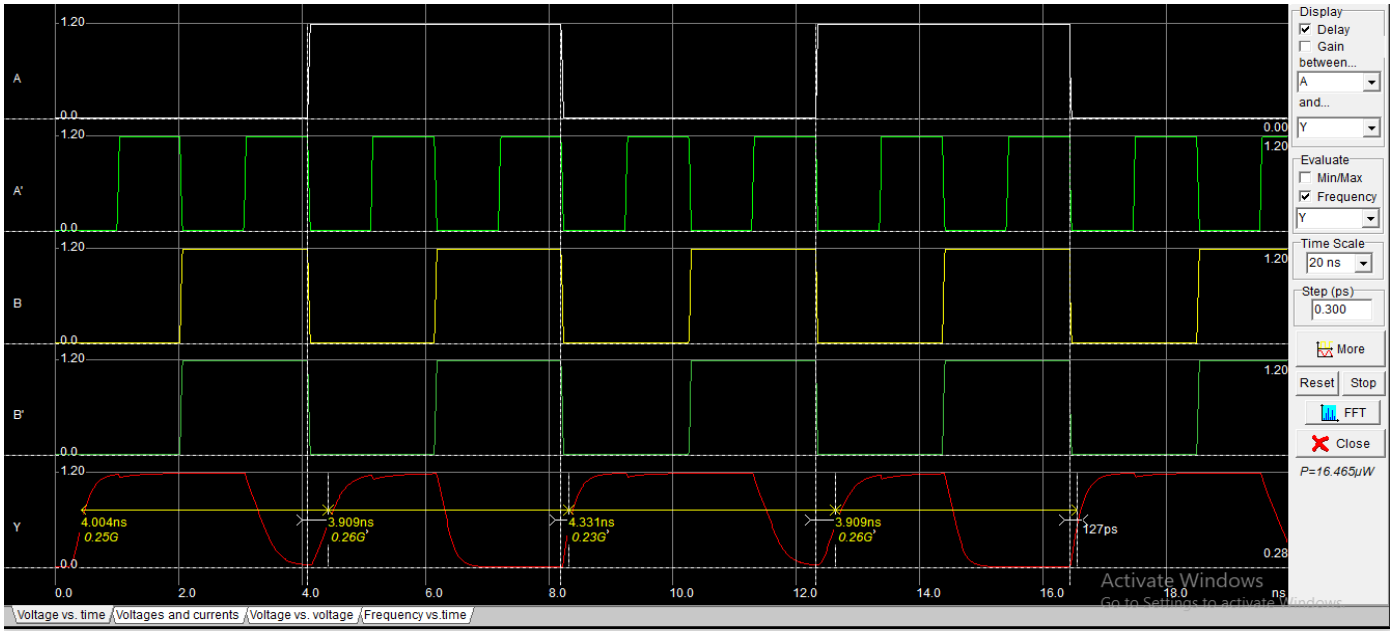
Layout


Microwind 2 - example
File View Edit Simulate Compile Analysis Help
10 lambda
0.600µm
Vdd
Vss
A
B
Y
No design rule error. Congratulations (1.4% memory used)
No Error
CMOS 0.12µm - 6 Metal (1.20V,3.30V)


Vdd+
Vdd+
A
B
B
A
Y
Vss-
Vss-

Waveform


Simulation of example
A
A'
B
B'
Y
4.004ns
0.25G
3.909ns
0.26G'
4.331ns
0.23G'
3.909ns
0.26G'
127ps
P=16.465µW
Voltage vs. time
Voltages and currents
Voltage vs. voltage
Frequency vs.time
20.00ns simulation in 2s, with MOS model Level 3 with 4 NMOS, 4 pMOS
dtr=0.127
CMOS 0.12µm - 6 Metal (1.20V,3.30V)
6:53 PM
8/15/2023


A
A'
B
B'
Y
4.004ns
0.25G
3.909ns
0.26G'
4.331ns
0.23G'
3.909ns
0.26G'
127ps
P=16.465µW
Voltage vs. time
Voltages and currents
Voltage vs. voltage
Frequency vs.time