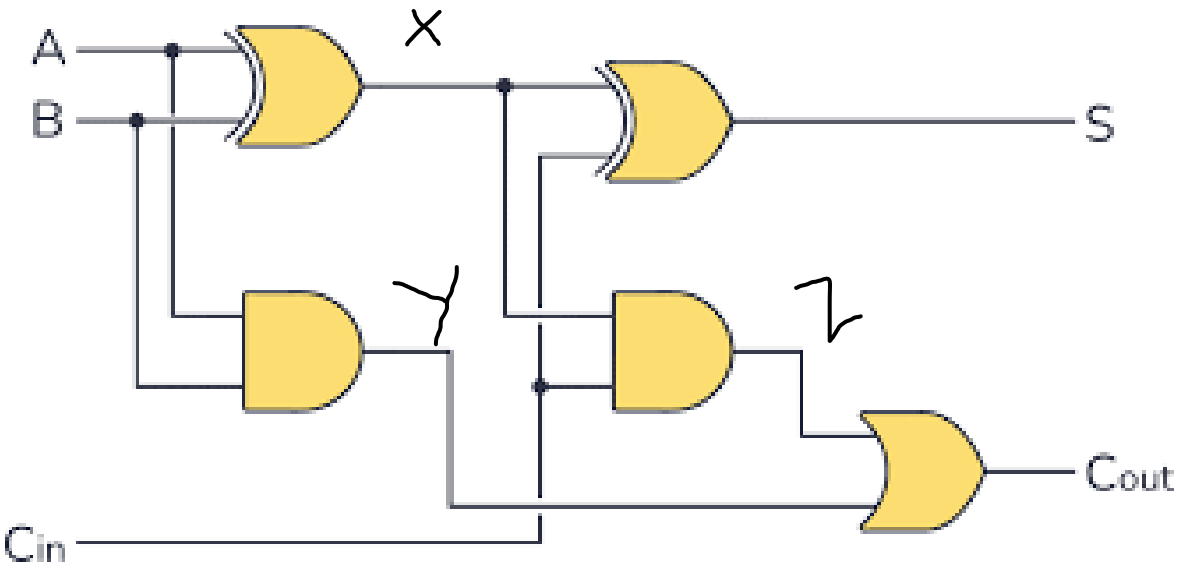
Full_Adder

Introduction:

Full Adder is the adder that adds three inputs and produces two outputs. The first two inputs are A and B and the third input is an input carry as C-IN. The output carry is designated as C-OUT and the normal output is designated as S which is SUM. In the following diagram we implement the full adder with the help of two half adders.

Circuit:

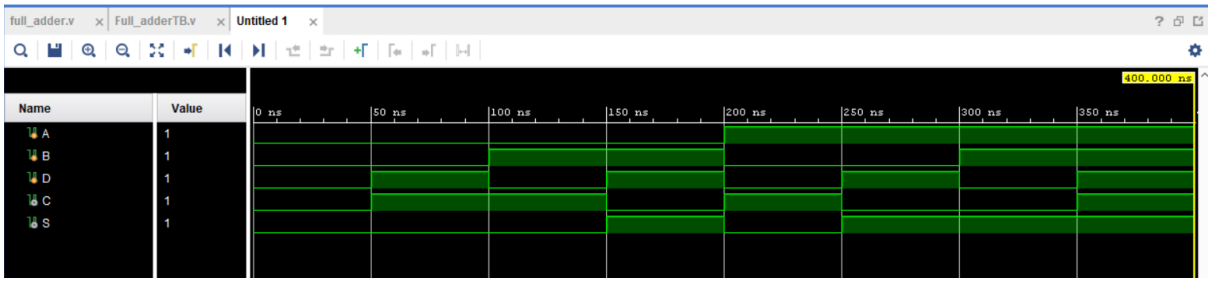


Code:

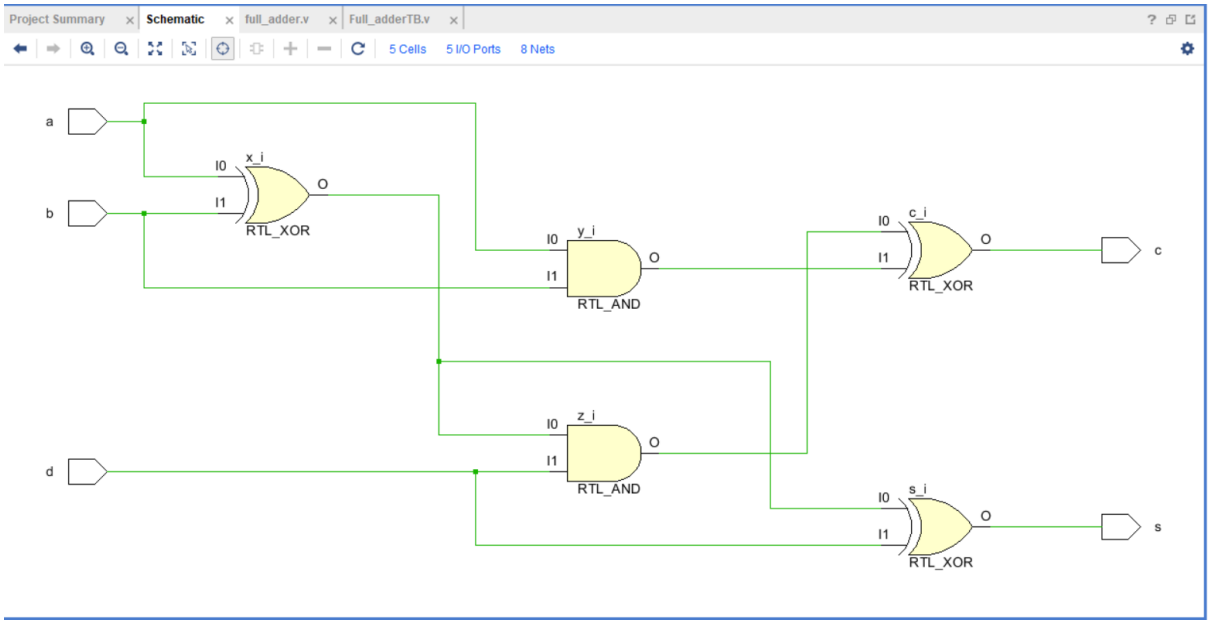
Full _adder.V	Testbench

module Full_adder(a,b,d,s,c);
input a,b,d;
output s,c;
wire x,y,z;
xor (x,a,b);
xor (s,x,d);
and (y,a,b);
and (z,x,d);
xor(c,z,y);
endmodule
	module Full_adderTB();
	reg A,B,D;
	wire C,S;
	Full_adder A1(A,B,D,C,S);
	initial
	begin
	A=0; B=0;D=0;
	#50
	A=0;B=0;D=1;
	#50
	A=0;B=1;D=0;
	#50
	A=0;B=1;D=1;
	#50
	A=1;B=0;D=0;
	#50
	A=1;B=0;D=1;
	#50
	A=1;B=1;D=0;
	#50
	A=1;B=1;D=1;
	#50
	$finish;
	end
	initial
	begin
	$display("A, B, D, C, S");
	$monitor(A,"\t",B,"\t",D,"\t",C,"\t",S);
	end
	endmodule

Simulation:



Elaborate design:



TCL Console: