Half adder

introduction :

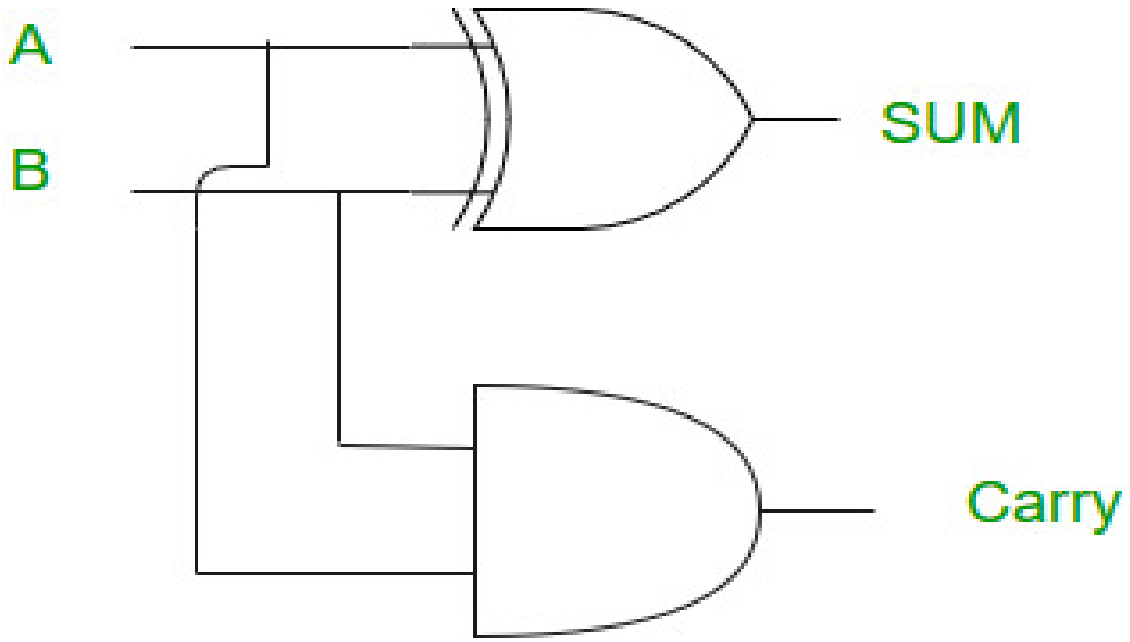
A half adder is a digital logic circuit that performs binary addition of two single-bit binary numbers. It has two inputs, A and B, and two outputs, SUM and CARRY.

Note. When we write system Verilog code we will add logic syntax after input and output the rest code will be same like Verilog.

i.e input logic a,b;

and output logic s ,c;

Circuit:

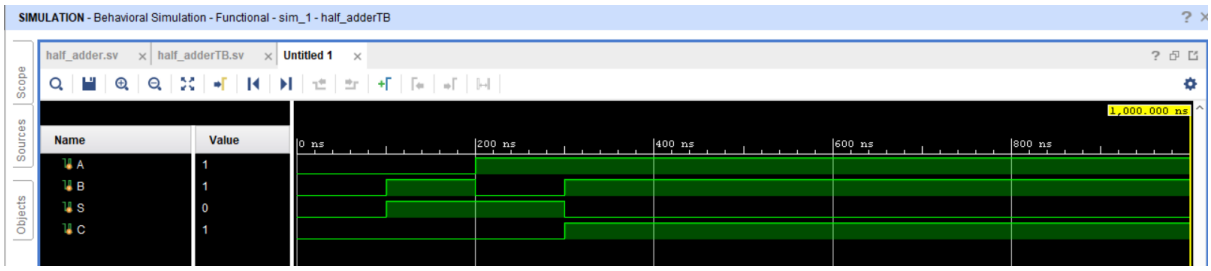


Code:

Half_adder.v	Testbench

module Half_adder(a,b,s,c);
input logic a,b;
output logic s,c;
and(c,a,b);
xor(s,a,b);
endmodule
	module half_adderTB();
	logic A,B;
	logic S,C;
	Half_adder H1(A,B,S,C);
	initial
	begin
	A=0;B=0;
	#100
	A=0;B=1;
	#100
	A=1;B=0;
	#100
	A=1;B=1;
	end
	endmodule

Simulation:



Elaborate design: