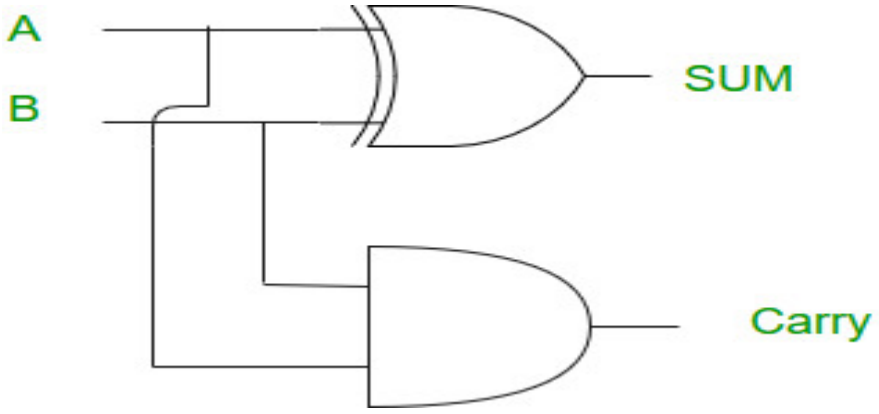
Half Adder

Introduction:

A half adder is a digital logic circuit that performs binary addition of two single-bit binary numbers. It has two inputs, A and B, and two outputs, SUM and CARRY. The SUM output is the least significant bit (LSB) of the result, while the CARRY output is the most significant bit (MSB) of the result, indicating whether there was a carry-over from the addition of the two inputs. The half adder can be implemented using basic gates such as XOR and AND gates.

Circuit:

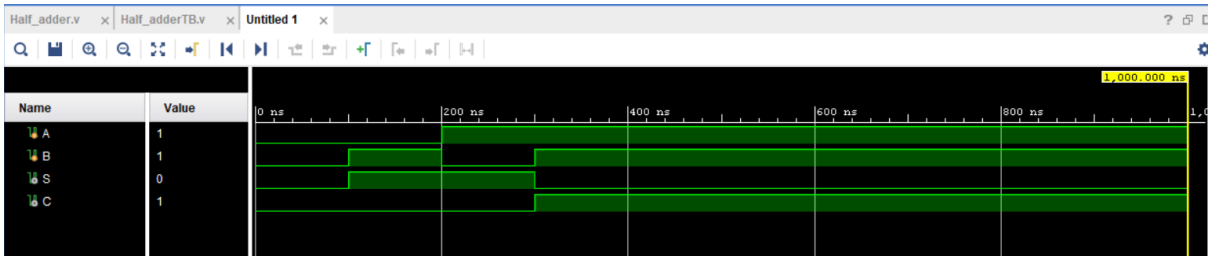


Code:

Half_adder.V	Testbench

module Half_adder(a,b,s,c);
input a,b;
output s,c;
and(c,a,b);
xor(s,a,b);
endmodule
	module Half_adderTB();
	reg A,B;
	wire S,C;
	Half_adder A3(.a(A),.b(B),.s(S),.c(C));
	initial
	begin
	A=0;B=0;
	#100
	A=0;B=1;
	#100
	A=1;B=0;
	#100
	A=1;B=1;
	end
	endmodule

Simulation:



Elaborate design: