Dept. of Computer Science &Engineering

Course Code: CSE-2324

Course Title : Digital Logic Design Lab

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Submitted to:

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SUBMISSION: *31-10-21*

Experiment No: 09

Experiment Name: Investigation of j-k flip-flop

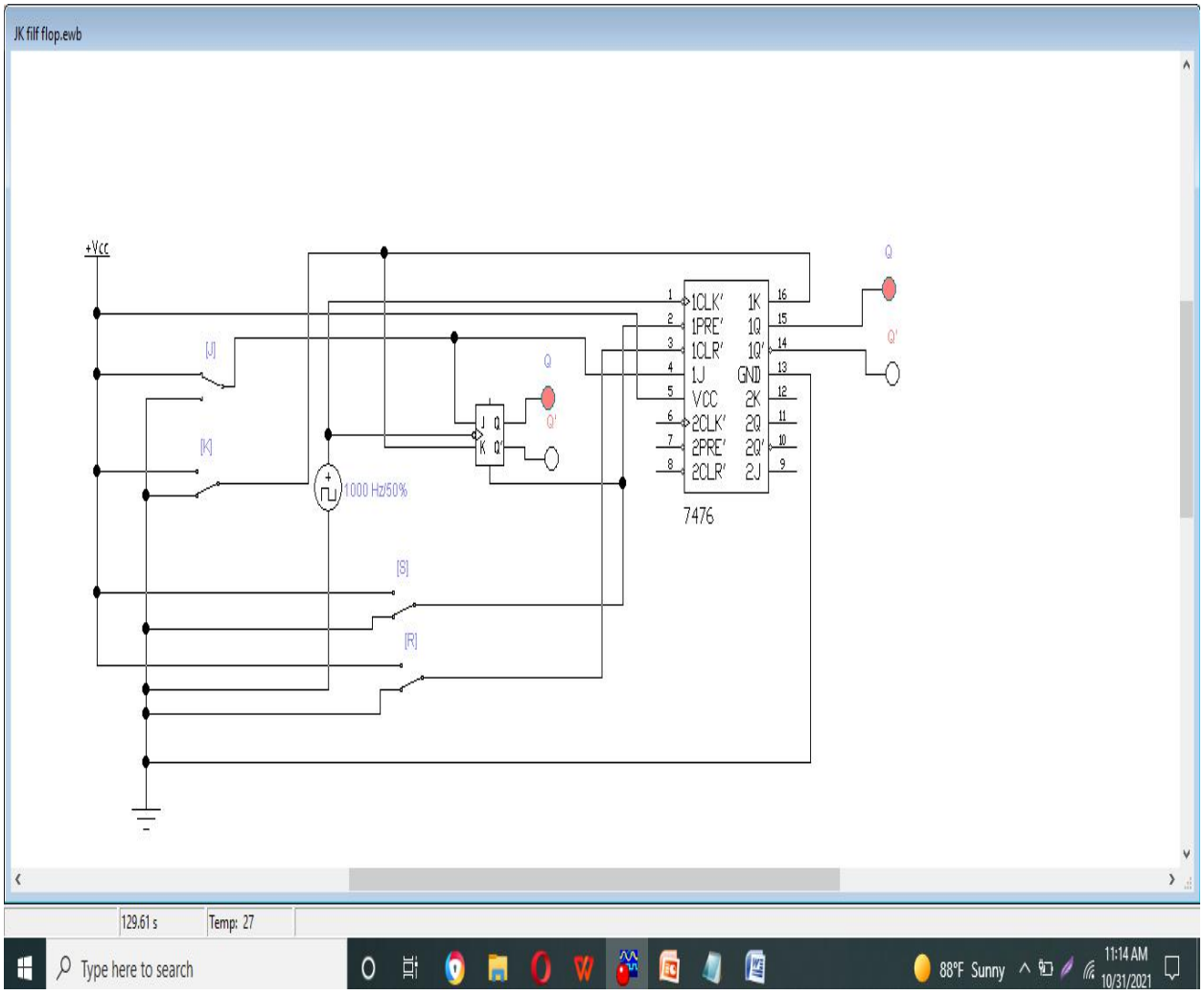
Required tools:

- IC 7476
- Wires
- LED
- Electronic Workbench Software

Turth Table:

Clock	J	K	Q	Q’	State
1	0	0	Q	Q’	No change is state
1	0	1	0	1	Resets Q to 0
1	1	0	1	0	Sets Q to 1
1	1	1	-	-	Toggles

IC level diagram:



Result Discussion:

The JK flip flop was termed after his inventor jack Kilby which is available as IC packages. The JK flip flops work as storage devices, control circuits, and counters. These flip flops have complicated wiring

and can only be used when the clock is set at high to get it activated. Such flip flops are Bi stabled latch.

It contains J and K as two other inputs. The working is the same as those of the SR flip flops for achieving a toggling function. A HIGH input given to RESET will activate it and thus, it will be inactivated at low inputs

Any problem arises:

No.

What Have I learnt :

A J-K flip-flop is nothing more than an S-R flip-flop with an added layer of feedback. This feedback selectively enables one of the two set/reset inputs so that they cannot both carry an active single to the multivibrator circuit, thus eliminating the invalid condition.