Dept. of Computer Science &Engineering

Course Code: CSE-2324

Course Title : Digital Logic Design Lab

Submitted by:

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Semester: 3rd

Section: 3AF

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Submitted to:
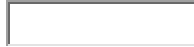
Mrs. Subrina Akter, Assistant Professor, Dept. of CSE,IIUC

SIGN: Farida Nusrat

SUBMISSION: 12-09-21

Experiment No: 04

Experiment Name : : Implementation of half adder circuit diagram for 2 inputs.

Required tools:

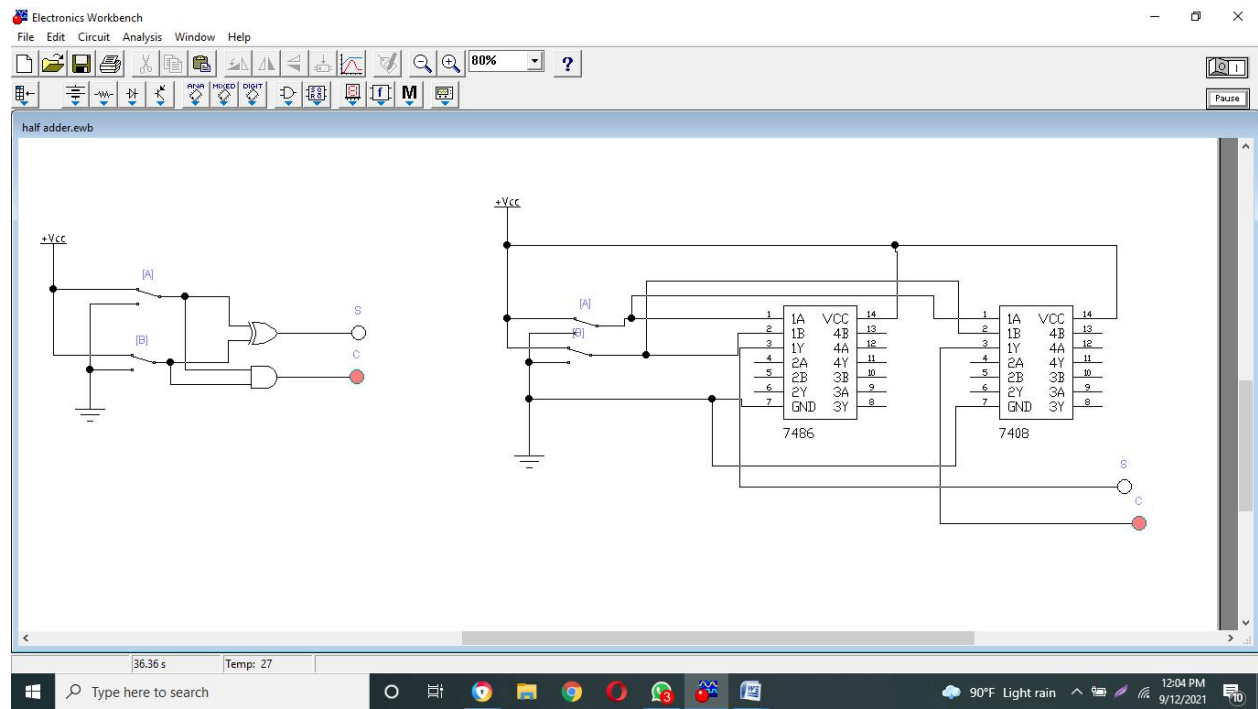➢ XOR 7486, AND 7408
➢ Wires
➢ LED
➢ Electronic Workbench Software
➢Switches
➢Voltage
➢Ground

Half Adder Turth Table:

A(Input)	B(Input)	S	C
0	0	1	1
0	1	1	0
1	0	0	1
1	1	0	0

Logic Circuit: IC level diagram:

Result Discussion:

The experiments are verified and it show the appropriate results for the fundamental logic circuit.

Any problem arises: No.

What Have I learnt:

I have learn some how simple inputs of ones and zeros can be used to store information for output.