# 2

# TRANSISTORS

## Bipolar Junction Transistors (BJT)

**npn transister**

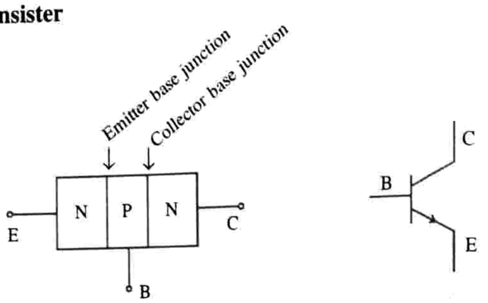



**Fig. 2.1**

**pnp transistor**

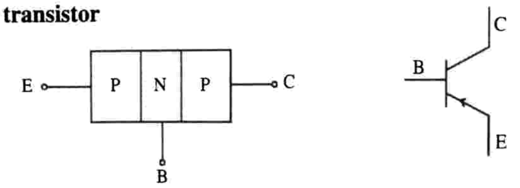



**Fig. 2.2**

*Note* : Emitter Base junction is always forward biased & collector base junction is always reverse biased.

### Different transistor amplifier configurations

Transistor can be connected in three configurations

(i) Common Base (CB) – Base is common for both input & output circuits.



(ii) Common Emitter (CE) – Emitter is common for both input & output circuits.

(iii) Common Collector (CC) – Collector is common for both input & output circuits.

### Common Base (CB) configuration

Here the Emitter base junction is forward biased by the battery $V_{EE}$ and the collector Base junction is reverse biased by the battery $V_{CC}$.

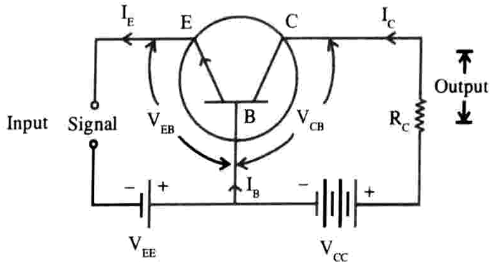



**Fig. 2.3**

### Current amplification factor ($\alpha$)

Ratio of change in collector current to the change in emitter current at constant collector base voltage $V_{CB}$ is called current amplification factor.

$$\alpha_{ac} = \left.\frac{\Delta I_C}{\Delta I_E}\right|_{V_{CB=Constant}} \qquad \alpha_{dc} = \frac{I_C}{I_E}$$

$I_C < I_E$ $\therefore$ $\alpha$ is always lesser than 1

$\alpha$ lies from 0.9 to 0.99

### Problems

1. *Define $\alpha$ of a transistor and show that it is always less than unity.* *(CU Nov. 18)*

*Ans*: $\alpha = \dfrac{\Delta I_C}{\Delta I_E}$, $\qquad I_C < I_E$, $\qquad \therefore\ \alpha$ is $< 1$

2. *What is amplification factor ?* *(CU Nov. 19)*

**Expression for collector current**

Collector base junction is reverse biased. Due to this a very small reverse saturation current $I_{CBO}$ (collector to base leakage current) flows across this junction.

$$\text{Total collector current } I_C = \alpha I_E + I_{leakage}$$

$$= \alpha I_E + I_{CBO} \quad (1)$$

By KCL,
$$I_E = I_C + I_B$$

Substituting in ①
$$I_C = \alpha(I_C + I_B) + I_{CBO}$$

$$I_C = \alpha I_C + \alpha I_B + I_{CBO}$$

$$I_C(1-\alpha) = \alpha I_B + I_{CBO}$$

$$I_C = \frac{\alpha}{1-\alpha} I_B + \frac{I_{CBO}}{1-\alpha} \quad (2)$$

Collector current can be controlled either by $I_E$ or by $I_B$

[see equations (1) & (2)]

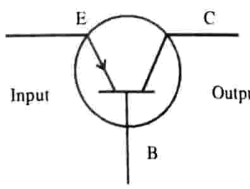
**Problem**

3. *In a transistor if* $I_C = 4.9\text{mA}$ *and* $I_E = 5\text{mA}$, *Find the value of* $\alpha$.

$$\alpha = \frac{I_C}{I_E} = \frac{4.9}{5} = 0.98$$

## Characteristics of Common Base Connection

**Common-Base circuit**




Common base configuration of pnp transistor

Fig. 2.4



Here the base terminal is common to both input and output terminals. The emitter terminal is taken as input and collector is taken as output terminal.

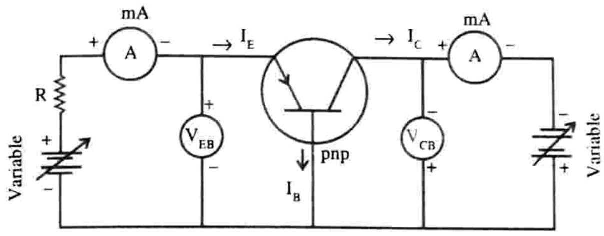



Fig. 2.5

**Input characteristics – ($V_{EB}$ versus $I_E$) and $V_{CB}$ = constant**

Output voltage $V_{CB}$ is kept constant. For each value of input voltage $V_{EB}$, corresponding value of $I_E$ is noted. Graph is ploted by taking $V_{EB}$ along x-axis and $I_E$ along y-axis.

The figure shows the input characteristics for different values of $V_{CB}$. In each case $V_{CB}$ is kept constant.

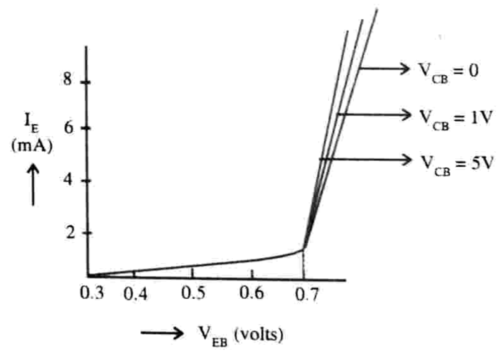



Fig. 2.6

Input resistance $R_i = \left(\dfrac{\Delta V_{EB}}{\Delta I_E}\right)_{V_{CB=Constant}}$

**Output characteristics – ($V_{CB}$ versus $I_C$) and $I_E$ = constant**

$I_E$ is kept constant. $V_{CB}$ is varied. Corresponding values of $I_C$ are noted.

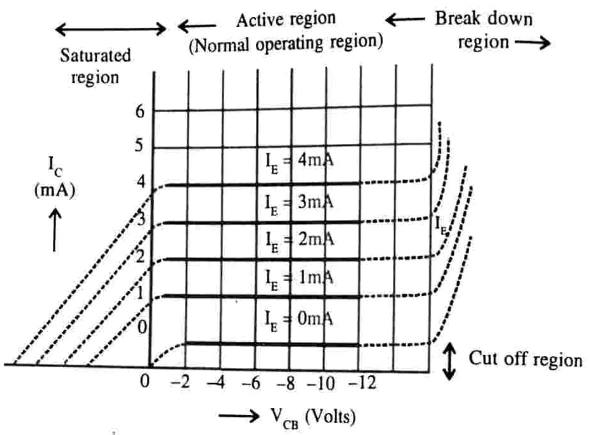



**Fig. 2.7**

Experiment is repeated for another value of $I_E$. Keeping $I_E$ constant (say 2mA), $V_{CB}$ is varied. Corresponding values of $I_C$ are noted.

Even when $V_{CB}$ is reduced to zero, $I_C$ flows. This is due to the barrier voltage existing at the collector base junction.

If we increase $V_{CB}$, breakdown occurs at collector-Base junction.

***Note :*** *[Transistor is called a* **current operating device**. *This is because input current $I_E$ controls output current $I_C$]*

Output resistance $R_0 = \left(\dfrac{\Delta V_{CB}}{\Delta I_C}\right)_{I_E=constant}$



**Saturation region** is the region located to the left of the line $V_{CB} = 0$ and above the output characteristics of emitter current $I_E = 0$. In this region, the collector current $I_C$ increases sharply for a small change in $V_{CB}$.

**Active region** is the region located to the right of the line $V_{CB} = 0$ and above the emitter current $I_E = 0$. Here collector current $I_C$ is constant ($I_C \approx I_E$).

**Properties of C-B configuration**

1. Voltage gain is very high
2. Current gain $\alpha = \dfrac{\Delta I_C}{\Delta I_E}$ is always less than 1.
3. Input resistance $R_i$ is low.
4. Output resistance $R_0$ is large.
5. Transistor in CB mode can be used as a constant current source.
6. Input and output voltages are in phase. So it can be used as a noninverting amplifier.

**Problems**

4. *For the CB circuit shown in fig.2.8 determine $I_C$ and $V_{CB}$. Transistor is made of Si.*

Ans: For Si transistor

$$V_{BE} = 0.7V$$

Apply KVL to mesh ①

$$I_E R_E = V_{EE} - V_{BE}$$

$$I_E = \frac{V_{EE} - V_{BE}}{R_E}$$

$$= \frac{6-0.7}{1.2\times10^3} = \frac{5.3}{1.2\times10^3} = 4.42\times10^{-3}A$$

$$I_C \approx I_E = \mathbf{4.42mA}$$

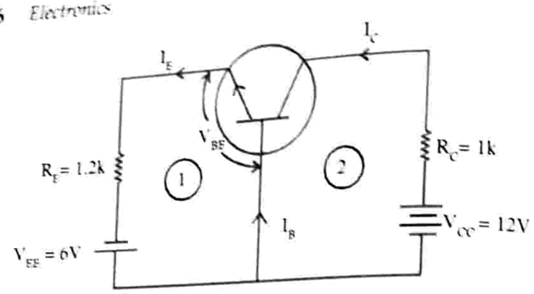



**Fig. 2.8**

Apply KVL to mesh ②

$$I_CR_C = V_{CC} - V_{CB}$$

$$V_{CB} = V_{CC} - I_CR_C$$

$$= 12 - 4.42 \times 10^{-3} \times 1 \times 10^{3}$$

$$= \mathbf{7.58}\ V.$$

5. *Draw the input and output characteristics of CB connection. What do you infer from these characteristics?* *(CU Nov. 19)*

## Common Emitter Configuration

**Base current amplification factor (β):**

The ratio of change in collector current ($\Delta I_C$) to the change in base current ($\Delta I_B$) is called base current amplification factor.

$$\beta = \frac{\Delta I_C}{\Delta I_B}$$



## Common Emitter (CE) Characteristics

**CE circuit**

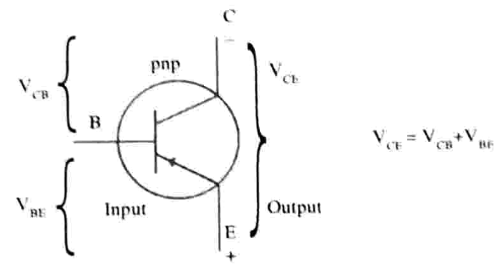



**Fig. 2.9**

Here the emitter terminal is common to both input as well as output. The base terminal is taken as input and collector terminal as output.

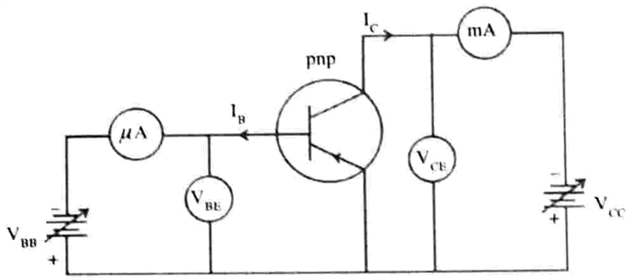



**Fig. 2.10**

**Input characteristics – ($V_{BE}$ Versus $I_B$) and $V_{CE}$ = constant**

$V_{CE}$ is kept constant. $V_{BE}$ is set and corresponding $I_B$ levels are noted. $V_{BE}$ is taken along X-axis and $I_B$ is taken along Y-axis.

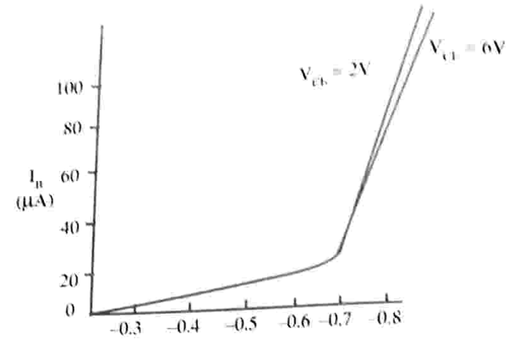



Fig. 2.11

$$\text{Input resistance, } R_i = \left[\frac{\Delta V_{BE}}{\Delta I_B}\right]_{V_{CE}=\text{constant}}$$

**Output characteristics – ($V_{CE}$ versus $I_C$) and $I_B$ = constant**

The output characteristics are drawn by noting output voltage $V_{CE}$ and the collector current $I_C$ keeping base current $I_B$ constant.

In active region, collector junction is reverse biased and emitter junction is forward biased. In figure active region is the area to the right of ordinate $V_{CE}$ = a few tenths of volt and above $I_B = 0$.

When $V_{CE}$ exceeds 0.7 V, the base-collector junction becomes reverse biased and the transistor goes into the active region. $I_C$ increases very slightly as $V_{CE}$ increases. This is due to widening of the base collector depletion region. This phenomenon is called **early effect**. In otherwords, the slope of the output characteristics is called the early effect.



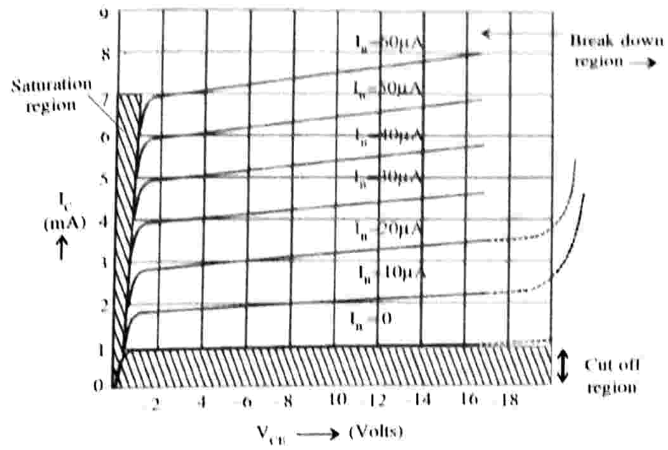



Fig. 2.12

When the characteristics are extended to the left of the current axis, they meet at a point on the horizontal scale.

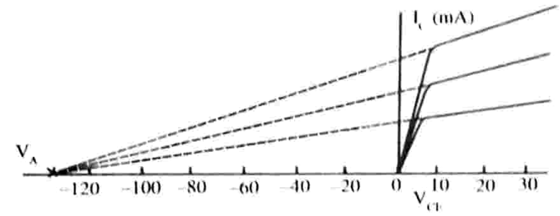



Fig. 2.13

The voltage at the point of intersection is around – 100 V to – 200 V. (in fig.2.13, – 120 V). This voltage $V_A$ is known as **early voltage**.

A small collector current exists even when $I_B = 0$. This is called **leakage current**.

The collector current is zero, when the base current is zero. Under this condition the transistor is in the **cut-off** state. The existing small collector current is called **collector cut off current**.

## Properties of CE configuration

1. Voltage and current gains in CE mode are greater than 1
2. The input resistance is high. Output is also high.
3. Transistor in CE mode can be used as a voltage or power amplifier.
4. Input and output voltages are out of phase by $180^{\circ}$. So it can be used as an inverting amplifier with $A_V > 1$.

### Problems

6. *A transistor has an emitter current of 12mA and a collector current of 11.95mA. Find its base current.*

   *Ans:* $I_E = I_B + I_C$

   $$I_B = I_E - I_C = 12 - 11.95 = 0.05\text{mA}$$

7. *Sketch the output characteristic of a common emitter configuration and discuss all the regions in the characteristic curve.* *(CU Nov, 20)*

8. *The most commonly used transistor arrangement is - configuration.* *(CU Nov. 20)*

   *Ans*: CE (Common Emitter)

## Relation between $\alpha$ and $\beta$ (CU Nov. 17)

$$I_E = I_B + I_C \quad \text{... (1)}$$

$$\alpha = \frac{I_C}{I_E}$$

$$I_C = \alpha I_E \quad \text{... (2)}$$

Substituting (1) in (2)

$$I_C = \alpha(I_B + I_C) = \alpha I_B + \alpha I_C$$



$$I_C - \alpha I_C = \alpha I_B$$

$$I_C(1-\alpha) = \alpha I_B$$

$$\frac{I_C}{I_B} = \frac{\alpha}{1-\alpha}$$

$$\beta = \frac{\alpha}{1-\alpha}$$

### Problems

9. *For a transistor the value of $\beta = 50$, then the value of $\alpha$ = ----* *(CU Nov. 17)*

   *Ans*: 0.98.

10. *For a transistor, the value of $\alpha$ is 0.9. Then the value of $\beta$ is –* *(CU Nov. 20)*

    *Ans*: 23

11. *A transistor has $\alpha = 0.97$ and $I_B = 200\ \mu A$. Calculate $I_C$, $I_E$ and $h_{FE}$ for the transistor.*

    (i) $I_C = \frac{\alpha I_B}{1-\alpha} = \frac{0.97 \times 200 \times 10^{-6}}{1-0.97} = \mathbf{6.47mA}$

    (ii) $I_C = \alpha I_E$

    $$I_E = \frac{I_C}{\alpha} = \frac{6.47 \times 10^{-3}}{0.97} = \mathbf{6.67mA}$$

    (iii) $h_{FE} = \beta = \frac{\alpha}{1-\alpha} = \frac{0.97}{1-0.97}$

    $$= \frac{0.97}{0.03} = \mathbf{32}.$$

12. *In a common base connection $\alpha = 0.95$. The voltage drop across $2K\Omega$ resistance which is connected in the collector is 2V. Find the base current* *(KU May 16)*

$$I_C = \frac{2V}{2K\Omega} = \frac{2}{2\times10^3} = 10^{-3}A = 1mA$$

$$\beta = \frac{\alpha}{1-\alpha} = \frac{0.95}{1-0.95} = \frac{0.95}{0.05} = 19$$

$$\beta = \frac{I_C}{I_B}$$

$$I_B = \frac{I_C}{\beta} = \frac{1\times10^{-3}}{19} = \mathbf{0.053\times10^{-3}A}$$

13. *A transistor has measured currents of $I_C$ = 3mA and $I_E$ = 3.03 mA. Calculate the new current levels when the transistor is replaced with a device that has $\beta = 75$. Assume that $I_B$ remains constant.*

$$\alpha = \frac{I_C}{I_E} = \frac{3}{3.03} = 0.99$$

$$\beta = \frac{\alpha}{1-\alpha} = \frac{0.99}{1-0.99} = \frac{0.99}{0.01} = 99$$

$$\beta = \frac{I_C}{I_B}$$

$$I_B = \frac{I_C}{\beta} = \frac{3mA}{99} = 0.03\times10^{-3}$$

$$= 30\mu A$$

For new transistor

$$I_B = \frac{I_{C1}}{\beta_1}$$



$$30\times10^{-6} = \frac{I_{C_1}}{75}$$

$$I_{C1} = 2250\times10^{-6} = 2.25mA$$

$$\beta_1 = \frac{\alpha_1}{1-\alpha_1}$$

$$75 = \frac{\alpha_1}{1-\alpha_1}$$

$$75 - 75\alpha_1 = \alpha_1$$

$$76\alpha_1 = 75$$

$$\alpha_1 = \frac{75}{76} = 0.987$$

$$\alpha_1 = \frac{I_{C1}}{I_{E1}}$$

$$0.987 = \frac{2.25}{I_{E1}}$$

$$I_{E1} = \frac{2.25}{0.987} = \mathbf{2.28}mA$$

14. *Determine $\alpha$ and $I_B$ for a transistor that has $I_C = 2.5mA$ and $I_E = 2.55mA$. Calculate $\beta$ for the transistor.*

$$\alpha = \frac{I_C}{I_E} = \frac{2.5}{2.55} = 0.98$$

$$\beta = \frac{\alpha}{1-\alpha} = \frac{0.98}{1-0.98} = 49$$

$$\beta = \frac{I_C}{I_B}$$

$$I_B = \frac{I_C}{\beta} = \frac{2.5\times10^{-3}}{49} = 0.051\times10^{-3}\text{mA} = \mathbf{51\mu A}$$

15. *A given transistor has a current gain $\beta = 50$. In common-base configuration, find the theoretical a.c. collector current flows when ac current of 2mA flows through the emitter. The collector potential is kept constant.*

$$\alpha = \frac{\beta}{\beta+1} = \frac{50}{51} = 0.98$$

for ac $\alpha_{ac} = \frac{\Delta I_C}{\Delta I_e}$

$$\Delta I_C = \alpha \Delta I_e = 0.98\times2 = \mathbf{1.96}\text{mA}$$

16. *In a CE configuration, the collector supply voltage is 10V. The voltage drop across 500Ω connected in a collector circuit is 0.5 V. If $\alpha = 0.98$, find (i) the collector-emitter voltage and (ii) base current.*

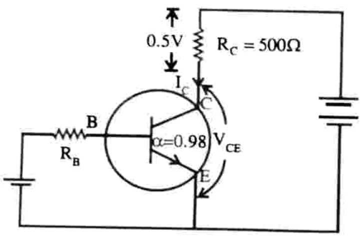



**Fig. 2.14**



(i) In CE configuration

$$V_{CC} = V_{R_C} + V_{CE}$$

$$V_{CE} = V_{CC} - V_{R_C} = 10 - 0.5 = \mathbf{9.5}\text{ V}$$

(ii) Voltage drop across $R_C = I_C R_C = 0.5$ V

$$I_C = \frac{0.5}{R_C} = \frac{0.5}{500} = 1\text{mA}$$

$$\beta = \frac{\alpha}{1-\alpha} = \frac{0.98}{1-0.98} = 49$$

$$I_B = \frac{I_C}{\beta} = \frac{1\text{mA}}{49} = \mathbf{0.0204}\text{mA}$$

17. *What will be the base current of a transistor of $\alpha = 0.99$ and $I_E = 8\text{mA}$.*

$$\alpha = \frac{I_C}{I_E}$$

$$I_C = \alpha I_E = 0.99\times8\times10^{-3} = 7.92\text{mA}$$

we have, $I_E = I_C + I_B$.

$$I_B = I_E - I_C = 8 - 7.92 = \mathbf{0.08}\text{mA}$$

18. *The emitter circuit is 2mA in a CB configuration of a transistor. The emitter circuit is open. The collector leakage current $I_{CBO}$ = 0.050 mA. If $\alpha = 0.98$, find the total collector current.*

$$I_C = \alpha I_E + I_{CBO}$$
$$= 0.98 \times 2 \times 10^{-3} + 0.050 \times 10^{-3}$$
$$= 1.96\text{ mA} + 0.050\text{ mA}$$
$$= \mathbf{2\text{ mA}}.$$

## Common Collector Configuration

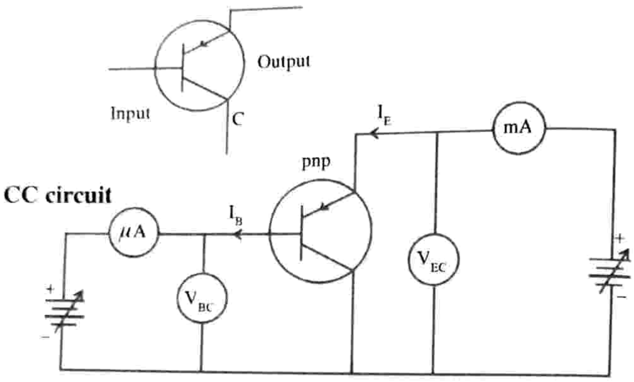



Fig. 2.15

### Input characteristics

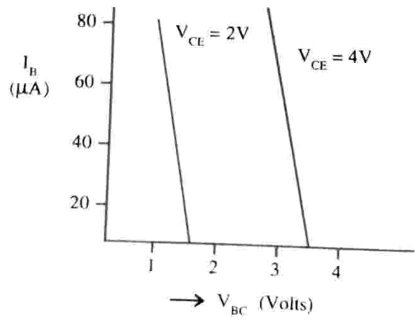



Fig. 2.16



### Output characteristics

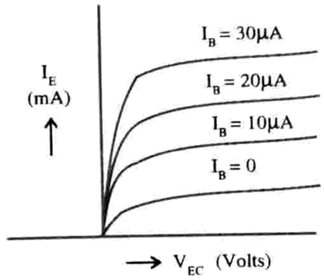



Fig. 2.17

***Note:*** Current amplification in CB, CE and CC are $\alpha$, $\beta$ and $\gamma$

$$\alpha = \left(\frac{\Delta I_C}{\Delta I_E}\right)_{V_{CB} = \text{constant}}$$

$$\beta = \left(\frac{\Delta I_C}{\Delta I_B}\right)_{V_{CE} = \text{constant}}$$

$$\gamma = \left(\frac{\Delta I_E}{\Delta I_B}\right)_{V_{CE} = \text{constant}}$$

***Note*** : Relation between leakage current in CB, $I_{CBO}$ and leakage current in CE, $I_{CEO}$ is

$$I_{CEO} = (\beta + 1) I_{CBO}$$

**Problems**

*19.* $V_{cc} = 10V$. *Transistor is connected in CE configuration. The voltage drop across* $500\Omega$ *connected in collector circuit is 0.6V. If* $\alpha = 0.98$, *find the collector-emitter voltage and base current.*

*Ans :*

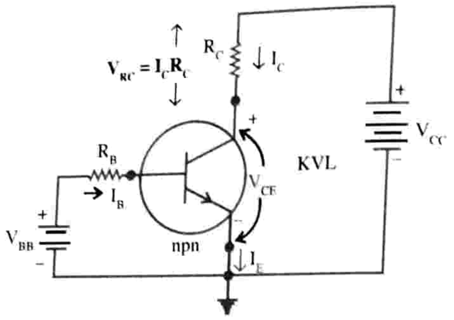



**Fig. 2.18**

In output circuit using KVL

$$I_C R_C = -V_{CE} + V_{CC}$$

$$V_{CE} = V_{CC} - I_C R_C \qquad \because V_{RC} = I_C R_C = 0.6V$$

$$= 10 - 0.6$$

$$= \mathbf{9.4}V$$

$$I_C R_C = 0.6$$

$$I_C \times 500 = 0.6$$

$$I_C = \frac{0.6}{500} = 1.2 \text{ mA}$$

$$\beta = \frac{\alpha}{1-\alpha} = \frac{0.98}{1-0.98} = 49$$

$$\beta = \frac{I_C}{I_B}$$

$$I_B = \frac{I_C}{\beta} = \frac{1.2\times10^{-3}}{49} = \mathbf{0.0245}\text{mA}$$



20. *In a transistor CE configuration, $V_{CC} = 12V$. Zero signal collector current is 1mA. What is the operating point if $R_C = 5K\Omega$*

*Ans :*

$$I_C R_C = V_{CC} - V_{CE}$$

$$V_{CE} = V_{CC} - I_C R_C$$

$$= 12 - (1\times10^{-3})(5\times10^{3})$$

$$= 12 - 5 = 7V$$

$\therefore$ Operating point $(I_C, V_{CE})$ is **(1mA, 7V)**

21. *In a CB circuit, the emitter current is 1mA. The emitter circuit is open. The collector leakage current is $40\mu A$. Calculate the total collector current. $\alpha$ of the transistor = 0.98*

*Ans :* Considering the leakage current $I_{CBO}$

In CB, $$I_C = \alpha I_E + I_{CBO}$$

$$= 0.98\times1\times10^{-3} + 40\times10^{-6}$$

$$= 0.98\text{mA} + 40\mu A$$

$$= \mathbf{1.020}\,\text{mA}$$

22. *In CE circuit, the collector current increases from 4mA to 4.02mA when the collector emitter voltage changes by 1V. Find the output resistance.*

*Ans :* $$R_o = \left|\frac{\Delta V_{CE}}{\Delta I_C}\right|_{I_B = \text{constant}}$$

$$= \frac{1}{0.02\times10^{-3}} = \frac{1000}{0.02} = 50000\Omega$$

23. *The cut off current $I_{CBO}$ for a transistor is $15\mu A$ at room temperature. $\beta = 50$. Calculate the collector current when base current is 0.2mA.*

*Ans :* In CE,

$$I_C = \beta I_B + I_{CEO}$$

$$I_{CEO} = I_{CBO} + \beta I_{CBO}$$

$$I_C = \beta I_B + (\beta+1)I_{CBO}$$

$$= 50\times 0.2\times 10^{-3} + (50+1)15\times 10^{-6}$$

$$= 10\times 10^{-3} + 765\times 10^{-6}$$

$$= \mathbf{10.765}\,\text{mA}$$

*24. A transistor is connected in CE configuration in which collector supply is 10V and voltage drop across resistor* $R_C = 800\Omega$ *connected in the collector circuit is 0.5V. If* $\alpha = 0.98$, *determine a) collector – emitter voltage b) base current*

*Ans :*

$$I_C R_C = V_{CC} - V_{CE} \qquad V_{CC} = 10V$$

$$V_{CE} = V_{CC} - I_C R_C \qquad R_C = 800\Omega$$

$$= 10 - 0.5 = 9.5V \qquad I_C R_C = 0.5V$$

$$\beta = \frac{I_C}{I_B} = \frac{\alpha}{1-\alpha} \qquad \alpha = 0.98$$

$$\frac{I_C}{I_B} = \frac{\frac{0.5}{800}}{I_B} = \frac{0.98}{1-0.98} = \frac{0.98}{0.02}$$

$$I_B = \frac{0.02}{0.98}\times\frac{0.5}{800} = \frac{0.01}{784} \qquad \because\ I_C = \frac{0.5}{R_C} = \frac{0.5}{800}$$

$$= \mathbf{12\mu A}$$



## Comparison of transistor connections

**Table 2.1**

| Parameters | CB | CE | CC |
|---|---|---|---|
| $R_i$ (input resistance) | Low ($\approx 100\Omega$) | Low ($\approx 750\Omega$) | Very high ($\approx 750k\Omega$) |
| $R_o$(output resistance) | $\approx 450\,k\Omega$ | $\approx 45\,k\Omega$ | $\approx 50\Omega$ |
| $A_V$(Voltage gain) | $\approx 150$ | $\approx 500$ | $< 1$ |
| Applications | for HF | for AF | for impedance matching |
| $A_i$ (current gain) | < 1 | high | Appreciable |

*25. The collector leakage current in a transistor is 250 $\mu A$ in CE configuration. If the same transistor is connected in CB configuration, find out the value of leakage current. $\beta$ of the transistor is 100.*

*Ans :*

Leakage current in CE, $I_{CEO} = 250\,\mu A$

$$\beta = 100$$

$$I_{CEO} = (\beta+1)I_{CBO}$$

$$I_{CBO} = \frac{I_{CEO}}{\beta+1}$$

$$= \frac{250\times 10^{-6}}{100+1}$$

$$= 2.5\mu A.$$

***Note :*** $I_C = \beta I_B + I_{CEO}$

$$I_{CEO} = I_{CBO} + \beta I_{CBO} = (\beta+1)\,I_{CBO}$$

### Expression for voltage gain, Current gain and power gain of CE amplifier

**Voltage gain ($A_v$)**

It is the ratio of change in output voltage $(\Delta V_{CE})$ to the change in input voltage $(\Delta V_{BE})$

$$A_v = \frac{\Delta V_{CE}}{\Delta V_{BE}}$$

$$= \frac{\text{change in output current} \times \text{effective load } (R_{AC})}{\text{change in input current} \times \text{input resistance}}$$

$$= \frac{\Delta I_C \cdot R_{AC}}{\Delta I_B \times R_i}$$

where $R_{AC} = R_C // R_O$

$R_O$ = output resistance

$R_i$ = input resistance

$$= \frac{\Delta I_C}{\Delta I_B} \cdot \frac{R_{AC}}{R_i}$$

$$= \beta \cdot \frac{R_{AC}}{R_i}$$

For single stage amplifier, $R_{AC} = R_C$

For multistage $R_{AC} = \frac{R_C \times R_i}{R_C + R_i}$

**Current gain ($\beta$)**

It is the ratio of change in collector current $(\Delta I_C)$ to the change in base current $(\Delta I_B)$.

Current gain $\beta = \frac{\Delta I_C}{\Delta I_B}$

Input current becomes $\beta$ times in the collector circuit.

*Note* : If $\beta_1$ and $\beta_2$ are individual stage gain of a two stage transistor circuit, then overall gain is $\beta = \beta_1 \beta_2$.



**Power gain ($A_p$)**

It is the ratio of output signal power to the input signal power.

$$A_p = \frac{(\Delta I_C)^2 \times R_{AC}}{(\Delta I_B)^2 \times R_i}$$

$$= \left(\frac{\Delta I_C}{\Delta I_B}\right) \cdot \frac{\Delta I_C \times R_{AC}}{\Delta I_B \times R_i}$$

$A_p$ = current gain $(\beta) \times$ voltage gain.

### Cut off saturation points

Consider CE transistor circuit. Its output characteristics is as shown below.

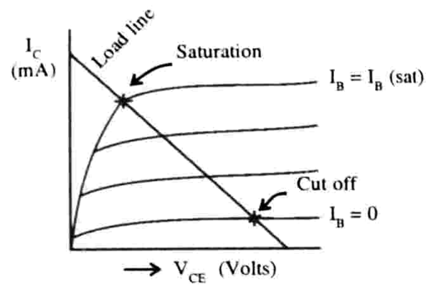



**Fig. 2.19**

**Cut off**

The point where the dc load line intersects the $I_B$ = O curve.

Here small collector current exists.

At cut off, the base - emitter junction no longer remains forward biased and normal transistor action is lost.

Emitter diode and collector diode are OFF

**Saturation**

The point where the load line intersects the $I_B = I_{B(sat)}$ curve.

Here Base current is maximum.

At saturation, collector base junction no longer remains reverse biased and normal transistor action is lost.

Emitter diode and collector diode are connected as show in fig.

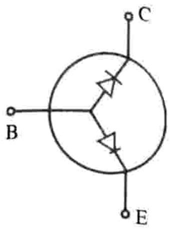


**Fig. 2.20**

### Active region

The region between cut off and saturation.
Here collector Base junction is reverse biased.
Base emitter junction is forward biased.
Transistor works normally.

## Transistor Biasing

The proper flow of zero signal collector current and the maintanance of proper collector – emitter voltage during the passage of signal is called transistor biasing.

*Purpose* : to keep the base – emitter junction properly forward biased and collector base junction properly reverse biased.

### Problem

*26. Mention the essentials of a biasing circuit.* *(CU Nov. 19)*

## Different types of biasing

### 1. Base resistor method (CU Nov. 17)

### Base bias (or) fixed current bias using npn transistor

Here base Current remains constant. It is determined by $V_{CC}$ (Supply voltage) and $R_B$ (Base resisitor). Since $V_{CC}$ and $R_B$ are constant quantities, $I_B$ remains same.

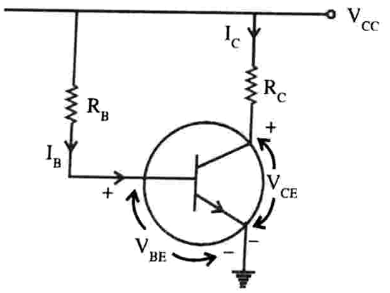


**Fig. 2.21**



Apply KVL to the input circuit

$$-I_B R_B = V_{BE} - V_{CC}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \qquad \text{... (1)}$$

Here $V_{BE}$ = 0.7 V for Si and 0.3 V for Ge transistors.

$$\beta = h_{FE} = \frac{I_C}{I_B}$$

$$I_C = h_{FE} I_B \qquad \text{... (2)}$$

Apply KVL to the output circuit

$$I_C R_C = -V_{CE} + V_{CC}$$

$$V_{CE} = V_{CC} - I_C R_C \qquad \text{... (3)}$$

Substituting (2) in (3)

$$V_{CE} = V_{CC} - (h_{FE} I_B) R_C$$

If supply voltage $V_{CC}$, $\beta$ and $R_C$ are known base bias circuit can be easily constructed by using (1)

### Problems

*27 $R_B = 470\,K\Omega$, $R_C = 2K\Omega$, $V_{CC} = 12$ V, $\beta$ or $h_{FE} = 100$.*
*Find the values of $I_B$, $I_C$ and $V_{CE}$. Given ($V_{BE} = 0.7$ V).*

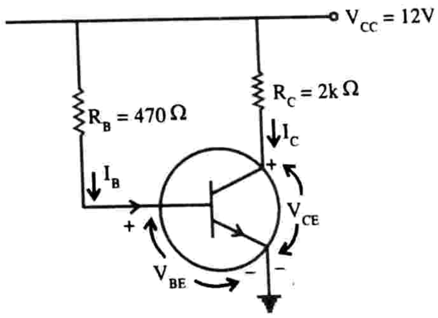


**Fig. 2.22**

Apply KVL to input

$$-I_B R_B = V_{BE} - V_{CC}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12 - 0.7}{470} = \frac{11.3}{470} = 24\mu A$$

$$h_{FE} = \beta = \frac{I_C}{I_B}$$

$$I_C = \beta \times I_B = 100 \times 24\mu A$$

$$= 2.4 \text{ mA}$$

Apply KVL to output

$$I_C R_C = -V_{CE} + V_{CC}$$

$$V_{CE} = V_{CC} - I_C R_C$$

$$= 12 \text{ V} - (2.4 \text{ mA} \times 2K\Omega)$$

$$= 12 - 4.8 = 7.2 \text{ V}$$

28. *From figure find* $I_{C_{saturation}}$, $I_C$, $V_C$, $V_E$ *and* $V_{CE}$

***Note***: Here emitter feedback is also included. $R_E$ provides a form of –ve feedback that can be used to stabilize DC operating point)

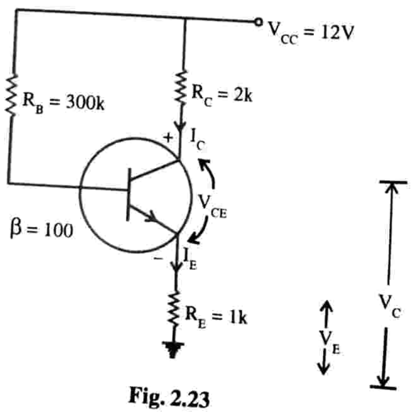



**Fig. 2.23**



$$I_{C_{saturation}} = \frac{V_{CC}}{R_E + R_C} = \frac{12}{1+2} = 4\text{mA}$$

$$\text{Actual } I_C = \frac{V_{CC}}{R_E + \frac{R_B}{\beta}} = \frac{12}{1 + \frac{300}{100}} = 3\text{mA}$$

Apply KVL to output circuit.

$$I_C R_C = V_{CC} - V_C$$

$$V_C = V_{CC} - I_C R_C = 12 - 3 \times 2 = 6\text{V}$$

$$V_E = I_E R_E \approx I_C R_E$$

$$= 3 \times 1 = 3\text{V}$$

$$V_{CE} = V_C - V_E = 6 - 3 = 3\text{V}$$

**Base bias using a pnp transistor**

Here polarities and directions of current are reversed compared to npn transistor base bias circuits.

**Base Bias circuit design**

Apply KVL to output circuit.

$$V_{CE} = V_{CC} - I_C R_C$$

$$R_C = \frac{V_{CC} - V_{CE}}{I_C} \quad \dots (1)$$

Apply KVL to input circuit.

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} \quad \dots (2)$$

$$\text{Also } \beta = h_{FE} = \frac{I_C}{I_B}$$

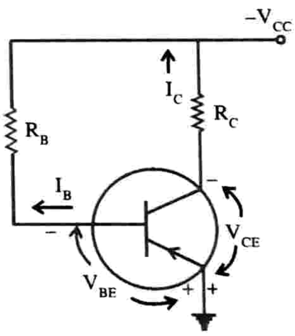



**Fig. 2.24**

$$\therefore \quad I_B = \frac{I_C}{h_{FE}} \qquad \ldots (3)$$

*29. Design a base circuit with $V_{CE}$ = 6V and $I_C$ = 5mA. The supply voltage is 12V. $\beta = h_{FE} = 100$*

*Ans:*

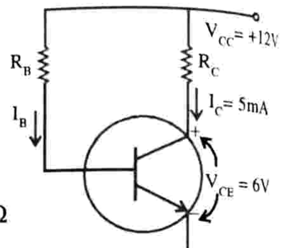


**Fig. 2.25**

$$R_C = \frac{V_{CC} - V_{CE}}{I_C} = \frac{12-6}{5\times10^{-3}}$$

$$= \frac{6}{5}\times10^3 = 1.2\times10^3 = 1.2\text{K}\Omega$$

$$I_B = \frac{I_C}{\beta} = \frac{5\times10^{-3}}{100} = 50\mu\text{A}$$

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{12-0.7}{50\times10^{-6}} = \frac{11.3\times10^6}{50} = 0.226\times10^6$$

$$= \mathbf{226\ K\Omega}$$

*30. Explain the difference between base bias and emitter bias circuits.*

*Ans:*

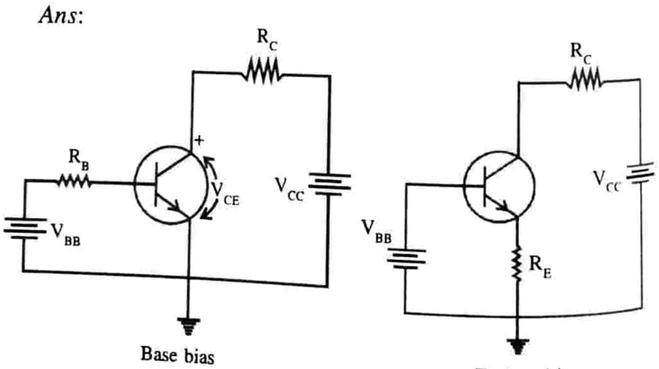


**Fig. 2.26**



Base Resistor moves from base circuit to the emitter circuit.

Base bias is used in digital circuits. Emitter bias used in amplifier circuits.

### Advantages

1. Very simple (only one resistance $R_B$ is required).
2. Calculations are simple.
3. Biasing conditions can easily be obtained.
4. No resistor is used across base emitter junction.

### Disadvantage

1. Poor stabilization. [If $\beta$ increases, $I_C$ also increases ($\because$ $I_B$ = constant)]
2. Stability factor is very high.
3. There is a chance of thermal runaway.

### Voltage divider bias method

It is the most stable bias circuit. Due to the change in $\beta$ of the transistor or by change in temperature, the operating point may change. To compensate this variation, voltage divider bias is used. Here an additional resistance $R_2$ is connected between base and ground. The word 'voltage divider' comes from voltage divider formed by the resistors $R_1$ and $R_2$.

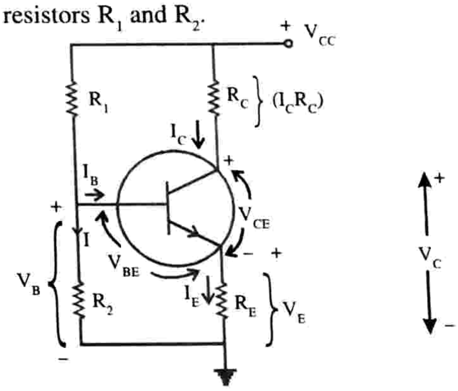


**Fig. 2.27**

According to the voltage divider circuit.

$$V_B = IR_2$$

$$= \frac{V_{CC}}{R_1 + R_2} \cdot R_2$$

$$V_{CC} \times \frac{R_2}{R_1 + R_2} = V_B \qquad \text{... (1)}$$

Apply KVL in lower mesh

$$-V_B + V_E + V_{BE} = 0$$

$$V_E = V_B - V_{BE} \qquad \text{... (2)}$$

$$I_E R_E = V_B - V_{BE}$$

$$I_E = \frac{V_B - V_{BE}}{R_E} \qquad \text{... (3)}$$

$V_B$, $V_{BE}$ and $R_E$ are constants.

$\therefore$ $I_E$ is constant.

$I_E \approx I_C$

$\therefore$ $I_C$ is at constant level

From fig.

$$V_C = V_{CC} - I_C R_C \qquad \text{... (4)}$$

$$V_{CE} = V_C - V_E \qquad \text{... (5)}$$

Substituting (4) in (5)

$$V_{CE} = V_{CC} - I_C R_C - V_E$$

But $V_E = I_E R_E \approx I_C R_E$ $\qquad \because I_E = I_C$

$$\therefore \; V_{CE} \approx V_{CC} - I_C R_C - I_C R_E$$

$$= V_{CC} - I_C(R_C + R_E) \qquad \text{... (6)}$$

Keeping $I_C$ constant, $V_{CE}$ remains constant.



***Note***: In any of the above equations $\beta$ is not there. Voltage divider circuit does not depend on $\beta$.

31. *Discuss the two biasing circuits used in CE amplifier configuration. Also explain how stabilization of operating point is achieved in each case and discuss the advantages of each circuit.* *(CU Nov. 20)*

32. *For the voltage divider circuit shown in figure find the emitter voltage $V_E$, collector coltage $V_C$ and collector emitter voltage $V_{CE}$ ($V_{BE}$ = 0.7V).*

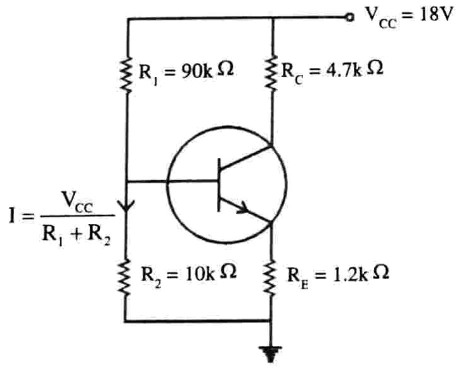



**Fig. 2.28**

$$V_B = \frac{V_{CC}}{R_1 + R_2} \times R_2 = V_{CC} \times \frac{R_2}{R_1 + R_2} \qquad \text{... (1)}$$

$$= 18 \times \frac{10}{90 + 10} = \frac{180}{100} = 1.8\text{V}$$

$$V_E = V_B - V_{BE} = 1.8 - 0.7 = 1.1 \text{ V} \qquad \text{... (2)}$$

$$I_E = \frac{V_B - V_{BE}}{R_E} = \frac{1.8 - 0.7}{1.2 \times 10^3} = \frac{1.1}{1.2} \times 10^{-3} = 0.916\text{mA}$$

$$I_C \approx I_E = 0.916\text{mA}$$

$$V_C = V_{CC} - I_C R_C \quad \cdots (4)$$

$$= 18 - 0.916\times10^{-3}\times4.7\times10^{3}$$

$$= 18 - 4.305 = 13.695 \text{ V}$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E) \quad \cdots (5)$$

$$= 18 - 0.916 \times 10^{-3} (4.7 \times 10^3 + 1.2 \times 10^3)$$

$$= 18 - 5.4 = \mathbf{12.6} \text{ V}$$

**Voltage-divider Bias circuit design**

Rule: $I_2 = \dfrac{I_C}{10}$

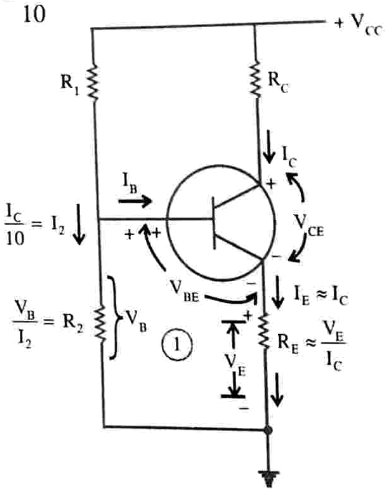



Fig. 2.29

Apply KVL to output

$$I_C R_C = -V_{CE} - V_E + V_{CC}$$

$$R_C = \frac{V_{CC} - V_{CE} - V_E}{I_C}$$



In mesh (1)

$$-V_B + V_E + V_{BE} = 0$$

$$V_B = V_E + V_{BE} \qquad (V_{BE} = 0.7 \text{ V})$$

$$R_2 = \frac{V_B}{I_2} = \frac{V_B}{I_C/10} = \frac{10\, V_B}{I_C}$$

Apply KVL,

$$- I_2 R_1 = V_B - V_{CC}$$

$$R_1 = \frac{V_{CC} - V_B}{I_2}$$

$$R_E = \frac{V_E}{I_C}$$

33. *Design a voltage divider bias circuit in which $V_{CE} = V_E = 6V$ and $I_C = 1.5$ mA. The supply voltage is 24 V and the transistor $\beta = 80$*

*Ans:* $R_C = \dfrac{V_{CC} - V_{CE} - V_E}{I_C} = \dfrac{24 - 6 - 6}{1.5\times10^{-3}} = \dfrac{12\times10^3}{1.5}$

$$= 8 \text{ k}\Omega$$

$$V_B = V_E + V_{BE} = 6 + 0.7 = 6.7$$

$$R_2 = \frac{V_B}{I_2} = \frac{6.7}{I_C/10} = \frac{67}{1.5\times10^{-3}} = \frac{67\times10^3}{1.5} = 44.67 \text{ k}\Omega$$

$$R_1 = \frac{V_{CC} - V_B}{I_2} = \frac{24 - 6.7}{I_C/10} = \frac{17.3}{\frac{1.5\times10^{-3}}{10}}$$

$$= \frac{173\times10^3}{1.5} = 115 \text{ k}\Omega$$

$$R_E = \frac{V_E}{I_C} = \frac{6}{1.5\times10^{-3}} = \frac{6\times10^3}{1.5} = \mathbf{4k\Omega}$$

34. *If $\beta$ of the transistor circuit shown in figure is 50, find the value of $I_C$ using both $\alpha$ and $\beta$.*

*Ans* :

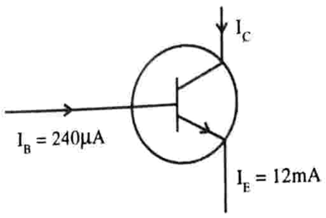



**Fig. 2.30**

$$\beta = \frac{\alpha}{1-\alpha}$$

$$50 = \frac{\alpha}{1-\alpha}$$

$$50 - 50\alpha = \alpha$$
$$51\alpha = 50$$

$$\alpha = \frac{50}{51}$$

$$\alpha = \frac{I_C}{I_B}$$

$$\frac{50}{51} = \frac{I_C}{240\times10^{-6}}$$

$$I_C = \frac{50}{51}\times240\times10^{-6}$$



$$= 0.98\times240\times10^{-6}$$

$$= 235.20\times10^{-6}$$

$$= \mathbf{0.235}\text{ mA}$$

35. *A CE connected transistor has $\beta = 50$ and $I_B = 20\mu A$. Compute the values of $I_C$ and $I_E$.* *(CU Nov. 19)*

36. *A transistor has the following ratings $I_C$ (max) = 500mA and $\beta_{max} = 300$. Determine the maximum allowable value of $I_B$ for the device* *(CU Nov. 19)*

37. *The $\alpha$ of an* ***npn*** *transistor is 0.98. The reverse saturation current $I_{CBO}$ is 12.5 $\mu$A. Determine the base current and collector current for an emitter current of 2mA.* *(CU Nov. 11)*

*Ans*:

Total collector current in CE,

$I_C$ = Total current in CB

$$= \alpha I_E + I_{CBO}$$

$$= 0.98 \times 2 \times 10^{-3} + 12.5 \times 10^{-6}$$

$$= 1.96 \times 10^{-3} + 0.0125 \times 10^{-3}$$

$$= 1.9725 \times 10^{-3}\text{ A}$$

$$= \mathbf{1.9725}\text{ mA}$$

$$\alpha = \frac{I_C}{I_E} = \frac{1.9725}{2} = 0.986$$

$$\beta = \frac{\alpha}{1-\alpha} = \frac{0.986}{1-0.986} = \frac{0.986}{0.014}$$

$$= 70$$

$$\beta = \frac{I_C}{I_B}$$

$$70 = \frac{1.9725 \times 10^{-3}}{I_B}$$

$$I_B = \frac{1.9725 \times 10^{-3}}{70}$$

$$= \mathbf{28\mu A}$$

38. *A transistor uses potential divider method of biasing. $R_1 = 50 K\Omega$, $R_2 = 10 K\Omega$ and $R_E = 1 K\Omega$. If $V_{CC} = 12V$, find*
*(a) The value of $I_C$; given $V_{BE} = 0.1V$.*
*(b) The value of $I_C$; given $V_{BE} = 0.3$ V.*
*Comment the result.* *(CU Nov. 17)*

*Ans*: (i) When $V_{BE} = 0.1V$, voltage across $R_2 = V_2$

$$= \frac{V_{CC}R_2}{R_1 + R_2}$$

$$= \frac{12 \times 10}{50 + 10} = \frac{120}{60} = 2V$$

$$\therefore \quad I_C = \frac{V_2 - V_{BE}}{R_E}$$

$$= \frac{2 - 0.01}{1k\Omega} = 1.9mA$$

(ii) When $V_{BE} = 0.3V, I_C = 1.7mA$

Comment : $I_C$ is almost independent of transistor parameter variations.

39. *In figure collector current is 5mA. Find collector-emitter voltage.*



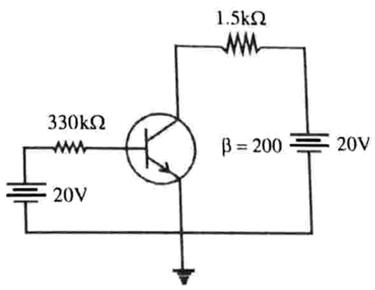



**Fig. 2.31**

*Ans*: $V_{CE} = V_{CC} - I_C R_C$
$= 20 - (5 \times 10^{-3} \times 1.5 \times 10^3) = 20 - 7.5 = 12.5V$

**Comparison of bias circuits**

**Table 2.2**

| *Base bias* | *Collector to base bias* | *Voltage divider bias* |
|---|---|---|
| 1. Only one resistance $R_B$ is required | Only one resistance $R_B$ is required | $R_1$, $R_2$, $R_E$ form biasing |
| 2. Biasing conditions can be easily set and calculations are simple | Provides a –ve feedback which reduces the gain of the amplifier. | |
| 3. There is no loading of the source by the biasing circuit ($\because$ no resistor is used across base-emitter junction) | | |
| 4. Provides poor stabilisation. If β increases due to transistor replacement $I_C$ also increases by the same factor as $I_B$ is constant. | Provides stabilization. But it is not better. | Excellent stabiliation is provided by $R_E$ (Not depending on β) |
| 5. There are chances for thermal run away | | |

40. *Describe the various methods used for transistor biasing? State their advantages and disadvantages.* *(CU Nov. 19)*

## Single stage transistor amplifier circuit

**Action**

When only **one transistor** with associated circuitry is used for amplifying a weak signal, the circuit is called single stage transistor amplifier.

When a weak a.c. signal (say 0.1v) is given to the base of a transistor, a small base current (a.c) starts flowing.

$$\beta = \frac{I_C}{I_B}$$

$$I_C = \beta I_B$$

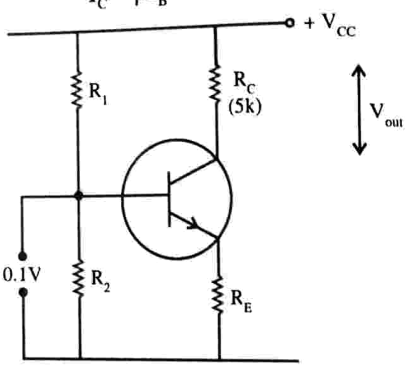



**Fig. 2.32**

$\beta$ is a large quantity

$\therefore$ $I_C$ is large. When $I_C$ flows through $R_C$

$V_{out} = I_C R_C$.

The value of $R_C$ is high.

$\therefore$ $V_{out}$ is high

Thus a weak signal applied to base circuit appears in amplified form in the collector circuit.

In fig., suppose $V_{in} = 0.1V$



$$R_C = 5k\Omega$$

$$\beta = 100, \; I_B = 10\mu A$$

$$\therefore \quad I_C = \beta I_B = 100 \times 10 \times 10^{-6} = 10^{-3} A$$

$$V_{out} = I_C R_C = 10^{-3} \times 5 \times 10^3 = 5V$$

$$\text{Voltage gain} \quad A_v = \frac{V_{out}}{V_{in}} = \frac{5V}{0.1V} = 50$$

**Problems**

41. *What do you understand by single stage transistor amplifier?* *(CU Nov. 19)*

42. *Draw the circuit diagram of a single stage CE amplifier. Describe its working with necessary theory and explain frequency response curve.* *(CU Nov. 20, CU Nov. 18)*

*Ans*: Circuit diagram of CE amplifier using a transistor – Explanation – Frequency response curve by taking frequency along X-axis and gain in Y-axis – and its explanation – Lower cut of frequency, upper cut off frequency, Band width, 3db concept etc.

**Practical circuit of transistor amplifier**

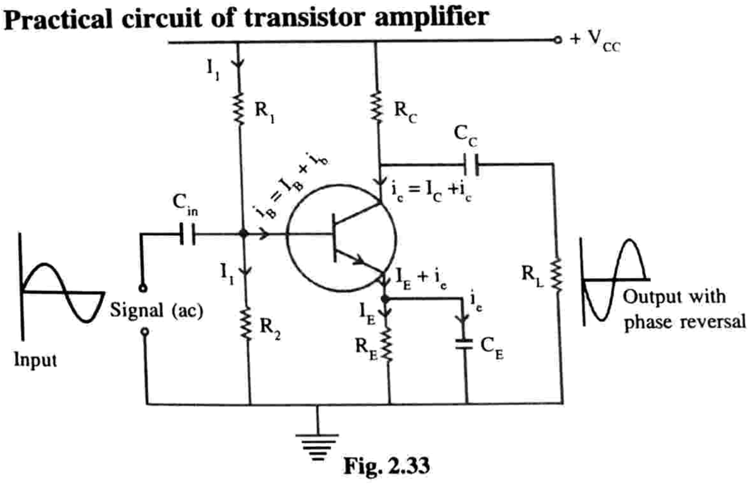



**Fig. 2.33**

$R_1$, $R_2$ and $R_E$ form the biasing and stabilisation circuit. This is for faithfull amplication.

$C_{in}$ is used to couple the signal to the base. It allows only a.c. signal to flow through it. i.e., signal source is isolated from $R_2$. (If C is not used, a.c. signal comes across $R_2$. This affects the biasing.)

$C_E$ is connected in parallel with $R_E$. It provides an easy path to the amplified a.c. signal. (if $C_E$ is not used, amplified a.c. signal will flow through $R_E$ which produces a voltage drop accross it. So output voltage will be reduced.)

$C_C$ is the coupling capacitor. It is used to couple one stage of amplifier to the next. (If $C_C$ is not used $R_C$ will come parallel to $R_1'$ of the next stage (not in figure). So, for the next stage, instead of $R_1'$, $R_C // R_1'$ will result. This will affect biasing condition of second stage) $C_C$ allows only a.c. signal to pass to the next stage.

**Problem**

*43. What do you understand by single stage transistor amplifier?*

*(CU Nov. 19)*

**Currents**

1. (i) $I_B$ : is the base current. This is d.c. It is due to biasing circuit.
2. (ii) $i_b$ : This flows when a.c. signal is applied.
   Total Base Current $i_B = I_B + i_b$
3. (i) $I_C$ : is the collector current when no signal (a.c.) is applied. It is d.c.
   (ii) $i_c$ : when signal (a.c.) is applied $i_c$ flows. It is a.c.
   Total collector current $i_C = I_c + i_c$

*Note* : $\therefore$ Zero signal collector current $I_C = \beta I_B$

When signal is applied $i_c = \beta i_b$.

4. (i) $I_E$ : When no signal is applied. It is d.c.
   (ii) $i_e$ : when signal (a.c.) applied $i_e$ flows.
   Total emitter current $i_E = I_E + i_e$.

*Note* : Apply KCL to the transistor



$I_E = I_B + I_C$

$i_e = i_b + i_c$

$I_B$ and $i_b$ are very small.

## Load line analysis circuit

### DC load line and Bias Point:

D.C load line is the line on the output characteristics of a transistor which gives the values of $I_C$ and $V_{CE}$ corresponding to zero signal.

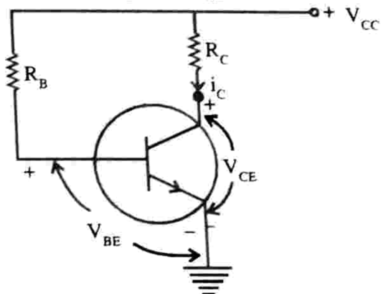



**Fig. 2.34**

Transistor functions linearly when it is made to operate in its active region.

Consider the output of common-emitter circuit as in figure 2.32 and apply KVL

$$I_C R_C = -V_{CE} + V_{CC}$$

dividing by $R_C$

$$I_C = \left(-\frac{1}{R_C}\right)V_{CE} + \frac{V_{CC}}{R_C} \qquad \text{... (1)}$$

Eqn (1) is in the form of $y = mx + C$, which is the equation of a straight line.

Here slope of the line $\mathbf{m} = -\dfrac{1}{\mathbf{R_C}}$ and the constant $\mathbf{C} = \dfrac{V_{CC}}{\mathbf{R_C}}$ which is the intercept on Y-axis.

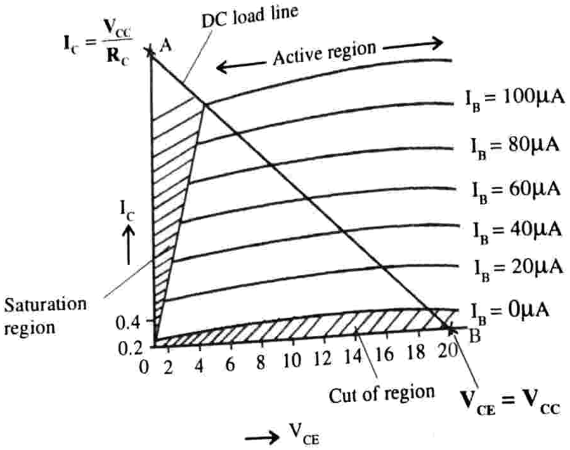



**Fig. 2.35**

In eqn (1) $R_C$ and $V_{CC}$ are constants. It is known as DC load line equation.

The two points required to draw the d.c. load line are found as follows

i) When $\mathbf{V_{CE} = V_{CC}}$, this gives the point **B** on X-axis. At this point the voltage drop across $R_C$ is zero.

Substituting in (1)

$$I_C = \left(-\frac{1}{R_C}\right)V_{CC} + \frac{V_{CC}}{R_C} = 0$$

$\therefore$ $I_C R_C$ is zero.

(or) when $I_C = 0$, $\mathbf{V_{CE} = V_{CC}}$

ii) When $V_{CE} = 0$,

$$(1) \rightarrow \mathbf{I_C = \frac{V_{CC}}{R_C}}$$



This gives the point **A** on Y axis.

The straight line AB drawn through the above two points A and B is the **dc load line**. The inverse of slope of this line gives the resistance of the load.

The portion along the load line which includes all points between saturation and cut-off is known as the **Active region** of the operation of the transistor. Transistor is operated in this linear region. So the output is a linear reproduction of input.

**Problem**

44. *How will you draw d.c. load line on the output characteristics of a transistor? What is its importance?* *(CU Nov. 19)*

45. *How load line is useful?*

*Ans*: Load line represents effect of the load on collector current and $V_{CE}$. Load line contains every possible operating point. When $R_B$ varies form zero to infinity, $I_B$ varies. This makes $I_C$ and $V_{CE}$ to vary over the entire range. If we plot $I_C$ and $V_{CE}$ for every possible values of $I_B$, we get a load line.

## Draw a DC load line for the given circuit

Apply KVL to output circuit

$$I_C R_C = -V_{CE} + V_{CC}$$

$$V_{CE} = V_{CC} - I_C R_C$$

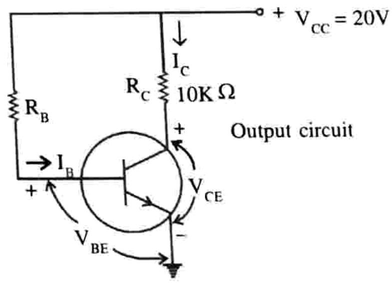



**Fig. 2.36**

When $I_C = 0$,

$$V_{CE} = V_{CC} = \mathbf{20V}.$$

The point A is fixed at this point on X-axis.

When $V_{CE} = 0$

$$0 = V_{CC} - I_C R_C$$

$$I_C R_C = V_{CC}$$

$$I_C = \frac{V_{CC}}{R_C}$$

$$= \frac{20}{10 \times 10^3}$$

$$= 2 \text{ mA}.$$

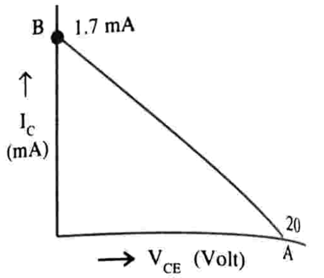


**Fig. 2.37**

The point B is fixed at this point on Y-axis. Drawing AB we get the DC load line.

## DC Bias point (Q-point)

Apply KVL to the base circuit

$$-I_B R_B = V_{BE} - V_{CC}$$

$$I_B R_B = V_{CC} - V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

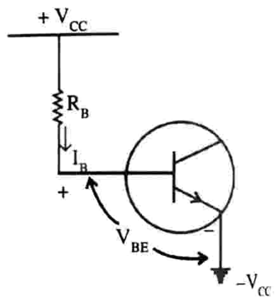


**Fig. 2.38**

For this value of $I_B$ (which is a constant for a particular experiment) draw the output characteristic curve. The intersection of this curve and d.c. load line gives the operating point Q.

Q is called **quiescent point** (quiescent means quite or silent)

The **dc bias point** or **dc operating point** or **quiescent point** or **Q-point** is selected midway between the saturation and cut off where



to collector-to-emitter voltage $V_{CE}$ is equal to nearly half of $V_{CC}$.

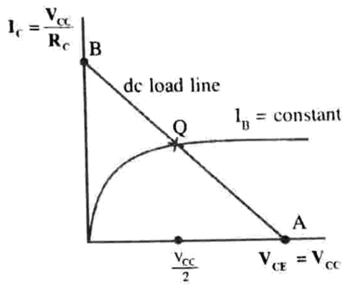


**Fig. 2.39**

### Selection of Q-point

If we fix Q point exactly at the half way along the load line, **faithful amplification** can be achieved. Now $V_{CE}$ ranges from $V_{CC}$ to zero when $I_C$ goes from zero to $\frac{V_{CC}}{R_C}$

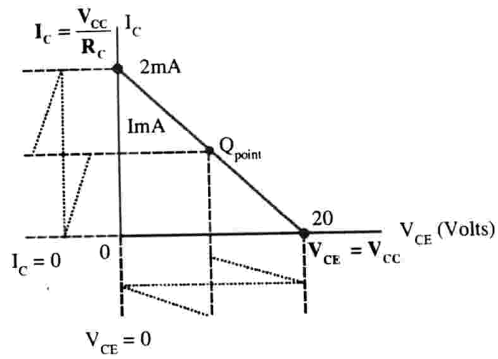


**Fig. 2.40**

Instead, the transistor is biased at $I_C = 0.5\text{mA}$ and $V_{CE} = 15\text{V}$

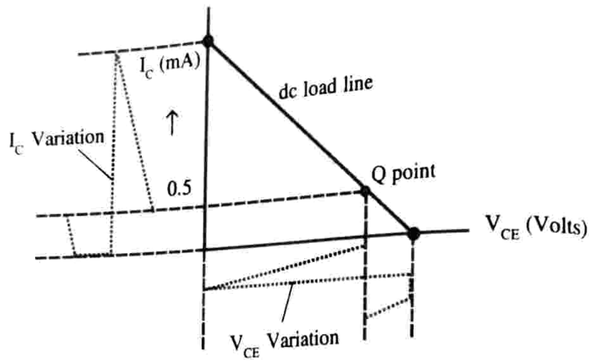



Fig. 2.41

**Problems**

Here the swing is not symmetrical above and below the bias point. When transistor is used as an amplifier, the transistor output voltage ($V_{CE}$) must swing up and down of the Q point by equal amounts. So

*46. Write a short note on operating point* *(CU Nov. 19)*

**Q point must be at the centre of load line**

*47.* $V_{CC} = 12V$, $R_C = 2k\Omega$ *and* $I_B = 30\mu A$. *Find the Q point.*

*Ans* : $V_{CE} = V_{CC} - I_C R_C$

When $I_C = 0$, $\quad V_{CE} = \mathbf{12V}$

When $V_{CE} = 0$, $\quad 0 = 12 - I_C \times 2 \times 10^3$

$$I_C = \frac{12}{2\times10^3} = \mathbf{6mA}$$

So Q point will be at **(12V, 6mA).**

***Note*** : Here the maximum symmetrical output voltage swing will be $I_C = \frac{6}{2} = 3mA$ and $V_{CE} = \frac{12}{2} = 6V$ and $\Delta V_{CE} = \pm 9V$



*48. Calculate the saturation current and cut-off voltage from the fig. given. Draw dc load line.*

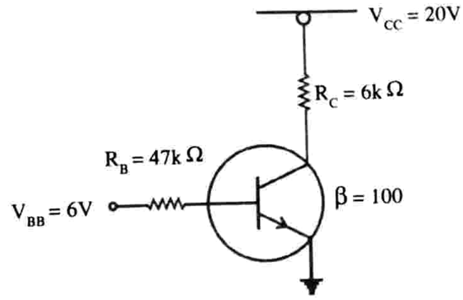



**Fig. 2.42**

*Ans*: $I_{C(saturation)} = \frac{V_{CC}}{R_C} = \frac{12V}{6k\Omega} = 2mA$

Cut off voltage, $V_{CE\ (cut\ off)} = V_{CC} = 12V$

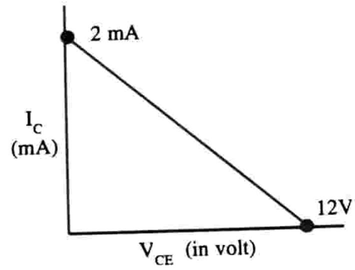



**Fig. 2.43**

*49. Draw the dc load line. Find the dc working point (Q-point).* $\beta = 100$. *Neglect* $V_{BE}$.

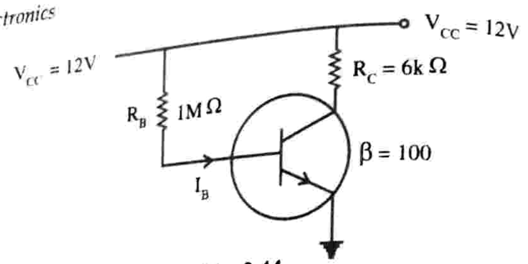



Fig. 2.44

*Ans :* $I_{C(saturation)} = \frac{V_{CC}}{R_C} = \frac{12}{6\times10^3} = 2mA$

Cut off voltage $V_{CE\,(cut\,off)} = V_{CC} = 12V$

DC load line is drawn

Apply KVL to the input circuit

$$-I_B R_B = V_{BE} - V_{CC}$$

$$V_{CC} = I_B R_B + V_{BE} \qquad [V_{BE} \approx 0.7 \text{ neglected}]$$

$$I_B R_B = V_{CC}$$

$$I_B = \frac{V_{CC}}{R_B} = \frac{12}{1\times10^6} = 12\mu A$$

$$I_C = \beta I_B = 100\times12\times10^{-6} = 1.2mA$$

Apply KVL to the output circuit

$$I_C R_C = -V_{CE} + V_{CC}$$

$$V_{CE} = V_{CC} - I_C R_C$$

$$= 12 - 1.2\times10^{-3}\times6\times10^3$$

$$= 12 - 7.2 = 4.8V$$

∴ Q point is **(4.8V, 1.2mA)**



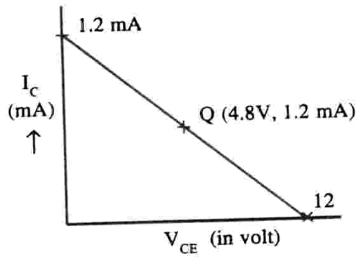



Fig. 2.45

50. *A base bias circuit has* $V_{CC} = 24V$, $R_B = 390K\Omega$, $R_C = 3.3K\Omega$ *and* $V_{CE} = 10V$. *Calculate the transistor* $h_{FE}$ (or) $\beta$ *value.*

*Ans :*

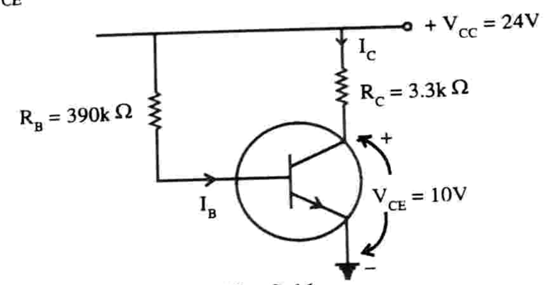



Fig. 2.46

$$\beta = \frac{I_C}{I_B} \qquad \text{... (1)}$$

Apply KVL to output ckt.

$$I_C R_C = -V_{CE} + V_{CC}$$

$$= -10 + 24 = 14$$

$$I_C \times 3.3\times10^3 = 14$$

$$I_C = \frac{14}{3.3\times10^3} = 4.24\times10^{-3} A = 4.24mA$$

Apply KVL to input ckt.

$$-I_B R_B = V_{BE} - V_{CC}$$

$$I_B R_B = V_{CC} - V_{BE}$$

$$= 24 - 0.7 = 23.3V$$

$$I_B = \frac{23.3}{390 \times 10^3} = 0.0000597A = 59.7\mu A$$

$$\beta = \frac{I_C}{I_B} = \frac{4.24 \times 10^{-3}}{59.7 \times 10^{-6}} = 0.0710 \times 10^3 = 71$$

*Note*: **Biasing helps** in setting a fixed level of current with a desired fixed voltage drop across the device.

**Operating point** is a fixed point on the output characteristics. It is specified by voltage & current values.

If voltage divider bias is taken $I_C = \dfrac{V_{CC}}{R_C + R_E}$ and $V_{CE} = V_{CC}$ are taken as two points.

*51. How location of Q point is affected by changing current gain in a base bias circuit?*

Ans: When current gain changes, $I_B$ has no change. But $I_C$ changes. When $I_C$ changes $V_{CE}$ changes. This shifts the Q point. If changes in current gain becomes much larger, the operating point shifts in to cut off or saturation region. Now amplifying circuit becomes useless. This is due to the loss of current gain outside the active region.

**a.c. load line**

**a.c. equivalent circuits:**

Capacitors behave as short-circuits to a.c. signals. So in a transistor circuit all capacitors are replaced with short circuits. Power supplies (including $V_{CC}$) are also behave as a.c. short circuits. (Because d.c. supply voltage is not affected by a.c. signals). So a.c. equivalent circuit of transistor amplifier can be drawn as



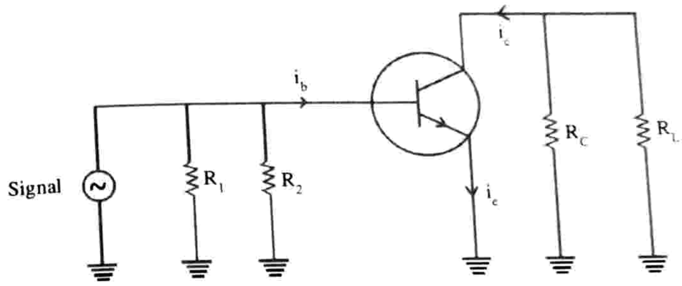



**Fig. 2.47**

When there is no input signal, the transistor voltage and current conditions are same as that of Q point on the d.c. load line. But when a.c. signal is applied, transistor voltage and current levels will change. They vary above and below Q-point. But *Q point is common to both a.c. and d.c. load lines.*

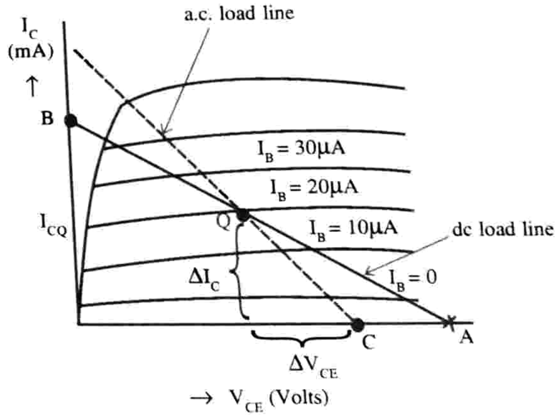



**Fig. 2.48**

Starting from Q point, another point is found on the a.c. load line by taking a convenent collector current change ($\Delta I_C = I_{CQ}$ in figure 2.48) and calculate corresponding change in collector emitter voltage ($\Delta V_{CE}$).

*For example* : Let $V_{CC}$ = 20V, $R_1$ = 18k$\Omega$, $R_2$ = 8.2k$\Omega$, $R_C$ = 2.2k$\Omega$, $V_{BE}$ = 0.7V.

Draw d.c. load line through A and B.

Voltage across $R_2$ } $V_B = \dfrac{V_{CC} \times R_2}{R_1 + R_2} = \dfrac{20 \times 8.2}{18 + 8.2} = 6.3V$

Voltage across $R_E$ } $V_E = V_B - V_{BE} = 6.3 - 0.7 = 5.6V$

$$I_C = I_E = \frac{V_E}{R_E} = \frac{5.6}{2.7 \times 10^3} = 2.07mA.$$

Mark the Q point on the d.c. load line at $I_C$ = 2.07mA = $I_{CQ}$.

**To draw a.c. load line**

Put $R_L = 0$

When $I_C$ changes by $\Delta I_C$ = 2.07mA

$\Delta V_{CE} = \Delta I_C \times R_C$ = 2.07mA × 2.2k$\Omega$ = 4.55V.

Plot point C at $\Delta I_C$ = 2.07mA & $\Delta V_{CE}$ = 4.55V from the Q - point. Then draw a.c. load line through points C and Q. (see figure 2.48).

52. *The point of intersection of DC and AC load line is ............ .* *(CU Nov. 18)*

*Ans:* Q - point

53. *Draw the a.c. equivalent circuit of a single stage transistor amplifier circuit* *(CU Nov. 20)*

54. *Determine the Q point of the transistor circuit shown in fig.2.49. Also draw the d.c. load line. Given*

$R_C = 1k\Omega, R_B = 47k\Omega,$

$R_E = 4.7k\Omega, V_{CC} = 10V, \beta = 100$

*and* $V_{BE} = 0.7V$.

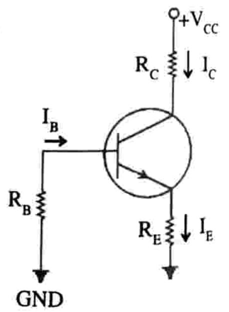



**Fig. 2.49**



*Ans:*

*Hints* : Find (i) Cut off voltage

(ii) Saturation current

– Draw the graph

– Find the operating point

– Mark the point in the graph.

## Exercises

1. How are the two transistor junctions biased for a transistor operation?
2. n-p-n transistor is preferred over pnp transistor. Why?
3. Distinguish between $\alpha_{dc}$ and $\alpha_{ac}$ .
4. Distinguish between $\beta_{dc}$ and $\beta_{ac}$
5. Why base region of a transistor is narrow and lightly doped.
6. Bring out the relation between $\alpha$ and $\beta$ of a transistor.
7. Explain the temperature dependance on current gain.

   *Ans:* When temperature increases collector current increases. Theirefore current gain increases.
8. What are the different types of transistor configurations? Draw circuit diagram of each type using NPN transistor. Explain each.
9. Sketch the input and output characteristics of NPN transistor in CE configuration.
10. Explain biasing of a transistor.
11. Explain the source of the leakage current in a transistor.
12. Explain the active, saturation and cut-off regions of a transistor.
13. Transistor means 'Transfer of Resistance'. Explain this statement.
14. Describe the action of pnp transistor
15. Describe the action of npn transistor
16. Explain leakage current in a transistor