Engineering 378 HW #1

SFSU Fall 2016

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Problems 1.9, 1.13 (ignore part c), 1.17

Engr 378 Homework #1

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1.9 Show how you can construct a T flip-flop using a J-K flip-flop.

1st Derive Excitation table for J-K Flip-Flop as practice.

Truth table

Clk	J	K	Q_{n+1}	
0	X	X	Q_n	Memory
1	0	0	Q_n	Memory
1	0	1	0	
1	1	0	1	
1	1	1	Q_n	(toggle)

Characteristic table

Q_n	J	K	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

Excitation Table J-K Flip Flop

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Excitation Table T-flip-flop

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Conversion Table

JK Flip Flop → T Flip Flop

T input	Outputs Q_n	Outputs Q_{n+1}	J-K inputs J	J-K inputs K
0	0	0	0	X
0	1	1	X	0
1	0	1	1	X
1	1	0	X	1

K-Map

... sum of products expression

Δ for J

T \ Q_n	0	1
0	0	X
1	1	X

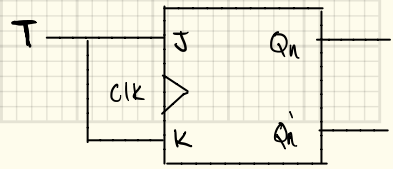
J = T

Δ for K

T \ Q_n	0	1
0	X	0
1	X	1

K = T

... So this is a T flip flop using a J-K flip flop.



(b) Show how to construct a JK flip-flop using a D flip-flop and gates.

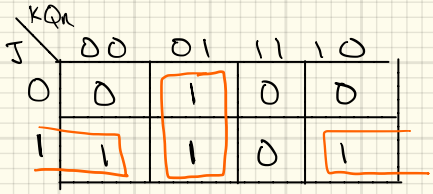
Excitation Table for a D flipflop

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

Δ Conversion table of D-flip flop to JK flip-flop

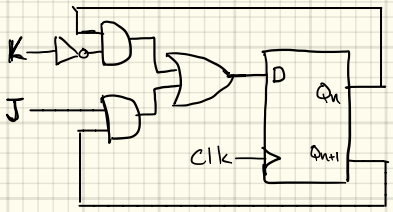
J-K inputs J	K	Outputs Q_n	Q_{n+1}	D flip-flop input D
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	0	0
1	0	0	1	1
1	0	1	1	1
1	1	0	1	1
1	1	1	0	0

Δ Deriving Sum-of Products expression for D



$D = J\overline{Q_n} + \overline{K}Q_n$

JK Flip Flop using D flip flop

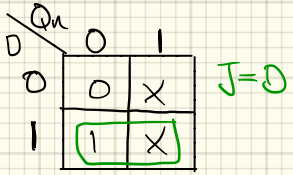


(C) Show how you can construct a D flip-flop using a JK flip-flop and gates

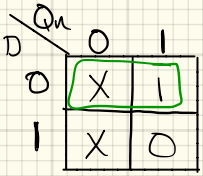
Conversion table of J-K flip-flop to D flip-flop

D input	Outputs		J-K flip-flop inputs	
D	Q_n	Q_{n+1}	J	K
0	0	0	0	X
0	1	0	X	1
1	0	1	1	X
1	1	0	X	0

Sum of products for J using K Map ... for K

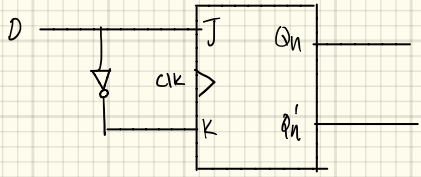


J=D



$K=\overline{D}$

△ Construct a D flip-flop using J-K flip flops



13. Derive a Mealy state graph and table with a minimum number of states(6 states).

X	S	V
0000	0010	0
0001	0011	0
0010	0100	0
0011	0101	0
0100	0110	0
0101	0111	0
0110	1000	0
0111	1001	0
1000	1010	0
1001	1011	0
1010	1100	0
1011	1101	0
1100	1110	0
1101	1111	0
1110	0000	1
1111	0001	1

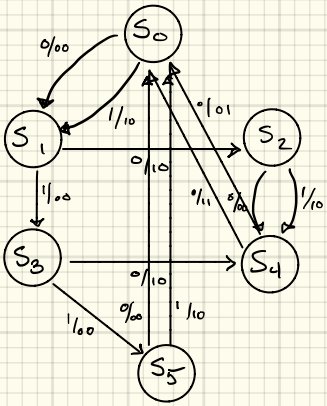
1.13 A sequential circuit has one input (X) and two outputs (S and V). X represents a 4-bit binary number N, which is input least significant bit first. S represents a 4-bit binary number equal to $N + 2$, which is output least significant bit first. At the time the fourth input occurs, $V = 1$ if $N + 2$ is too large to be represented by 4 bits; otherwise, $V = 0$. The value of S should be the proper value, not a don't care, in both cases. The circuit always resets after the fourth bit of X has been received.

(a) Derive a Mealy state graph and table with a minimum number of states (six states).

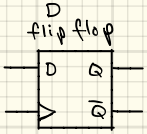
(b) Try to choose a good state assignment. Realize the circuit using D flip-flops and NAND gates. Repeat using NOR gates. (Work this part by hand.)

(a)

PS	NS X=0	NS X=1	SV X=0	SV X=1
S0	S1	S1	00	10
S1	S2	S3	10	00
S2	S4	S4	00	10
S3	S4	S5	10	00
S4	S0	S0	00	10
S5	S0	S0	11	01

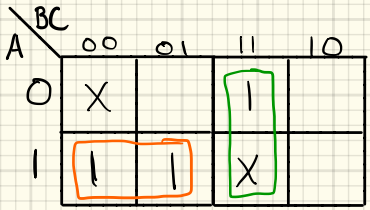


17. Derive the state transition table and the flip-flop input equations of a counter that counts from 1 to 6 (and back to one and continues).

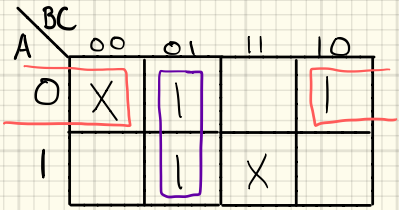


CLK	D	Q	$\bar{Q}$
0	0	Q	$\bar{Q}$
0	1	Q	$\bar{Q}$
1	0	0	1
1	1	1	0

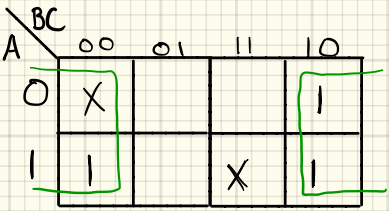
	Present State (ABC)	Next State (ABC)	
–	000	XXX	→ ABC
1	001	010	1
2	010	011	2
3	011	100	3
4	100	101	4
5	101	110	5
6	110	001	1
–	111	XXX	



$D_A = AB' + BC$



$D_B = A'C' + B'C$



$D_C = C'$