Homework #7 3.14 -- 3.15 -- 3.16

Engineering 378

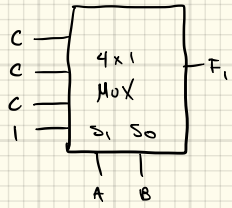
Farnam Adelkhani
915815724

3.14 **(a)** Implement the function $F_1 = A'BC + B'C + ABC$ using an FPGA with programmable logic blocks consisting of 4-to-1 multiplexers. Assume inputs and their complements are available as shown in Figure 3-34.

(b) Implement the function $F_1 = A'B + AB' + AC' + A'C$ using a multiplexer. What is the size of the smallest multiplexer needed, assuming inputs and their complements are available?

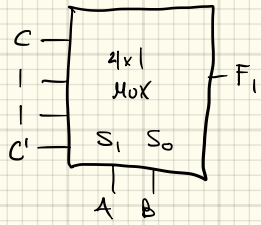
A $F_1 = \bar{A}BC + \bar{B}C + AB\bar{C}$ can be implemented w/ an FPGA w/ prog. logic blocks

inputs A	B	C	outputs F_1	Mux input in terms of $\{0, 1, C, \bar{C}\}$
0	0	0	0	C
0	0	1	1	
0	1	0	0	C
0	1	1	1	
1	0	0	0	C
1	0	1	1	
1	1	0	1	1
1	1	1	1	



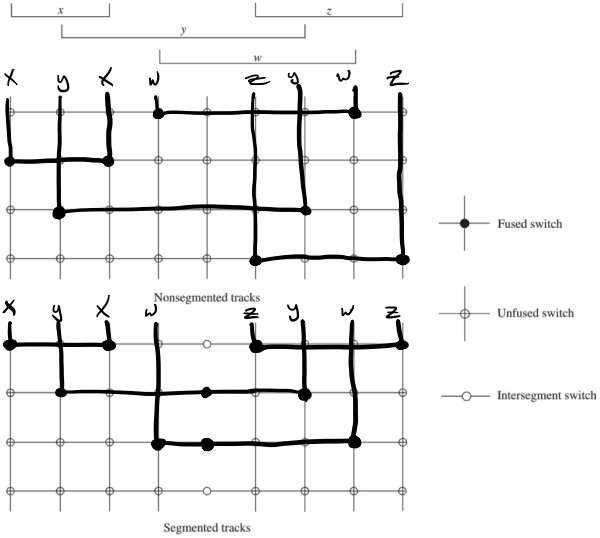
B

inputs A	B	C	outputs F_1	Mux input in terms of $\{0, 1, C, \bar{C}\}$
0	0	0	0	C
0	0	1	1	
0	1	0	0	1
0	1	1	1	
1	0	0	0	1
1	0	1	1	
1	1	0	1	$\bar{C}$
1	1	1	1	

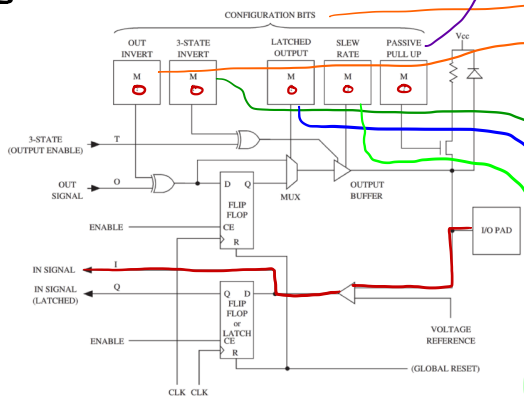


3.15 **(a)** Route the "w", "x", "y", and "z" nets on the non-segmented tracks shown in the diagram that follows. Use the minimum number of tracks possible.

(b) Route the "w", "x", "y", and "z" nets on the segmented tracks shown in the diagram that follows. Use the minimum number of tracks possible.



3.16 Consider the following programmable I/O block:



Highlight the connections to configure this I/O block as an INPUT pin. Specify the five configuration bits.

▷ avoid floating points of output signal.

▷ allow control of aspects of I/O blocks

1 - inverts output using exclusive OR
0 - acts as a buffer

▷ there block acts as input so assuming it is 0

▷ create active High/low state control signal

• when I/O block is used as input the output buffer must be in high-impedance state and hence the configuration bit is 0

▷ provide output in latched or complimented form
... since not using I/O blocks this is 0

▷ Controls rate at which output signal can be changed
.... since not using I/O block this is 0.