```verilog
module multi(Digi2, Digi1, Digi0, swtch, bttn);

        input [3:0] bttn;
        input[2:0]swtch;

        output [6:0] Digi2, Digi1, ;
        reg [6:0] Digi2, Digi1, Digi0;

        always @ (swtch or bttn) begin;

        if (bttn == 2) begin;
        case(swtch)
                0: begin Digi0 = 7'b0000001; Digi1 = 7'b0000000; end

        endcase
        end

        else if(bttn == 1) begin

        case(swtch)
                0:Digi0 = 7'b
        endcase
        end

        else if (bttn == 0) begin

        case(swtch)
                0:Digi0 = 7'b
        endcase
        end
        else begin
        Digi0 = 7'b0000000;
        Digi1 = 7'b0000000;
        Digi2 = 7'b0000000;
        end
end
endmodule
```