San Francisco State University

Electrical Engineering

ENGR 378 Digital systems design

Lab 3. Latches, Flip-flops and Sequential Circuits

Objectives

• To learn Verilog design of basic sequential circuit components: latches and flip-flops.

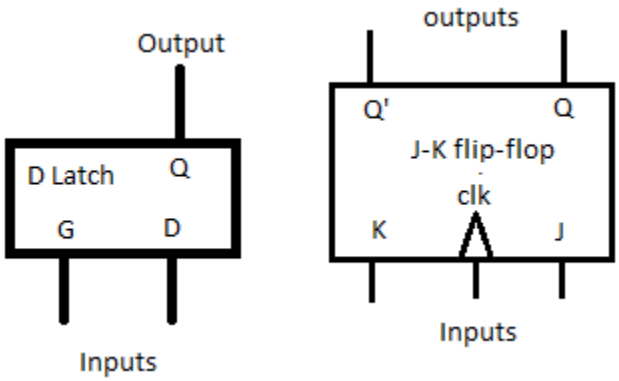
• To learn Verilog design of complete sequential circuits

• To design and experiment simulation testbench modules for sequential circuits using Verilog.

Prelab

(Every group member should do the prelab)

1. Write the truth tables for the following D latch and J-K flip-flops shown below and characterize their output signals in terms of their input signals in words.



2. Using a maximum of two JK flip-flops and no other registers, design a 2-bit counter with an active high reset signal. You can use any method such as circuit diagrams, logic tables, K-maps, etc. for this part as you see fit. Just be sure you are able to translate your design to Verilog code for lab. Also include an active high signal to reset the counter. The counter should run from 0 to 3 and then back to 0.

Tasks

1. D Latch design and simulation.

a) Write a Verilog module for the D latch.

b) Write a Verilog testbench module for the D latch and perform the simulation.

c) Verify it works by comparing the waveforms to the truth table from prelab.

2. J-K flip-flop design and simulation.

a) Write a Verilog module for the J-K flip-flop.

b) Write a Verilog testbench module for the J-K flip-flop and perform the simulation.

c) Verify it works by comparing the waveforms to the truth table from prelab.

3. 2-bit counter design and simulation.

a) Write a Verilog module for the 2 bit counter (with active high reset signal) using two JK flip-flops.

b) Write a Verilog testbench module for the cou Verilog nter and perform the simulation.

c) Verify the counter works by checking the 2-bit counter counts up from 0 to 3 and back to 0. Also make sure the reset signal resets the count to 0 when set high.

d) Show the counter waveforms to the lab instructor to have it signed off.