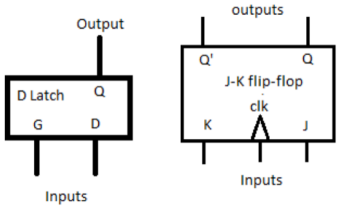
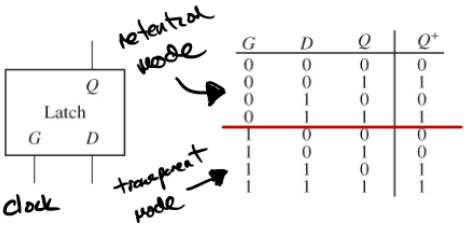
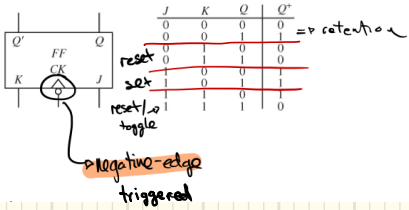
Prelab

1. Write the truth tables for the following D latch and J-K flip-flops shown below and characterize their output signals in terms of their input signals in words.







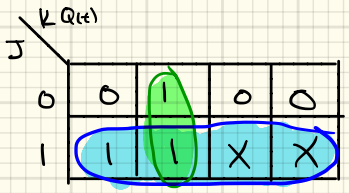
No 0... ➡ positive level sensitive latch

JK flip flop
- when J = 0 & K = 0 ... Q is in retention
- when J = 0 & K = 1 ... reset
- when J = 1 & K = 0 ... set
- when J = 1 & K = 1 ... toggle the circuit.

D latch
- when G = 0 & D = 0/1 ... retention mode
- when G = 1 & D = 0/1 ... transparent mode

2. Using a maximum of two JK flip-flops and no other registers, design a 2-bit counter with an active high reset signal. You can use any method such as circuit diagrams, logic tables, K-maps, etc. for this part as you see fit. Just be sure you are able to translate your design to Verilog code for lab. Also include an active high signal to reset the counter. The counter should run from 0 to 3 and then back to 0.

J	K	Q(t)	Q(t+1)	
0	0	0	0	
0	0	1	1	
0	1	0	0	
0	1	1	0	
1	0	0	1	
1	0	1	1	
1	1	0	X	} toggle
1	1	1	X	}



$Q_0, Q_1 = 1$ reset