Exp. 8:Latches and Flip-Flops

Engineering 357 - Digital Design Lab
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Experiment #5

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Abstract and Objective:

The objective and purpose of this lab assignment is to gain familiarity with latch and flip-flop circuits and their operational characteristics. When dealing with combinational circuits if the designer wanted to maintain a certain output, then she/he must maintain the required input combination. The topic being introduced in this lab is latches and flip-flops which have two stable states and stay in one of the two states unchanged even after the inputs are removed. This is an introduction to the first memory element studied in this course.

A pushbutton switch will be implemented to serve as the clock signal in the circuit. Each sequence of push and then release produces a positive pulse at the NORM OFF terminal and a negative pulse at the NORM ON terminal. The positive signal that is generated at the NORM OFF terminal is known as the positive edge of the clock pulse. When the button is released the transition from high to low takes place at the NORM OFF terminal causing it to now produce the negative-edge of the pulse. Pushbutton switches are used to generate pulse signals such as clock.

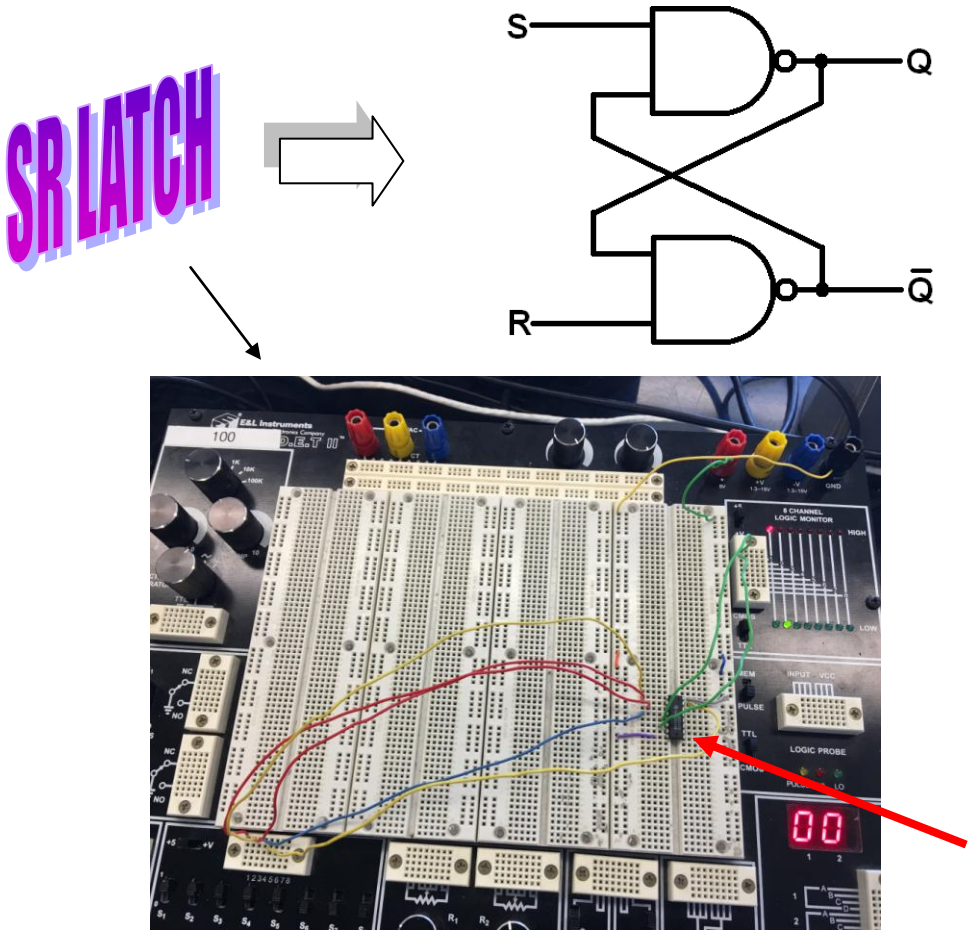
Components Used:

- Cadet II complete analog/digital electronics trainer complete with integrated breadboards
- Probing Wires
- The following gates/integrated circuits:
  - (3)74LS00 – Quad 2-input NAND gates
  - 74LS04 – Hex Inverters
  - 74LS08 – Quad 2-input AND gates
  - 74LS74A – Dual D type positive-edge-triggered flip-flops
  - 74LS112A – dual jk negative-edge-triggered flip-flops
- Logic Switches and the Logic Monitor are components of the Cadet used

Procedures and result:

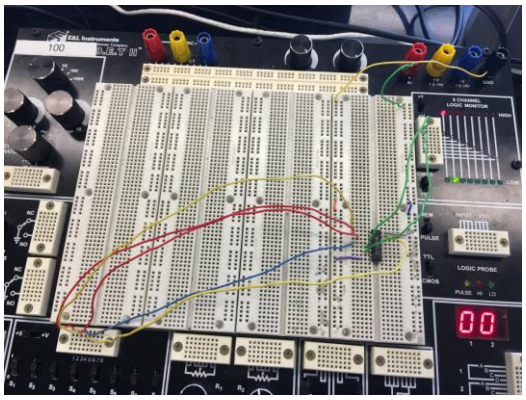
-Basic SR Latch-

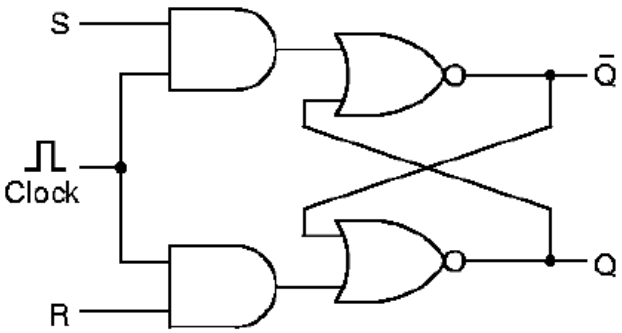
First step is to implement a basic SR Latch onto the breadboard using the required components. The SR latch can be constructed from basic logic gates such as the NAND, NOR, or-inverters and is often referred to as the S'R' latch, since it takes a logic-0 at these inputs to change the states of the latch. The basic SR latch was implemented and tested, the truth table was confirmed.



Clocked (Strobed) SR Latch

Next step is the addition two nand gates to the circuit to form the clocked SR Latch. The clock signal comes from the NORM OFF output of a pushbutton switch. A clock pulse is generated when the button is pushed and then released. The additional circuitry necessary was implemented onto the breadboard and the truth table was found.



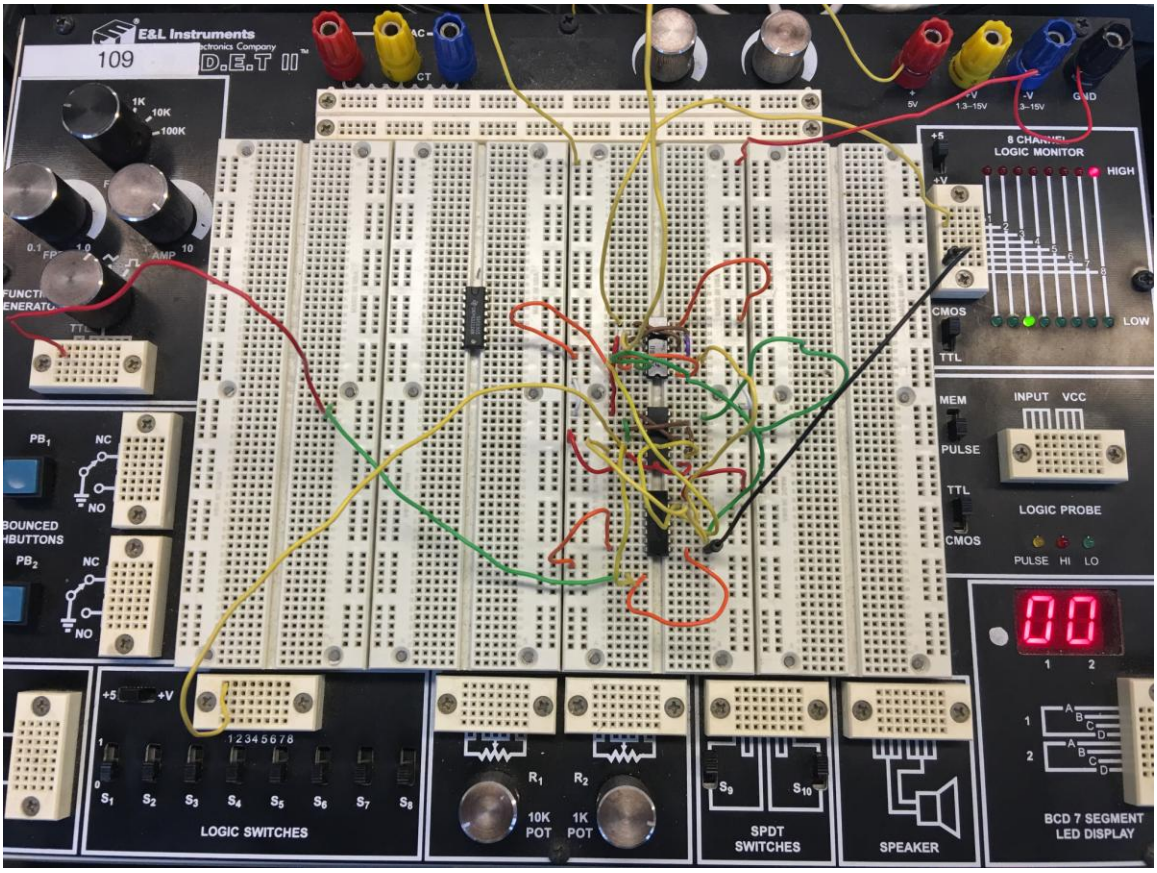


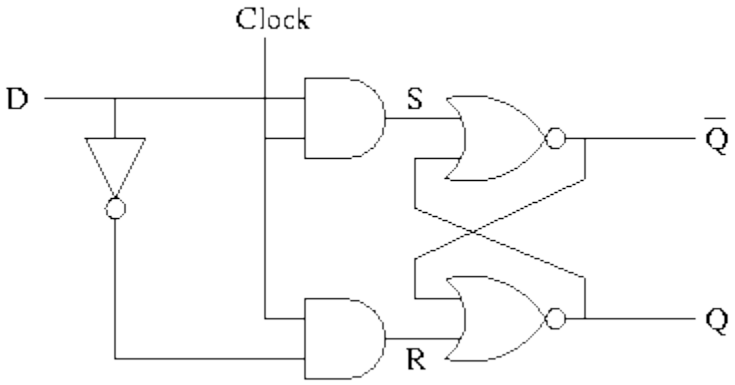
S	R	Q	Q+	Q'+
0	0	0	0	1
0	0	1	1	0
0	1	0	0	1
0	1	1	0	1
1	0	0	1	0
1	0	1	1	0
1	1	0	1	1
1	1	1	1	1

The characteristic table above was experimentally completed using the breadboard setup. It is not necessary to follow any particular order when filling out the table. When the signal line S goes high, the other line to the NAND gate from the pulse steering circuit must also be high for it to generate a low output. Likewise, a clock pulse must have the reset NAND gate high to receive a high RESET pulse. Therefore all transitions are synchronized to the clock. When resetting the nand gate The time sequence at right shows the conditions under which the set and reset inputs cause a state change, and when they don't.

Clocked D Latch

The clocked SR latch can be converted to a clocked D latch by simply adding an inverter between the S and R inputs. The clocked D latch also has two modes of operations: transparent and blocked. This depends on when the Q output follows the changes of the D input. The latch is in the transparent mode of operation. When the latch output does not react to changes at the D input it is in the block mode.

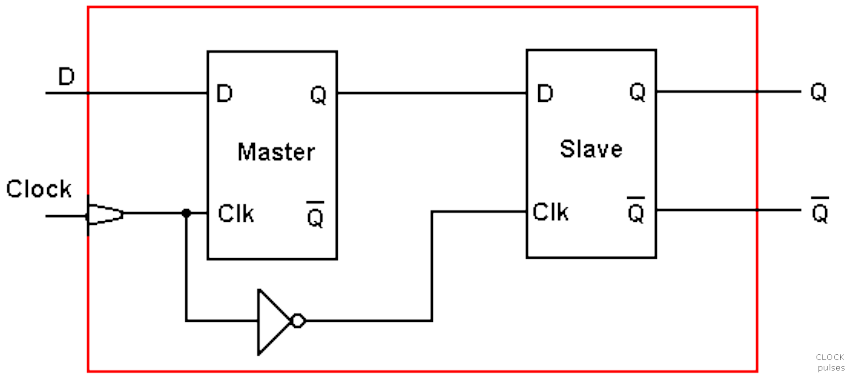


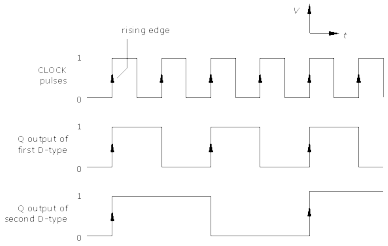


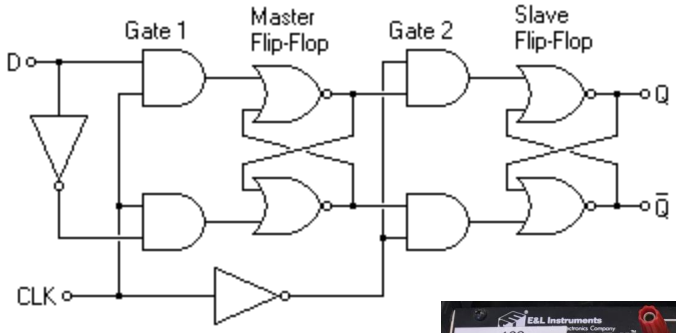
Clocked D latch

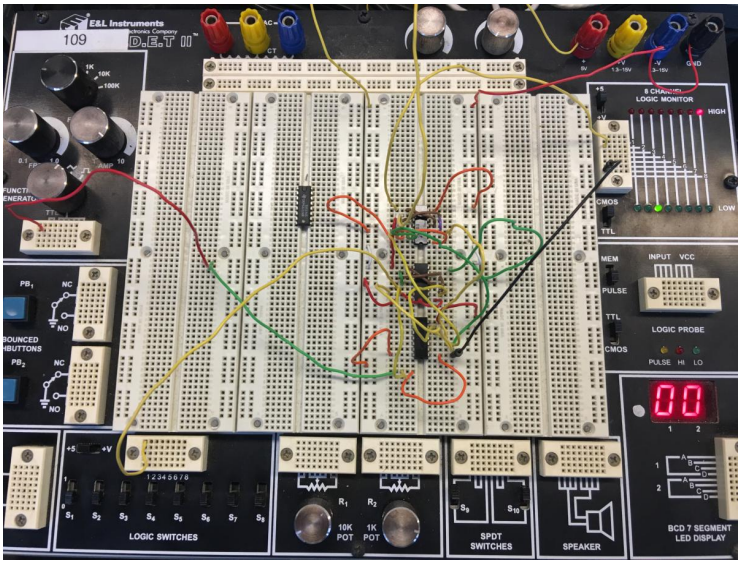
D Flip Flop

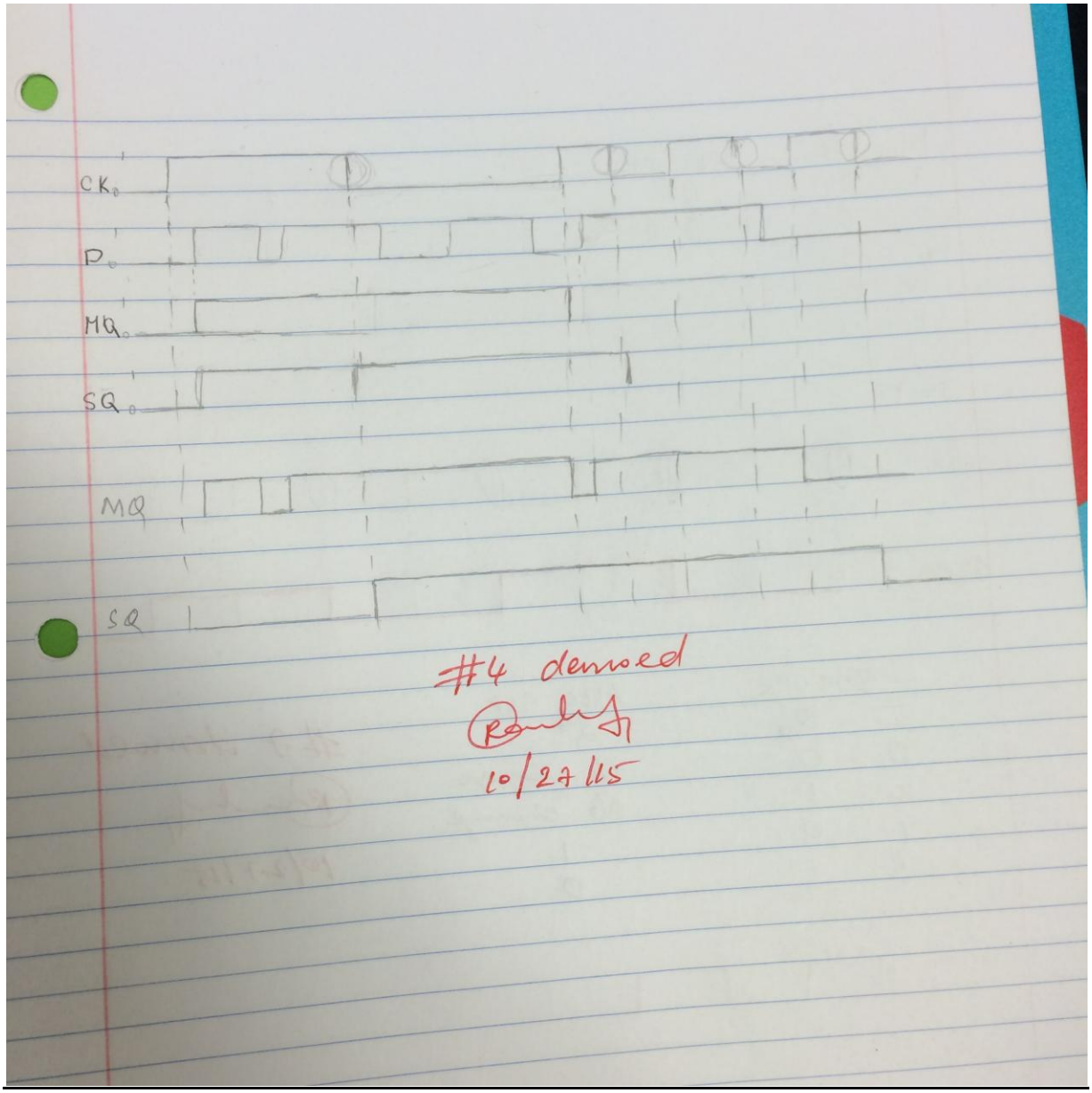
One of the main disadvantages of the basic SR NAND Gate bi stable circuit is that the indeterminate input condition of "SET" = logic "0" and "RESET" = logic "0" is forbidden. This state will force both outputs to be at logic "1", over-riding the feedback latching action and whichever input goes to logic level "1" first will lose control, while the other input still at logic "0" controls the resulting state of the latch. But in order to prevent this from happening an inverter can be connected between the "SET" and the "RESET" inputs to produce another type of flip flop circuit known as a Data Latch, Delay flip flop, D-type Bistable, D-type Flip Flop or just simply a D Flip Flop as it is more generally called.







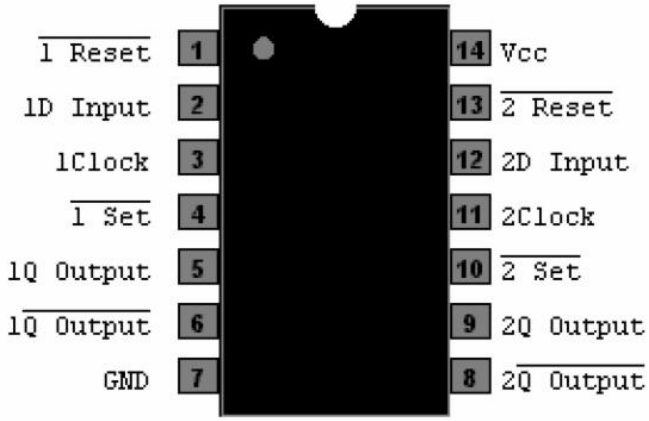


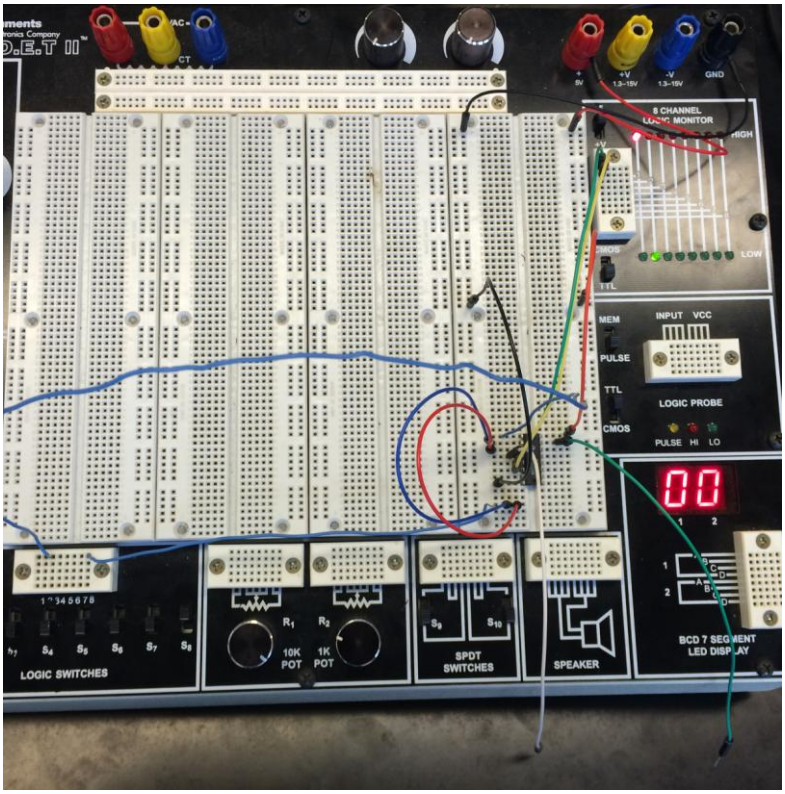


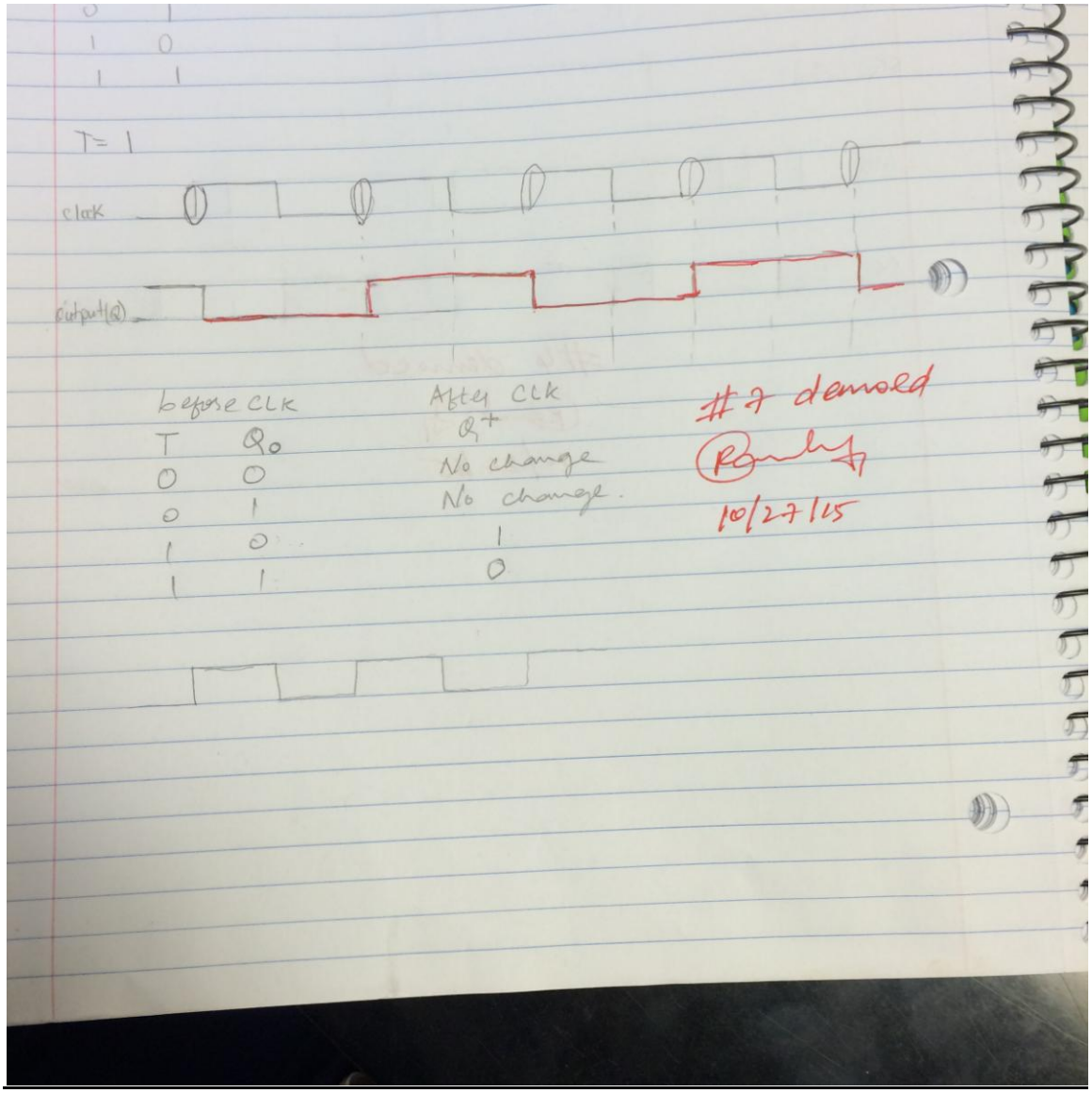
The 74LS74A

This device contains two independent positive-edge-triggered D flip-flops with the complementary outputs. The information directed onto the D input is accepted by the flip-flops on the positive going edge of the clock pulse. The triggering occurs at a voltage stage and is not openly related to the transition time of the rising edge of the clock. The data on the D input may be changed while the clock is LOW or HIGH without affecting the outputs as long as the data system and hold

times are not violated. A low logic level on the preset or clear inputs will set or reset the outputs in spite of the logic levels of the other inputs.







before CLK	
T	Q_0
0	0
0	1
1	0
1	1

After CLK
Q^+
No change
No change.
1
0

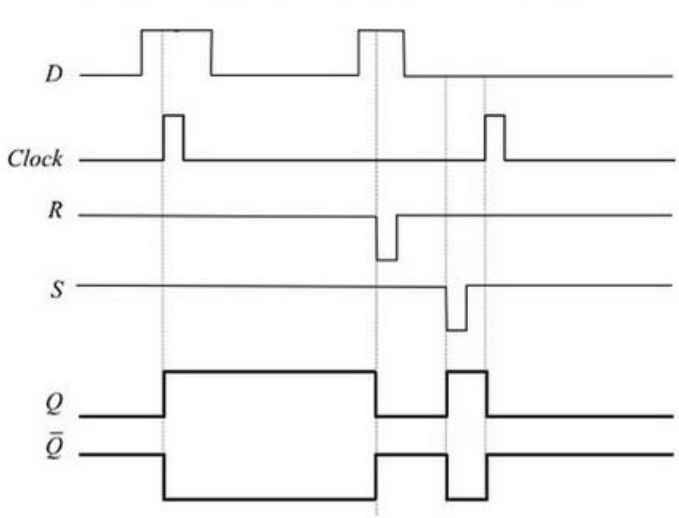
#7 demoed
10/27/15

Solutions to Questions:

74LS74A. What is the active level for the asynchronous inputs?.....

Asynchronous input set(s) and reset(R) on a flip-flop have control over the output regardless of clock input status. These inputs are called the present and clear. The present input drives the flip-flop to a set while the clear input drives it to a reset state.

When the present is activated the flip flop will be set regardless of any of the synchronous input or the clock. When the clear input is activated the flip-flop will be reset regardless of any of the synchronous input or the clock.



Post lab and Conclusion

It was found to save a tremendous amount of time when the circuit was simplified on paper before implementation especially when things got more complicated with two flip flops. This was an interesting introduction to clocks and how they function. The circuit is set to the state it wants to be set at and then the clock is set which allows the circuit to enter the set position and override or overlook and intermediate steps that may have interfered with the circuit and would have been a problem, without a doubt. Latches and flip flops can now be implemented into our tools arsenal as digital design engineers.