Exp. 5:Introduction to troubleshooting

Engineering 357 - Digital Design Lab
Fall 2015

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Date Experiment Performed: 9-10-2015

Date Report Submitted: 9-12-2015

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Experiment #5

Exp. 5 – Introduction to Troubleshooting

Abstract and Objective:

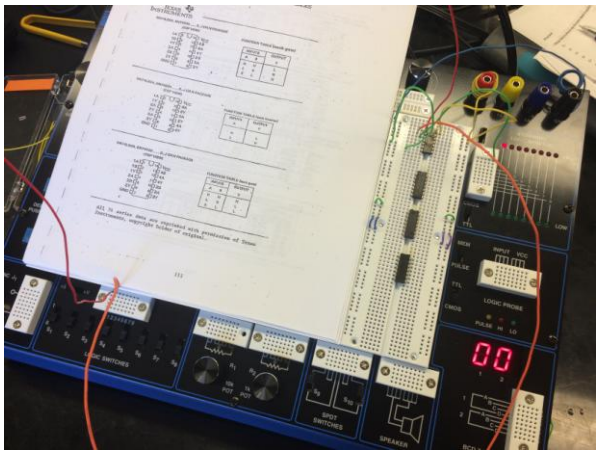
The objective and purpose of this lab assignment is to practice systemic hardware construction and troubleshooting techniques. We begin the lab by setting up our power (Vcc) and ground (GND) buses. The first objective is to test all the components (ICs) being used. After we have confirmed all the pins on the component we are using are functioning properly we move on to more advance troubleshooting techniques. We now build circuits using our IC's at hand and test for the desired outputs. After we confirm we have the outputs anticipated, we will introduce a problem/malfunction to the circuit and have our circuit lab partner check to see if they can find the issue without any direction. Then we switch and the other lab partner will go through the same process.

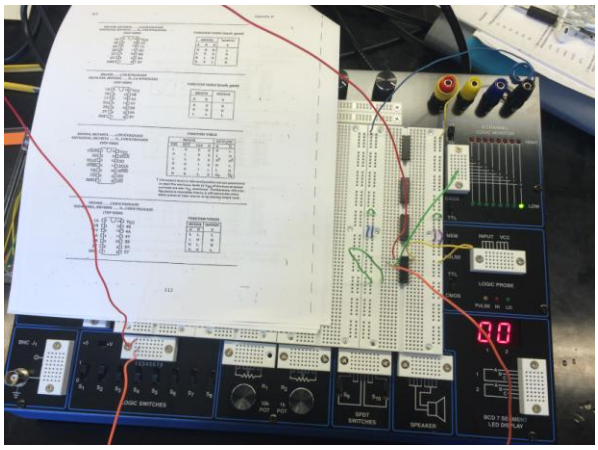
Components Used:

- Cadet II complete analog/digital electronics trainer complete with integrated breadboards
- Probing Wires
- The following gates/integrated circuits:
- 74LS00 74LS0474LS0874LS3274LS86A
- Logic Switches and Logic Monitor

Procedures and result:

1. We begin by connected all five ICs, 74LS00, 74LS04, 74LS08, 74LS32, and 74LS86A, onto the breadboard and of course connect V_{cc}/GND to the proper pins of the first IC being tested. As advised by our Professor during last lab class session, we setup our V_{cc} and GND buses on the left/right columns on the breadboard.We chose the right most breadboard because it is the closest to the Logic Monitor and we don't have excess wires longer than ~6 inches.



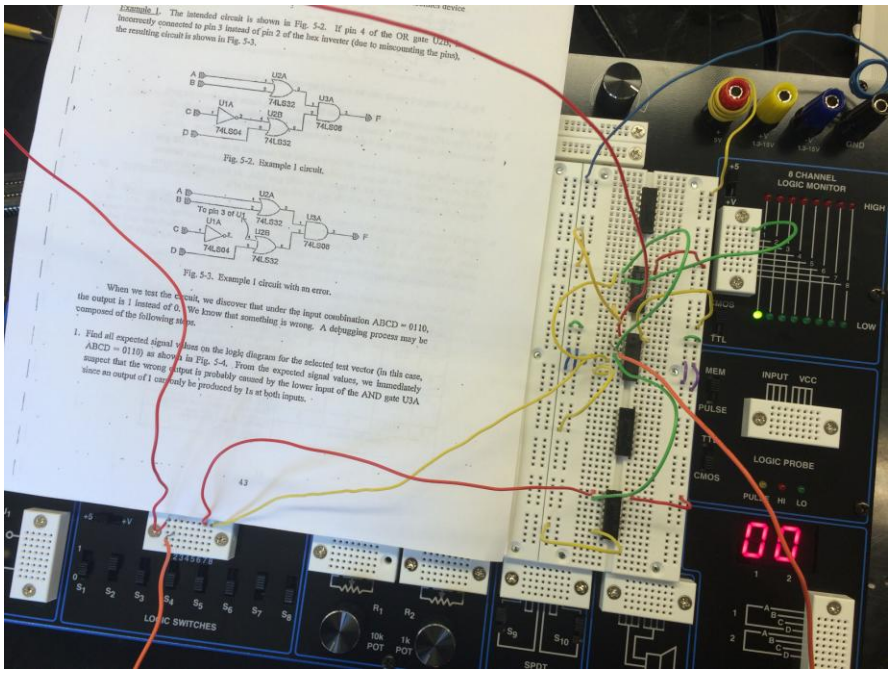


2. Next we connected two logic switches to the inputs of the first IC we are testing. We also connect a probe from the output of the IC to the input of the logic monitor. We test every combination of inputs from the switches (00,01,11,10) and assure that the outputs are as expected. We do this for every set of inputs/outputs on every IC. This is a tedious process but crucial and it is easy to see how doing this can save you much more time and money in the future in regards to not having to troubleshoot as much or as intensely.

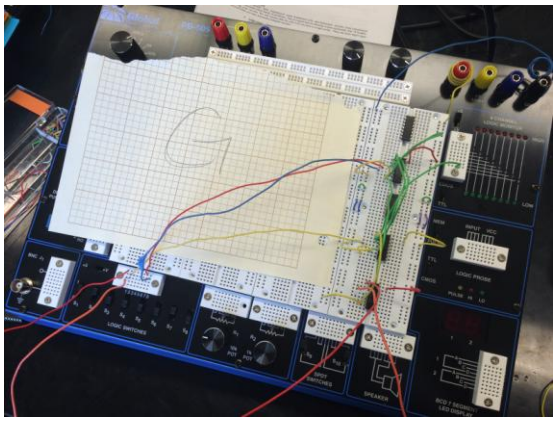
3. Now that it has been determined that all of our ICs are currently functional we are ready to build a circuit. We label and number our ICs. We are going to build a circuit and then test for the 3 types of errors that can arise; logic errors, component failures and connection errors. As we build our circuit we trace the connections we have made with a red pen. We found errors after building our circuit; logic outputs were not as expected. So we took another look at our circuit and fixed the errors which consisted of incorrectly connected wires. We then acquired the desired outputs from our circuit and we were ready to move on to the next step.

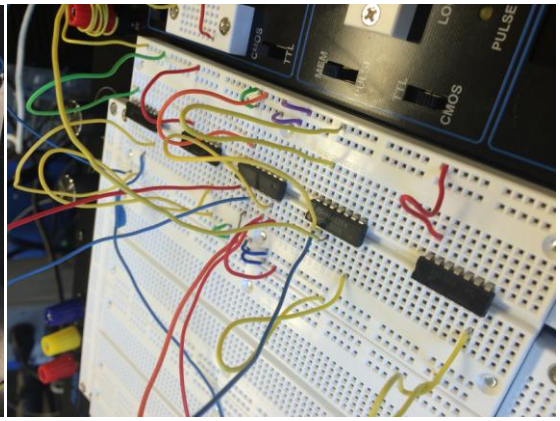
4. Now we introduce errors to our circuit and test our logic outputs tracing backwards from the final output. We trace back till we find the IC that is giving us the incorrect output. When we find the Problem IC we proceed

to analyze that component to see why it is giving an improper output. The likely hood of the problem being with the component itself is very low because we began the lab session by testing all our components; so we know they are functional. We proceeded to look at the probes instead. We found that the IC was improperly connected. So this was a solid fault that was not created by environmental factors but instead by a misconnection that is always going to be there. This was really expected because we created the error so there was no way we wouldn't know what the problem was.



5. The final circuit we build is the most complex and requires ICs that are not even listed on our component list. We are going to find all the expected outputs for the circuit being properly built, then we are going to introduce an error that has been specified to us and continue to again record the output results. At every instance where we find an output error we will record that problem and talk about what we believe is causing the issue to arise. Again we took the time to introduce an unknown error and allow our lab partner to attempt to diagnose it. Diagnosing the issue took much more time this time around because the circuit was more complex. We found the issue and tried to challenge ourselves by creating an issue that was completely unknown to us.





Pin #	Gate	Expected Out	Observed Out	Where to check
6	U1B	1	0	Pin 5 and 6 (inputs) forU1B - Make sure they are connected correctly
3	U2A	1	1	This Exor gate is ok
6	U3B	0	0	This pin is outputting as expected
6	U2B	0	1	The problem is U1B has the incorrect input coming from U3A instead of the Exor gate U2A
3	U3A	0	0	This IC is outputting as expected

Conclusion: An incorrect connection from U3a to U1B is the source of the issue causing U1B to output a false instead of a true.

W	X	Y	Z	F	G
0	0	0	0	0	0
0	0	0	1	0	0
0	0	1	0	0	0
0	0	1	1	0	0
0	1	0	0	1	1
0	1	0	1	1	1
0	1	1	0	1	0
0	1	1	1	1	1
1	0	0	0	1	1
1	0	0	1	1	1
1	0	1	0	1	0
1	0	1	1	1	0
1	1	0	0	1	1
1	1	0	1	1	1
1	1	1	0	1	0
1	1	1	1	1	1

Circuit troubleshooting challenge for 1st lab partner:

I (Farnam) built circuit 5-5 and tested it for proper output. Then I disconnected the probe from U2A to U3B and instead made a connection from U1A to U3B. Here is Sandra's diagnoses of the problem.

Pin #	Gate	Expected Out	Observed Out	Where to check
6	U1B	0	0	This IC output is good
3	U1A	1	1	This output is ok and not the problem, next
3	U2A	1	1	this output is good
3	U3A	0	0	This is ok
6	U3B	0	0	excellent
6	U2B	1	1	working just fine

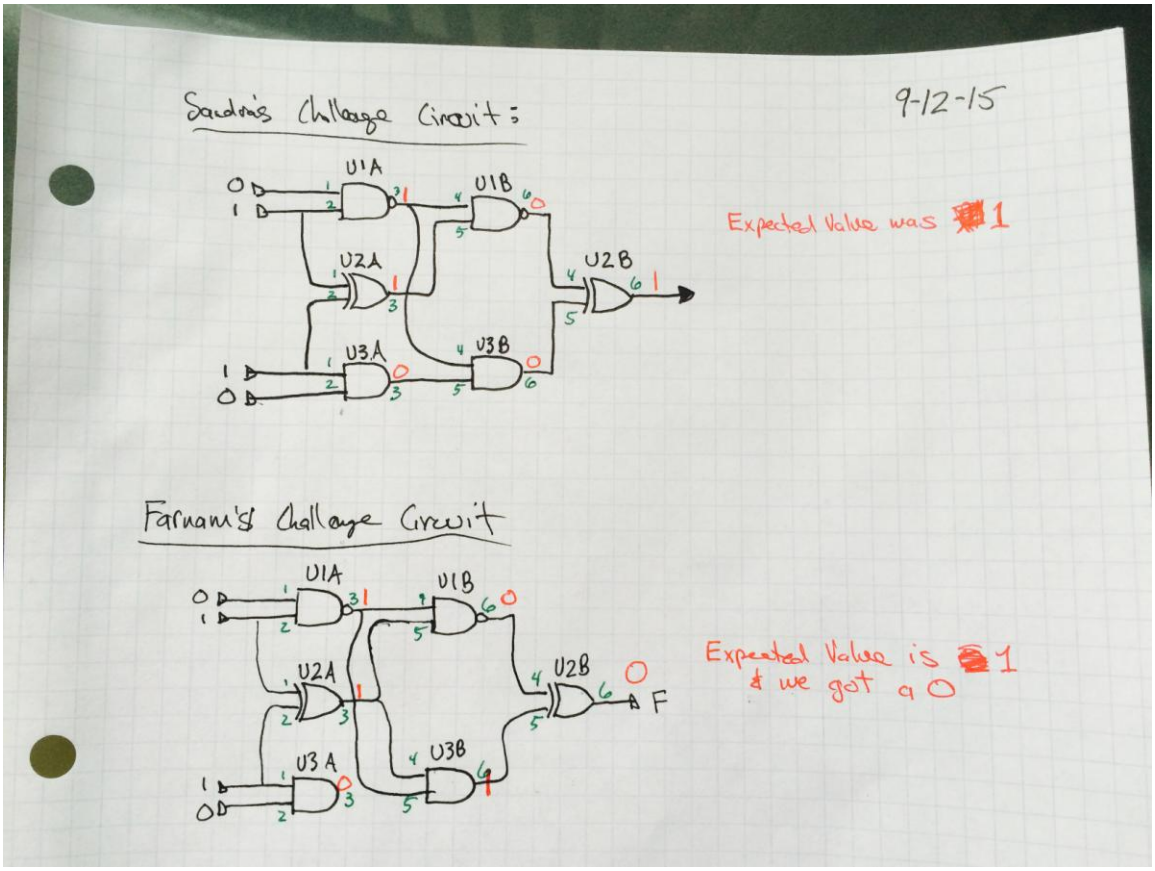
Conclusion: The changes made to this Circuit did not effect the final output at all,
The reason why is because U3B is still getting an 1&0 signal. Which leads to no change in U2B.

Next lab partner. Now Sandra will disconnect the probe from U3A to U3B and instead connect a probe from U1A to U3B and then allow Farnam to diagnose the issue.

Pin #	Gate	Expected Out	Observed Out	Where to check
6	U1B	0	0	Good
6	U3B	0	1	This is bad! Lets check the inputs on U3B
3	U1A	1	1	This pin is sending a 1 to U3B
3	U2A	1	1	This pin is also sending a 1 to U3B

Conclusion: U3B is receiving two true signals and it is an and gate so it is outputing 1.
The desired output is 0 so that U2B can output 0 from a 1&0 input.
Final conclusion: there is a wire misconnection from U1A to U3B.
This wire was disconnected and instead connected to U3A and now everything is working as it should.

The circuit diagrams below represent what changes were made during the challenge diagnoses.



Post lab and Conclusion

In this lab we learned how to troubleshoot our circuits before we begin to assemble them. It is obvious how important and critical it is, both financially and considering our time invested, to diagnose any errors with components before assembly begins. I feel this is a major and important lesson in circuit building. It is absolutely necessary for any circuit designer to know and understand how to properly diagnose issues with the circuits they are assembling. I would not want to hire someone who didn't have circuit diagnostic skills. We learned to be sure that we are bridging our circuits and have everything properly setup. The most important lesson of this lab was to learn and realize that we need to test all of our circuits before beginning assembly. I will only mention that if we are building circuits right after each other then we do not need to test every IC one after another. We will instead build the circuits and test every couple assemblies. This is to save time and money.

The challenge circuits are interesting. It is rewarding to know you can diagnose the issue. Familiarity with the gate truth tables is essential.