Exp. 10: Registers

Engineering 357 - Digital Design Lab

Fall 2015

Farnam Adelkhani
Sandra Hernandez

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Farnam Adelkhani
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Experiment #10

Exp. 10 Registers

Abstract and Objective:

This lab is an introduction to registers. The intention is to practice the design of data storage and shift registers. The lecture has covered registers, what they are and also the functionality of shift registers. Another goal for this lab is to master the operations of a universal shift register and once the experimenters do so they can learn some of the applications of the shift register. Mux can be used to select the correct serial input if a bidirectional shift register is desired. It should be noted that there are registers with built in MUXs, such as the 74LS298.

Ring counters are also covered, which are really not counters but a circular shift register with restricted operations. The restriction to this circuit is that it can only have one circulating in the register. That means that only one FF of the register is on at any given time. The ring counter is really a counter with a built in decoder. Simple ring counters are very susceptible to noise.

Components Used:

- Xilinx software on PC
- The following gates/integrated circuits:
  - D Flip-Flops
  - Dual 4-to-1 Multiplexers
  - 4-bit Universal Shift Registers
  - Other IC might be needed

Procedures and result:

1. This experiment is performed using the EDA software (Xilinx) and therefor planning and testing inputs carefully is required so that the verification process is compact yet complete. Familiarization with the Xilinx software and a good plan for intended circuit design are crucial. Before coming to class these topics are reviewed and these important subjects are rehearsed until the experimenters are comfortable with the required tools, ICs and software.

2. Using a 74LS74As as well as a 74LS153s the experimenters will now design and verify the operations of a4-bit register with a set of predestined capabilities with include:

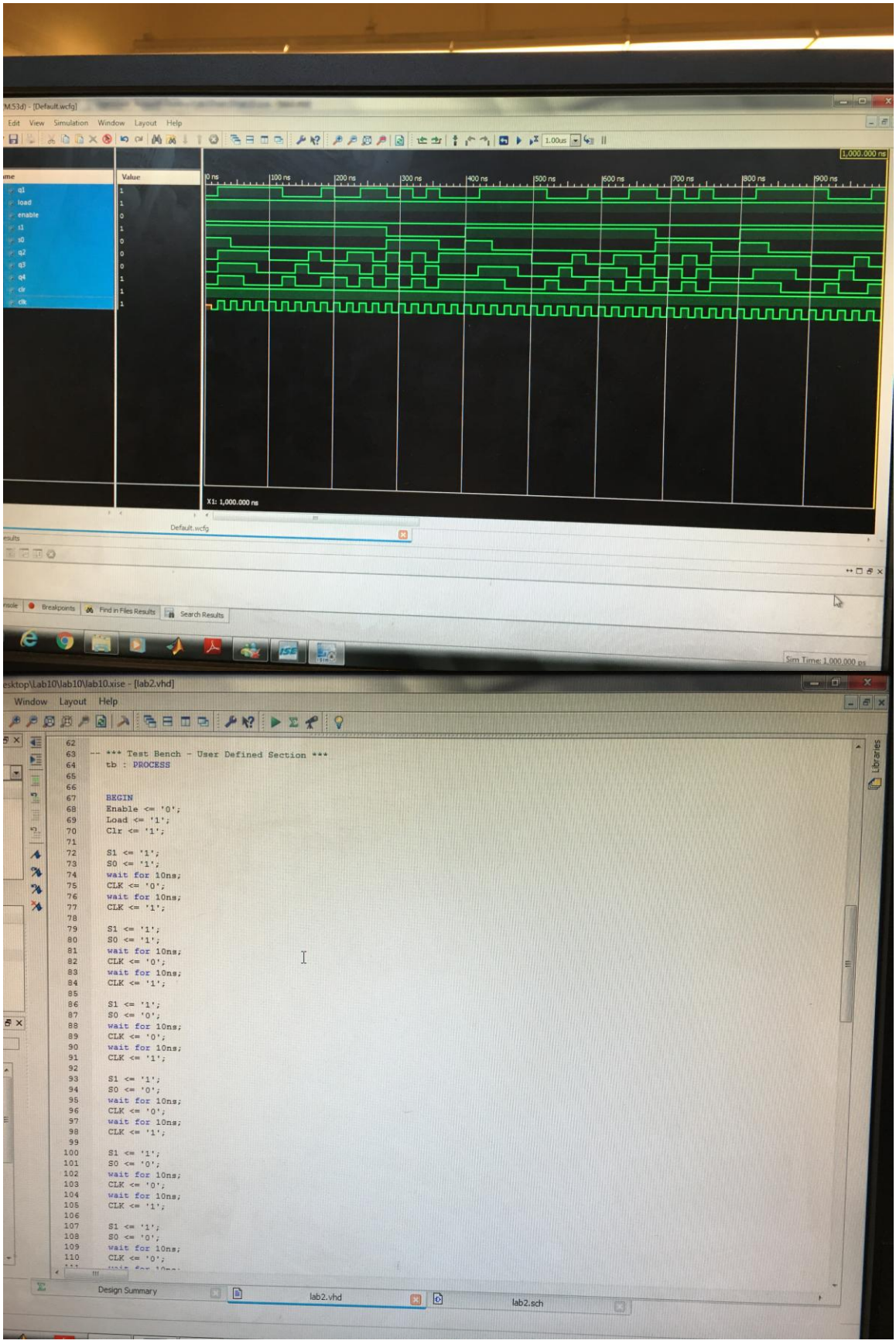
S1	S0	Mode	Operation
0	0	0	no change
0	1	1	1s complement
1	0	2	shift right
1	1	3	parallel load

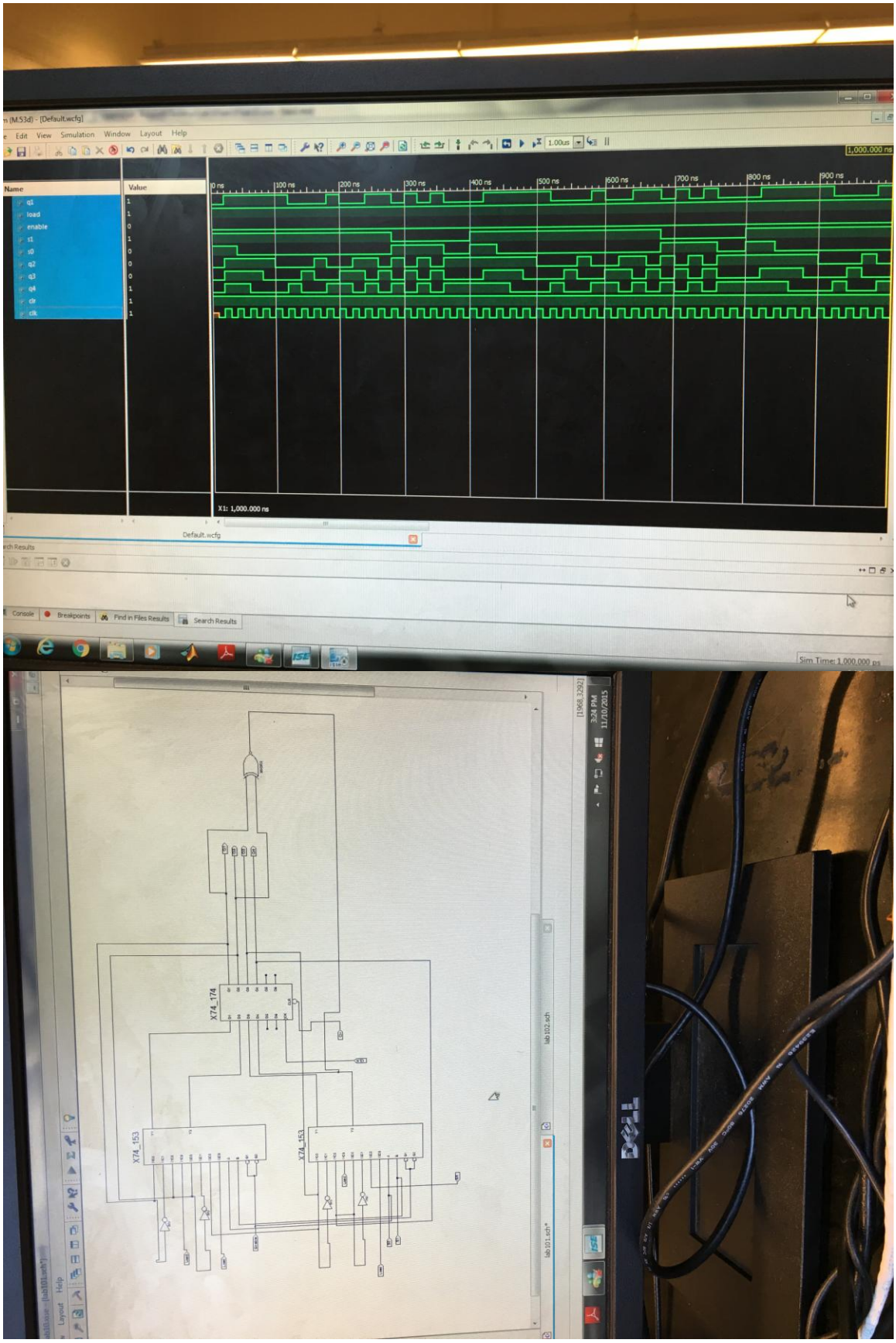
3. In the next step the experimenter is to use the circuit designed and implemented in the previous part with minimal changes to the circuit, to make the shift right operation into a 4-stage linear feedback shift register (while still maintain all other functions). The goal is that starting from the pattern 1000 the experimenter can find what the sequence being generated by the LFSF is. Make sure to show the sequence in the form of a timing diagram as one of your simulation outputs.

4. Next, using two 74LS194As the experimenters are to design and verify the operations of a 8-bit register with the following properties and capabilities:

S1	S0	Mode	Operation
0	0	0	no change
0	1	1	Arithmetic right-shift
1	0	2	rotate (circular shift) left
1	1	3	parallel load

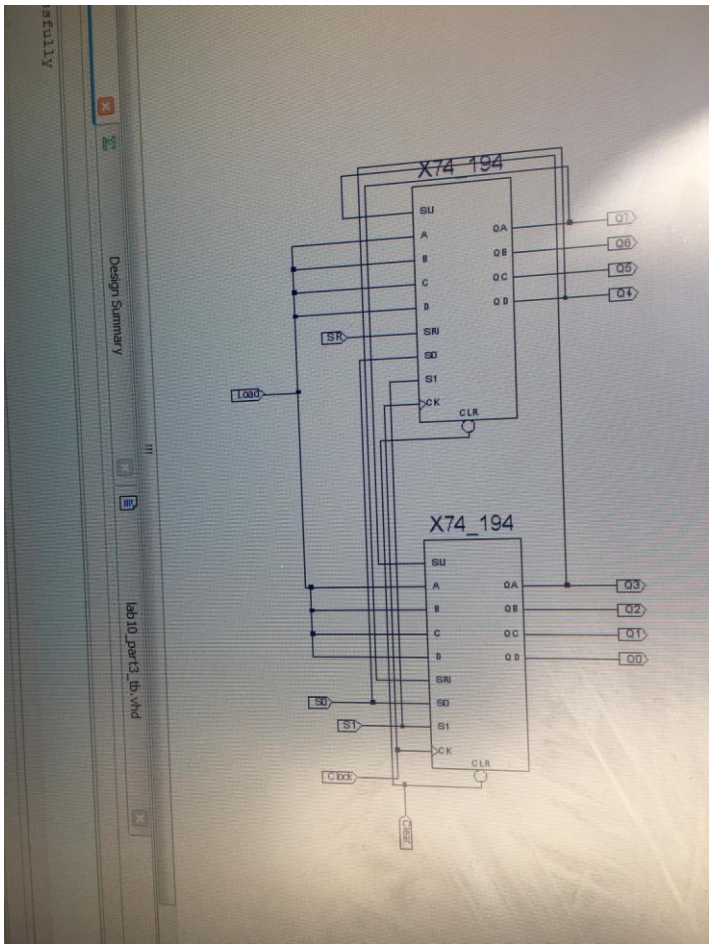
4. Again, in this step the experimenter is to use the circuit designed and implemented in the previous part with minimal changes to the circuit, to make the shift right operation into a 8-bit register (while still maintain all other functions). With minimal changes to the circuit, the rotation operation is to be changes into a self-correcting ring counter. Verify its operations and especially the self-correcting property. Make sure to include a timing diagram showing the pulse distibution feature. The functionality of this circuit was successfully demonstrated to the instructor.

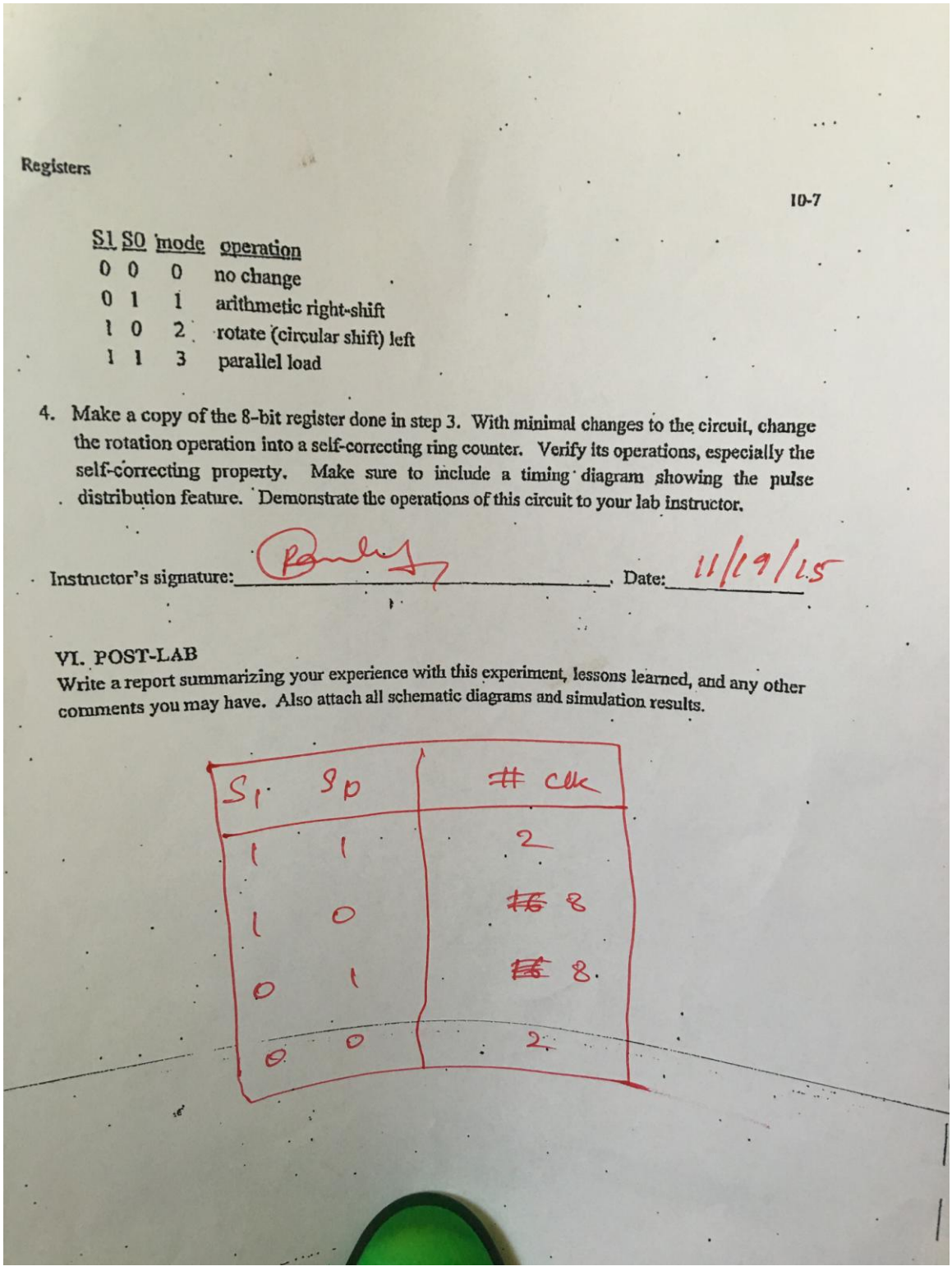

Edit View Simulation Window Layout Help
Value
q1
load
enable
s1
s0
q2
q3
q4
clr
clk
0 ns
100 ns
200 ns
300 ns
400 ns
500 ns
600 ns
700 ns
800 ns
900 ns
1,000.000 ns
X1: 1,000.000 ns
Default.wcfg
Breakpoints
Find in Files Results
Search Results
Window Layout Help
-- *** Test Bench - User Defined Section ***
tb : PROCESS
BEGIN
Enable <= '0';
Load <= '1';
Clr <= '1';
S1 <= '1';
S0 <= '1';
wait for 10ns;
CLK <= '0';
wait for 10ns;
CLK <= '1';
S1 <= '1';
S0 <= '1';
wait for 10ns;
CLK <= '0';
wait for 10ns;
CLK <= '1';
S1 <= '1';
S0 <= '0';
wait for 10ns;
CLK <= '0';
wait for 10ns;
CLK <= '1';
S1 <= '1';
S0 <= '0';
wait for 10ns;
CLK <= '0';
wait for 10ns;
CLK <= '1';
S1 <= '1';
S0 <= '0';
wait for 10ns;
CLK <= '0';
wait for 10ns;
CLK <= '1';
S1 <= '1';
S0 <= '0';
wait for 10ns;
CLK <= '0';
Design Summary
lab2.vhd
lab2.sch
Libraries


Edit View Simulation Window Layout Help
Name
Value
q1
load
enable
s1
s0
q2
q3
q4
clr
clk
0 ns
100 ns
200 ns
300 ns
400 ns
500 ns
600 ns
700 ns
800 ns
900 ns
1,000.000 ns
X1: 1,000.000 ns
Default.wcfg
Console
Breakpoints
Find in Files Results
Search Results
Sim Time: 1,000.000 ns
X74_174
X74_153
X74_153
lab102.sch
lab101.sch*
3:24 PM
11/10/2015

Conclusion and Summary:

So as the experimenters have gained familiarity with register design and implementation of the circuit design while also learning to implement the circuit to perform as an 8-bit register. It is useful to be given data points that can be confirmed by hand in order to confirm our system is working as expected. There are often issues that arise in the Xilinx software itself. You might assume a 10 gb program is free of bugs but not so by any means. Often the best fix is to save the circuit and reload it. I do have some concern that these software issues with Xilinx may become overbearing as a problem once the circuit is much more complex. It is important and vital that the experimenters are gaining familiarity with the Xilinx design suite.





Registers

10-7

S1	S0	mode	operation
0	0	0	no change
0	1	1	arithmetic right-shift
1	0	2	rotate (circular shift) left
1	1	3	parallel load

4. Make a copy of the 8-bit register done in step 3. With minimal changes to the circuit, change the rotation operation into a self-correcting ring counter. Verify its operations, especially the self-correcting property. Make sure to include a timing diagram showing the pulse distribution feature. Demonstrate the operations of this circuit to your lab instructor.

Instructor's signature: _____ Date: 11/19/15

VI. POST-LAB

Write a report summarizing your experience with this experiment, lessons learned, and any other comments you may have. Also attach all schematic diagrams and simulation results.

S_1	S_0	# clk
1	1	2
1	0	~~16~~ 8
0	1	~~16~~ 8
0	0	2

We Demonstrated the design from part 4 and had the test bench verified as being correct but unfortunately forgot to photograph the tb and simulation.