

Xilinx ISE (Version: 12.1)

Basic Tutorial

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Fall 2010
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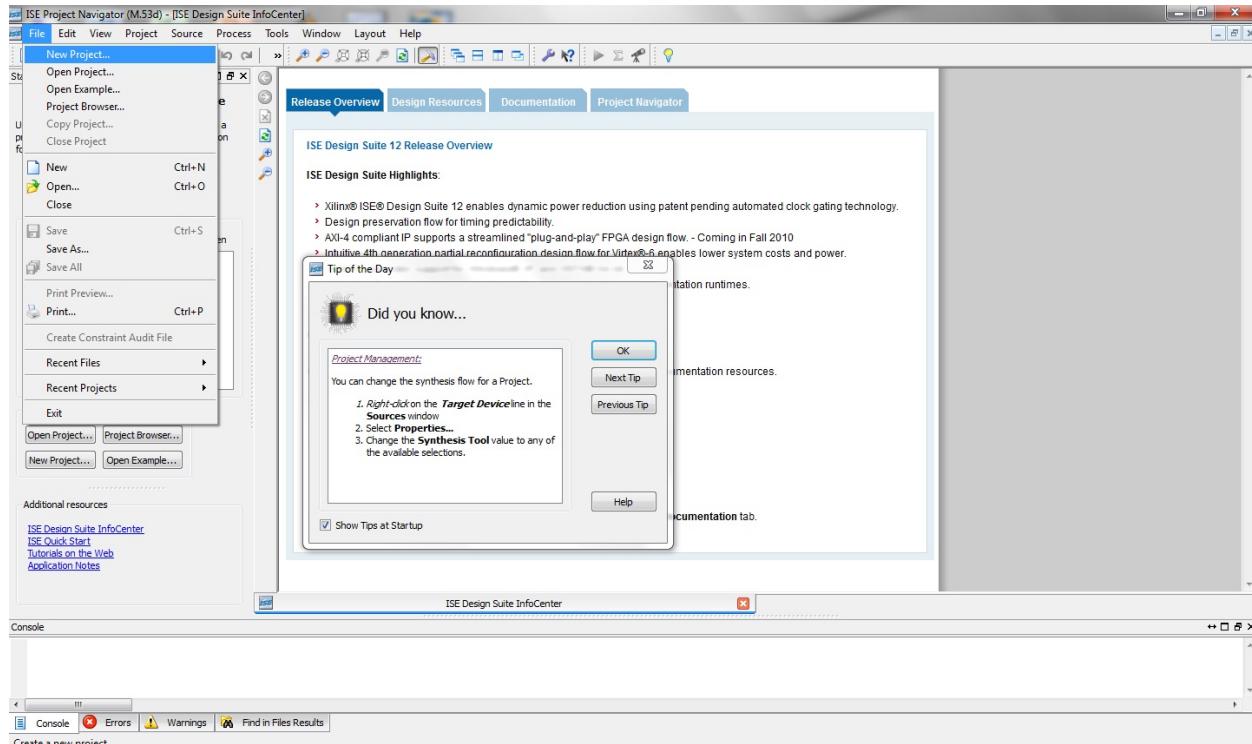
Starting the ISE program



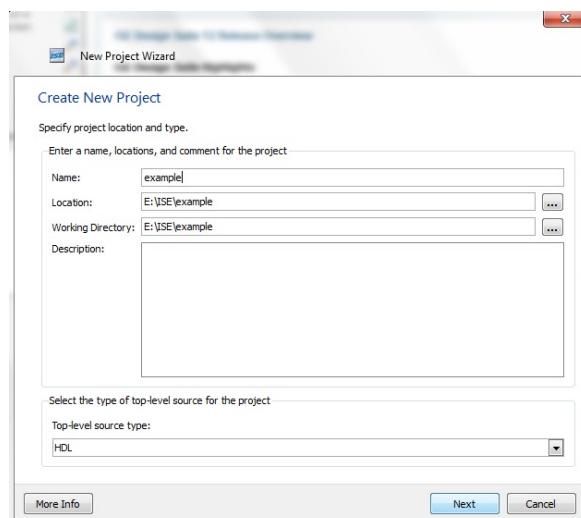
Double click the icon **Xilinx ISE Design Suite...** from desktop.

I. Creating a New Project

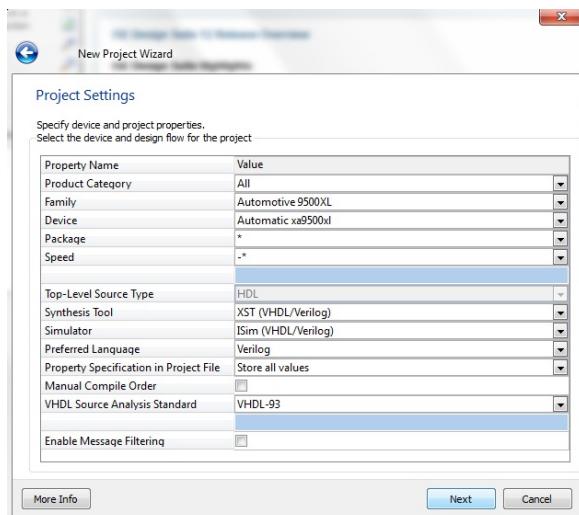
Select **File >> New Project**



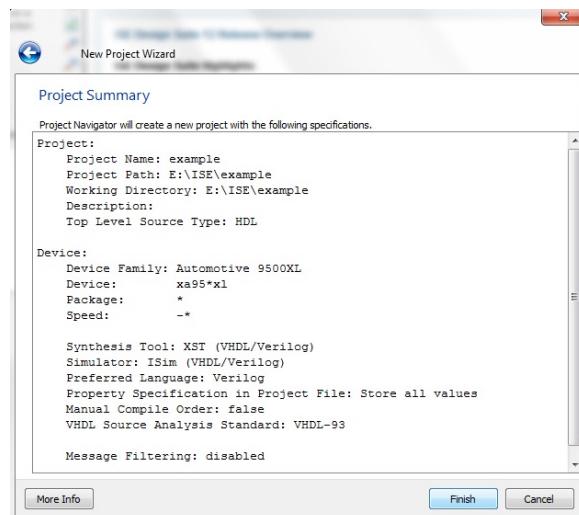
In the **New Project Wizard** dialog box, enter the project **Name** ‘example’ and browse to the desire **Working Directory** (USB drive). And click **Next**.



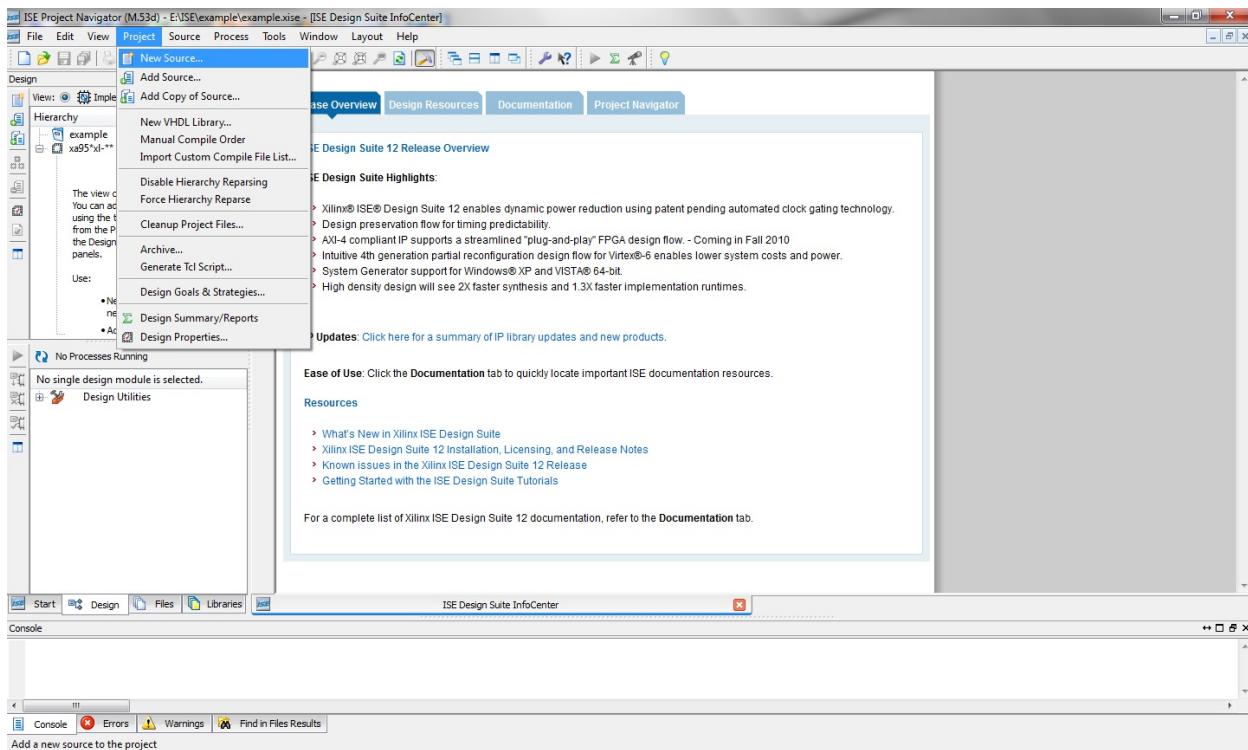
Click Next



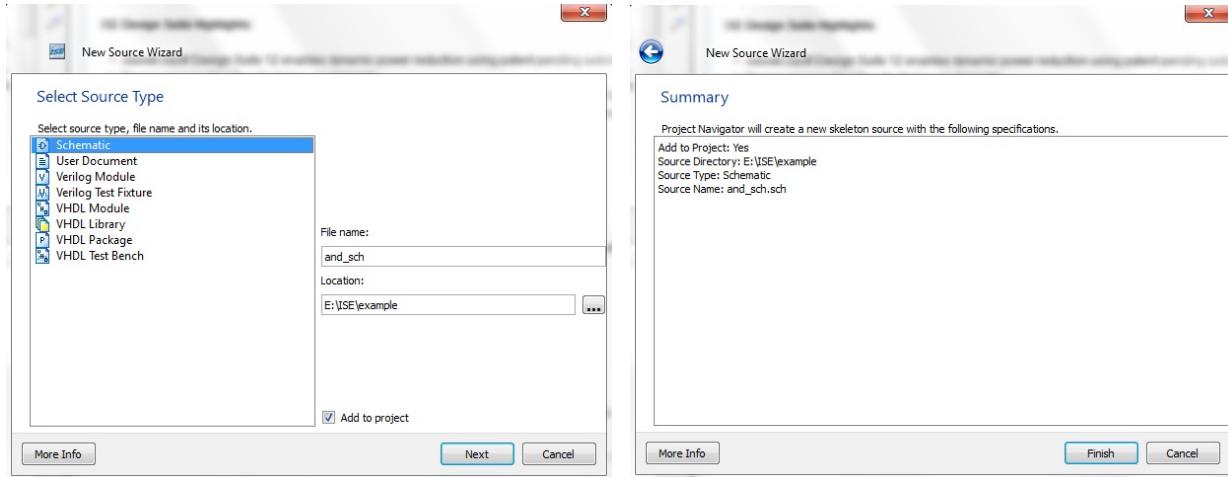
Click Finish



Now from main menu, click on **New Source** to create a new source under **Project**.

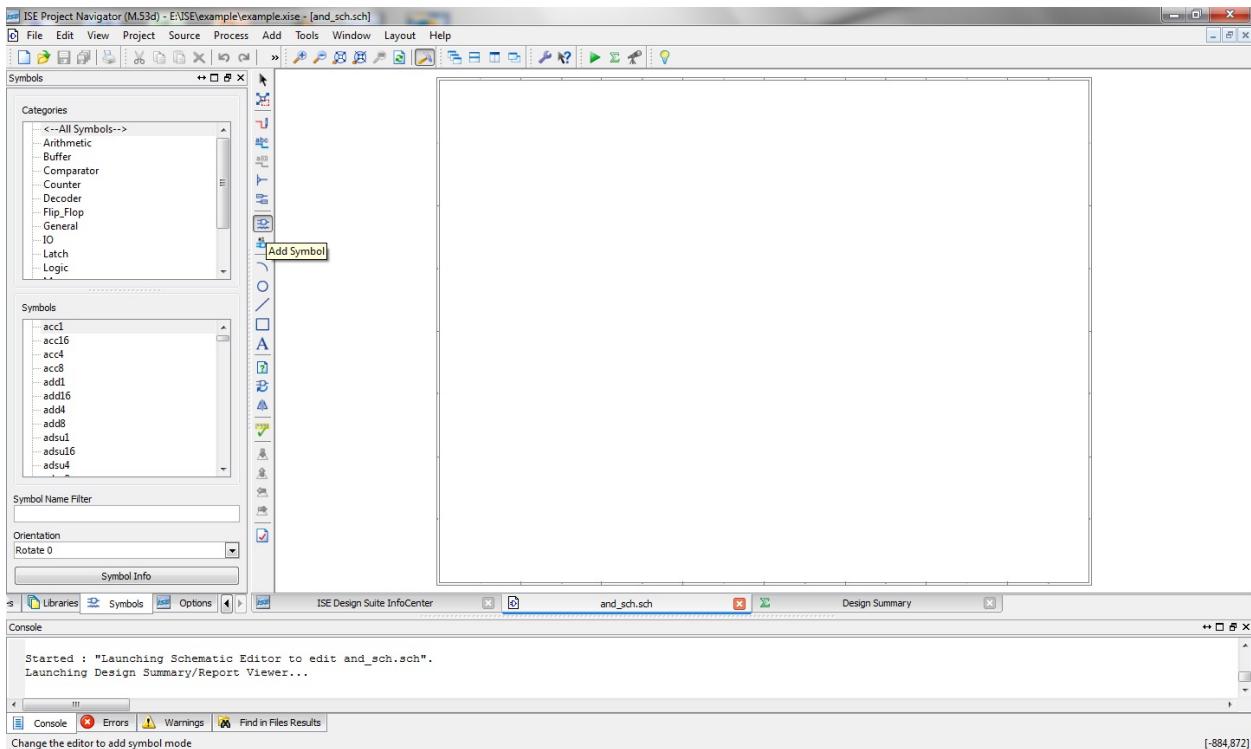


In the **New Source Wizard** dialog box, select **Schematic** from source type. Enter ‘and_sch’ in the **File Name** field. Verify that the Add to project check box is selected. Then click **Next**. In the next window, click **Finish**.

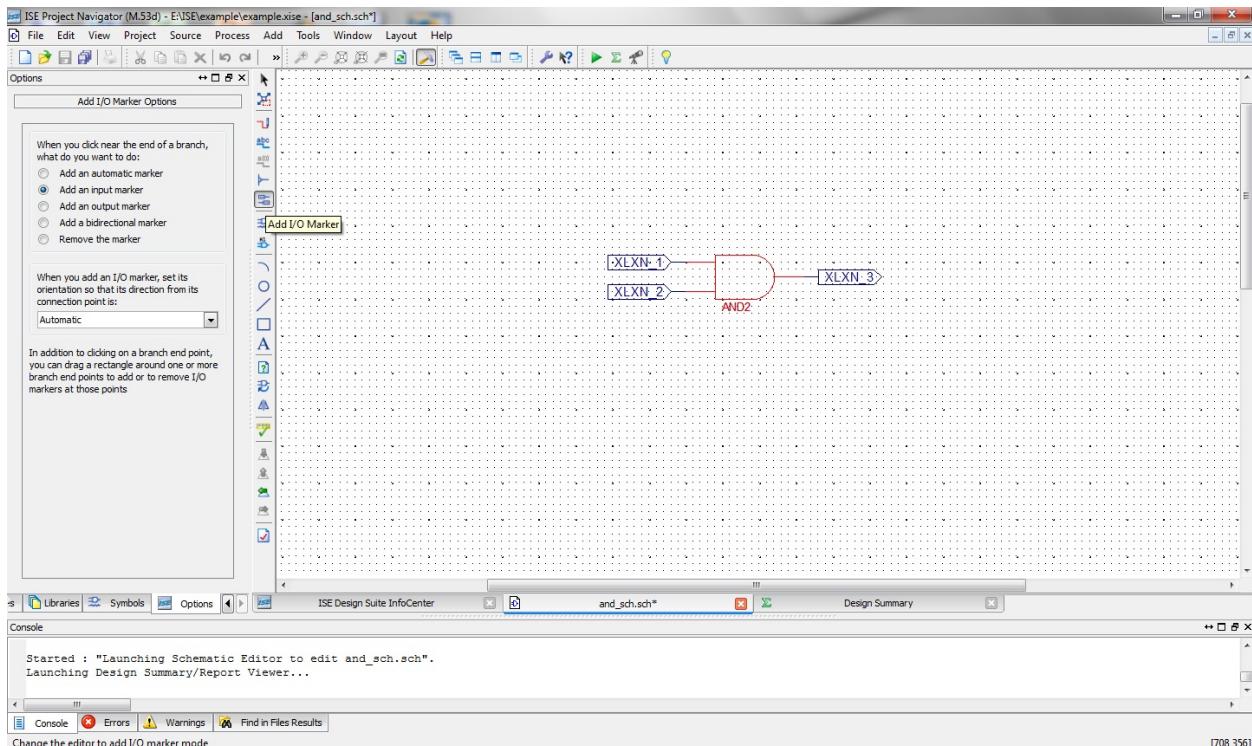


II. Creating Schematics

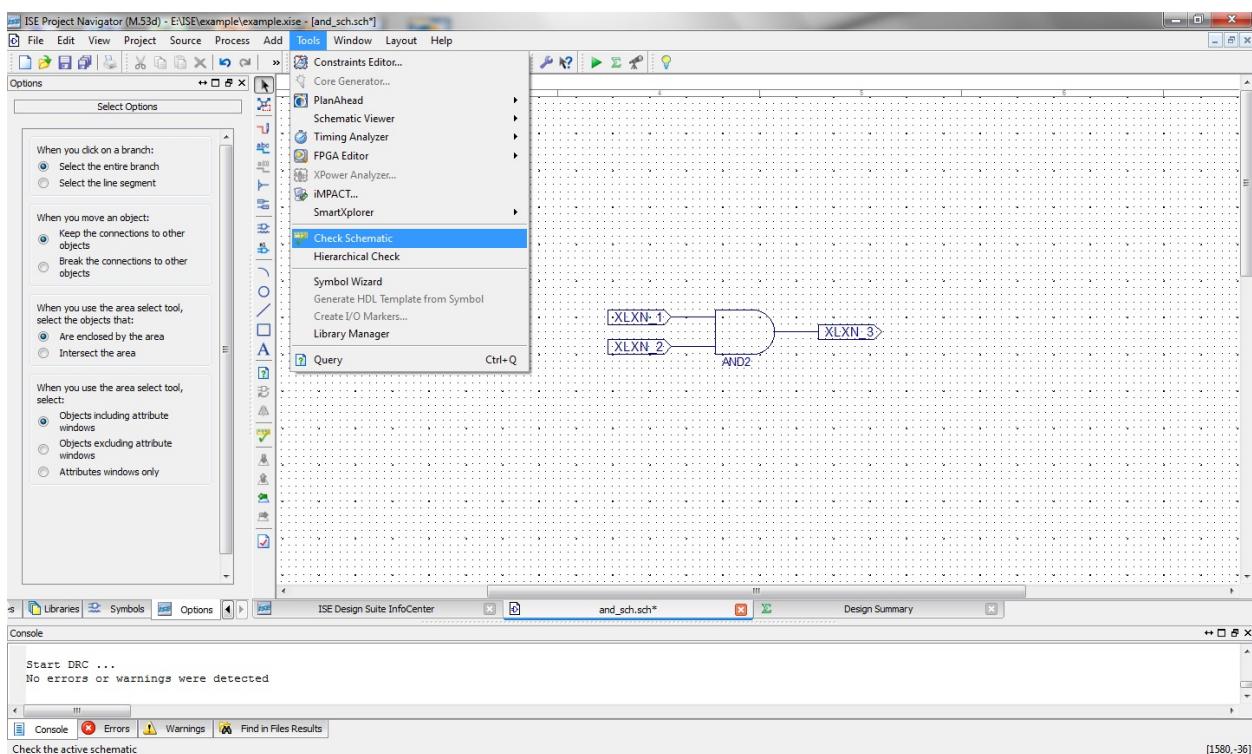
Find the **Add Symbol** icon >> Select **Logic** from Categories >> Select **add2** from Symbols >> Put on the blank schematic sheet on the right.



Find the **Add I/O Marker** icon >> Select **Add an input/ output marker** >> Connect them

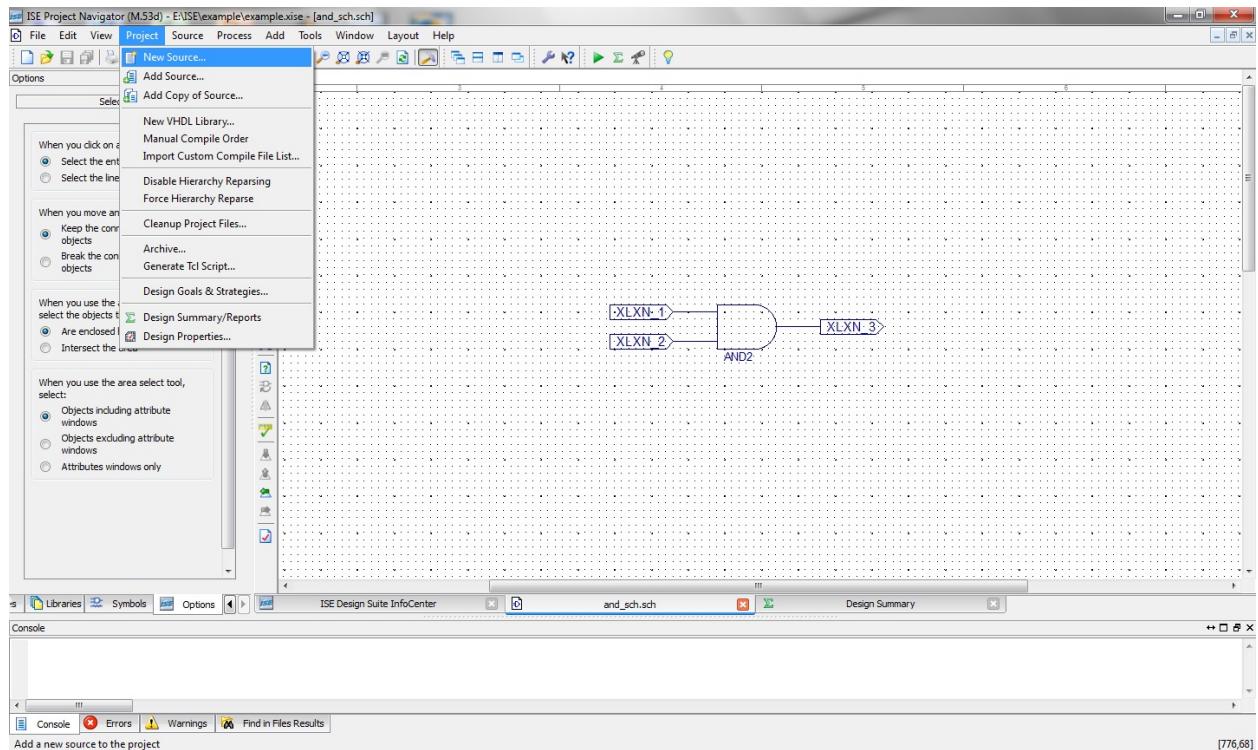


From main menu, click **Check Schematic** under **Tools**, then “No errors or warnings were detected” showing at bottom window and next click **Save** icon.

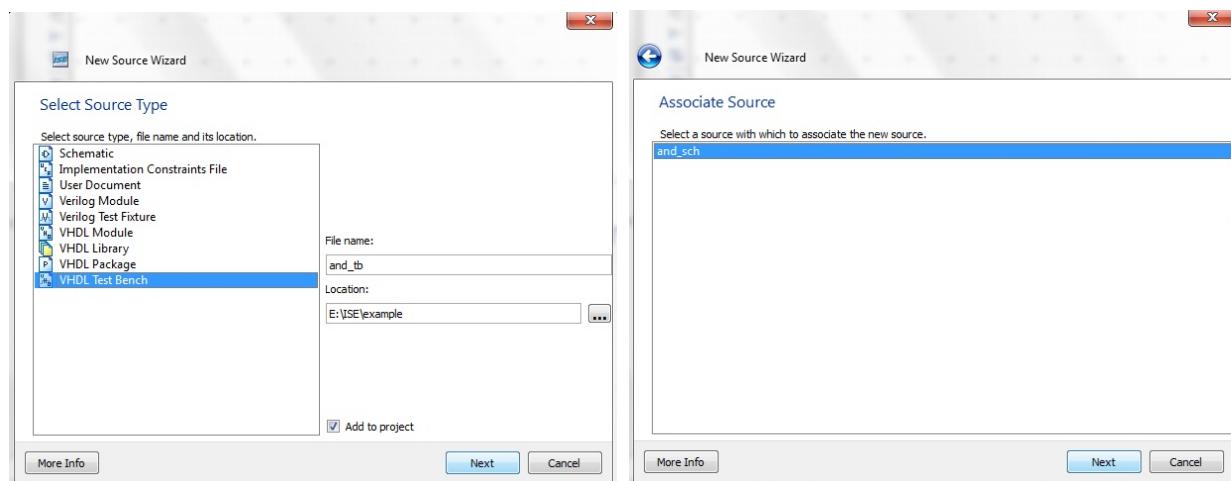


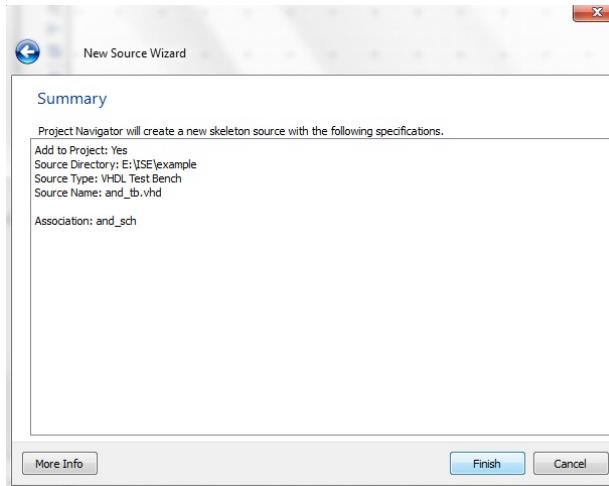
III. Creating VHDL Test Bench

Now from main menu, click on **New Source** to create a new source under **Project**.



In the **New Source Wizard** dialog box, select **VHDL Test Bench** from source type. Enter ‘and_tb’ in the **File Name** field. Verify that the **Add to project** check box is selected. Then click **Next**. In the next window, select the ‘and_sch’ and click **Next >> Finish**.





Write appropriate VHDL code to in the User Defined Section to generate waveform output and Save the file.

```

15 LIBRARY ieee;
16 USE ieee.std_logic_1164.ALL;
17 USE ieee.numeric_std.ALL;
18 LIBRARY UNISIM;
19 USE UNISIM.Vcomponents.ALL;
20 ENTITY and_sch_and_sch_sch_tb IS
21 END and_sch_and_sch_sch_tb;
22 ARCHITECTURE behavioral OF and_sch_and_sch_sch_tb IS
23
24   COMPONENT and_sch
25     PORT( XLXN_1 : IN STD_LOGIC;
26           XLXN_2 : IN STD_LOGIC;
27           XLXN_3 : OUT STD_LOGIC);
28   END COMPONENT;
29
30   SIGNAL XLXN_1 : STD_LOGIC;
31   SIGNAL XLXN_2 : STD_LOGIC;
32   SIGNAL XLXN_3 : STD_LOGIC;
33
34 BEGIN
35
36   UUT: and_sch PORT MAP(
37     XLXN_1 => XLXN_1,
38     XLXN_2 => XLXN_2,
39     XLXN_3 => XLXN_3
40   );
41
42   -- *** Test Bench - User Defined Section ***
43   tb : PROCESS
44   BEGIN
45     WAIT; -- will wait forever ←
46   END PROCESS;
47   -- *** End Test Bench - User Defined Section ***
48
49 END;
50

```

Write VHDL code to
generate output wave
form.

```

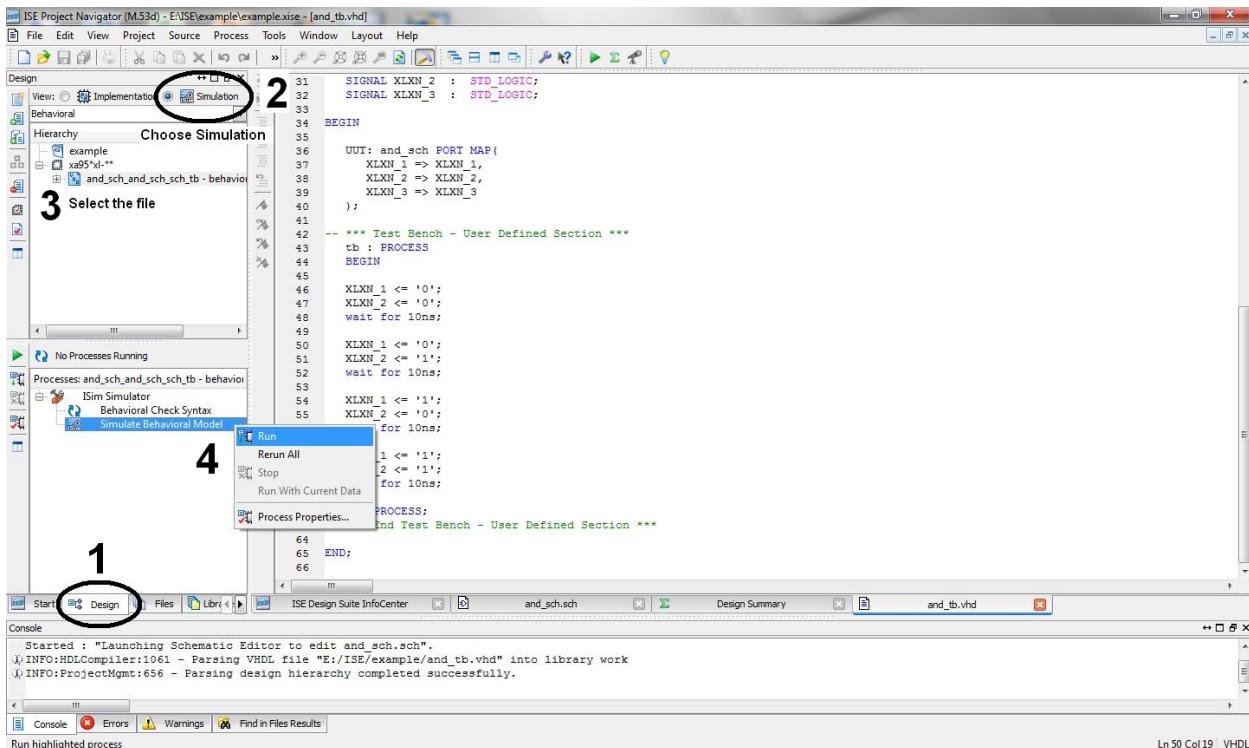
46   XLXN_1 <= '0';
47   XLXN_2 <= '0';
48   wait for 10ns;
49
50   XLXN_1 <= '0';
51   XLXN_2 <= '1';
52   wait for 10ns;
53
54   XLXN_1 <= '1';
55   XLXN_2 <= '0';
56   wait for 10ns;
57
58   XLXN_1 <= '1';
59   XLXN_2 <= '1';
60   wait for 10ns;

```

Define input value
Set up period time

Ln 45 Col 33 VHDL

- 1) Find Hierarchy from Design
- 2) Choose Simulation
- 3) Select the file
- 4) Run Simulate Behavioral Model



IV. Creating Waveform

