```
module NoC (
  input clock,
  input [3:0] src_id,
  input [3:0] dest_id,
  input [7:0] data_in,
  output [7:0] data_out
);
  reg [7:0] mem [0:15][0:15];
  always @(posedge clock) begin
    mem[dest_id][src_id] <= data_in;
  end
  always @(posedge clock) begin
    data_out <= mem[src_id][dest_id];
  end
endmodule
```