```
module ISP_core (
  input clock,
  input [7:0] address,
  input [1:0] rw,
  input [7:0] data_in,
  output [7:0] data_out
);
  reg [7:0] mem [0:255];
  always @(posedge clock) begin
    if (rw == 2'b00) mem[address] <= data_in;
    else if (rw == 2'b01) data_out <= mem[address];
  end
endmodule
```