Design and Implementation of a Multistage BJT Audio Power Amplifier

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1. Objective:

The objective of this project is to design and build a multistage BJT amplifier that can deliver an average power of 100 mW to a 12 Ω loudspeaker by amplifying a low-level microphone signal (10 mV). The amplifier must be built with discrete transistor stages and designed to meet the specifications for proper biasing, impedance matching, voltage gain, and current drive capability. The design emphasizes the use of an appropriate configuration, accurate biasing networks, and coupling parts to ensure that the amplifier achieves the desired gain while retaining signal integrity, low distortion, and stable operation.

2. Design Methodology:

The proposed multistage amplifier is built on a Common-Collector (CC)-Common-Emitter (CE)-Common-Collector (CC)-Common-Collector (CC) topology. This configuration meets the requirements for high input impedance, sufficient voltage gain, and adequate current delivery to a low-impedance load (12 Ω speaker).

The input stage is implemented with a common-collector amplifier, which has a very high input resistance and nearly unity voltage gain. This prevents the amplifier from overloading the microphone source (10 kΩ resistance) while providing current gain and level-shifting to bias the next CE stage. The CC stage also separates the signal source from the rest of the circuit, enhancing overall input matching and stability.

The output average power is given as 100mW, and the output resistance is 12Ω. In order to calculate the output voltage, we will use this formula for power.

$$P = V_{rms} I_{rms}$$

$$= \frac{V_{rms}^2}{R}$$

$$\therefore V_{rms} = \sqrt{P R}$$

$$= \sqrt{100 \times 10^{-3} \times 12}$$

$$= 1.095$$

$\therefore V_{rms} \approx 1.1\text{V}$

This is the output RMS value of the voltage.

At the input side, the peak-to-peak voltage $V_{pk\text{-}pk} = 10\text{mV}$.

$$\therefore V_{rms} = \frac{V_{pk-pk}}{2\sqrt{2}}$$

$$= \frac{10m}{2\sqrt{2}}$$

$$= 3.53\text{mV}$$

$$\therefore \text{Gain } A_v = \frac{1.1}{3.53m} = 311.615 \text{ V/V}$$

Therefore, we must design the amplifier to achieve a 311.615 V/V gain.

For β, we have used 21321007 = 2+1+3+2+1+0+0+7 = 16 x 10 = 160
So, β = 160

$$\alpha = \frac{160}{160+1} = 0.99$$

The common-emitter amplifier is the primary gain stage in the design. Since the surrounding CC stages have near-unity gain, this CE stage must provide almost all of the voltage gain. To achieve the required overall amplifier gain of approximately **311**, the CE stage was designed with a carefully selected collector resistor, bias current, and partially bypassed emitter resistor. The collector bias current was set to 1-2 mA to achieve a balance of high transconductance, acceptable power dissipation, and stable small-signal parameters. A small unbypassed emitter resistance ensures DC stability and linearity, while the remaining emitter resistance is bypassed with a large capacitor to maximise AC gain.

At the output, two additional common-collector stages are used in cascade (Darlington configuration). These stages offer high current gain and low output resistance, enabling the amplifier to drive a 12 Ω speaker load efficiently. The output pair's quiescent bias current was chosen between 10 and 30 mA to reduce crossover distortion while maintaining thermal safety. Small emitter resistors are used in the output transistors to improve current sharing and thermal stability.

To reduce bias sensitivity to transistor β variations, resistive voltage-divider networks are used to bias all transistors. Divider currents are at least ten times the base currents. The supply voltage was set to 15 V to allow for a voltage swing at the output. Inter-stage coupling capacitors are used to block DC offsets while passing the required AC signal.

The CC–CE–CC–CC arrangement provides an effective compromise between gain, input/output impedance requirements, and load-driving capability. The input CC ensures high input resistance and signal integrity, the CE stage delivers the required voltage amplification, and the two CC stages at the output provide sufficient current gain and impedance matching to the low-resistance load. This systematic approach ensures that the amplifier achieves the specified performance while maintaining bias stability, low distortion, and reliable operation under the given design constraints.

3. Design and Analysis:

Whole Circuit picture:

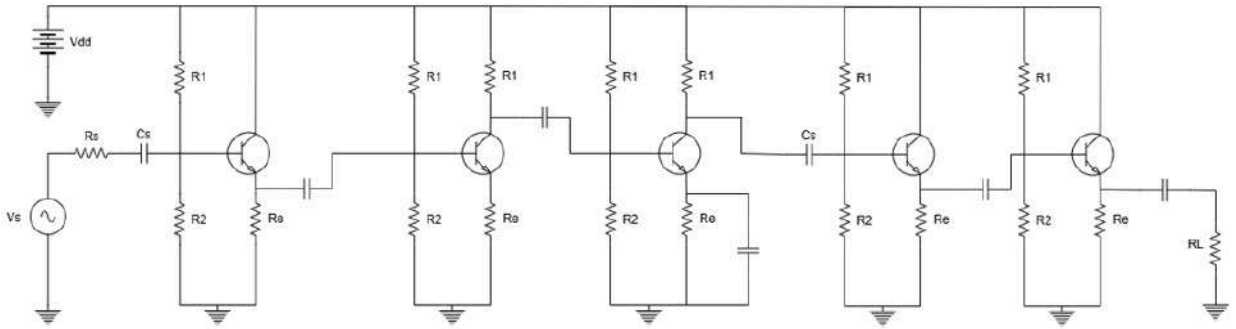


Figure: Whole circuit diagram

Small Equivalent Circuit:

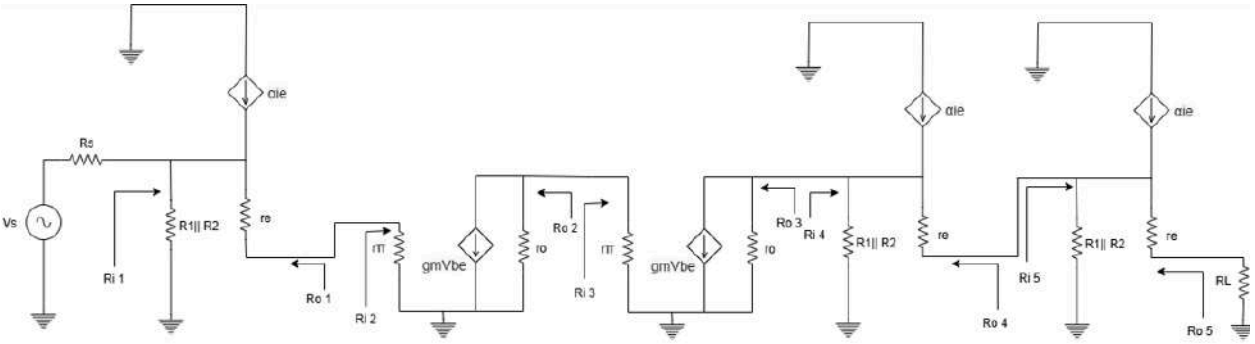


Figure: AC equivalent circuit diagram

Whole Circuit input and output Resistance

Input Resistance	Output Resistance
$R_{i_5} = r_{\pi_5} + (\beta + 1) R_L$	$R_{o_5} = r_{e_5} + \frac{R_{o_4}}{(\beta+1)}$
$R_{i_4} = r_{\pi_4} + (\beta + 1) R_{i_5}$ $= r_{\pi_4} + (\beta + 1) r_{\pi_5} + (\beta + 1) R_L$	$R_{o_4} = r_{e_5} + \frac{R_{o_4}}{(\beta+1)}$
$R_{i_3} = r_{\pi_3}$	$R_{o_3} = r_{o_3}$
$R_{i_2} = r_{\pi_2}$	$R_{o_2} = r_{o_2}$
$R_{i_1} = r_{\pi_1} + (\beta + 1) R_{i_2}$ $= r_{\pi_1} + (\beta + 1) r_{\pi_2}$	$R_{o_1} = r_{e_1} + \frac{R_s}{(\beta+1)}$

Let's assume,
For all Common Collector configurations,

$$I_C = 1mA$$
$$I_B = \frac{I_C}{\beta} = \frac{1m}{160} = 6.25 \times 10^{-6} = 6.25\mu A$$
$$I_C = I_E$$

So,

$$r_e = \frac{V_T}{I_C} = \frac{25m}{1m} = 25\Omega = 0.04$$

$$r_o = \frac{V_A}{I_C} = \frac{100}{1m} = 100000\Omega = 100k\Omega$$

$$g_m = \frac{I_C}{V_T} = \frac{1m}{25m} = 0.04$$

For all Common Emitter configurations,

$$I_C = 0.2mA$$

$$g_m = \frac{I_C}{V_T} = \frac{0.2m}{25m} = 0.008$$

$$r_{o_3} = \frac{V_A}{I_C} = \frac{100}{0.2m} = 500k$$

So, resistance calculations are,

Input Resistance

$$R_{i_1} = r_{\pi_1} + (\beta + 1) r_{\pi_2}$$
$$= \frac{25\times10^{-3}}{6.25\times10^{-6}} + (160+1)\frac{25\times10^{-3}}{6.25\times10^{-6}}$$
$$= 648000\Omega$$
$$= 648k\Omega$$

$$R_{i_2} = r_{\pi_2}$$
$$= \frac{25\times10^{-3}}{6.25\times10^{-6}}$$
$$= 4000\Omega$$
$$= 4k\Omega$$

$$R_{i_3} = r_{\pi_3}$$
$$= \frac{25\times10^{-3}}{6.25\times10^{-6}}$$
$$= 4000\Omega$$
$$= 4k\Omega$$

$$R_{i_4} = r_{\pi_4} + (\beta + 1) R_{i_5}$$
$$= \frac{25\times10^{-3}}{6.25\times10^{-6}} + (160+1)\times5932\ \Omega$$
$$= 959052\Omega \approx 960k\Omega$$

$$R_{i_5} = r_{\pi_5} + (\beta + 1) R_L$$
$$= \frac{V_T}{I_B} + (160 + 1)12$$

Output Resistance

$$R_{o_1} = r_{e_1} + \frac{R_s}{(\beta+1)}$$
$$= 25 + \frac{10\times10^3}{(160+1)}$$
$$= 87.11\Omega$$

$$R_{o_2} = r_{o_2}$$
$$= 100k\Omega$$

$$R_{o_3} = r_{o_3}$$
$$= 100k\Omega$$

$$R_{o_4} = r_{e_5} + \frac{R_{o_3}}{(\beta+1)}$$
$$= 25 + \frac{100\times10^3}{(160+1)}$$
$$= 646.11\Omega$$

$$R_{o_5} = r_{e_5} + \frac{R_{o_4}}{(\beta+1)}$$

$$= \frac{25\times10^{-3}}{6.25\times10^{-6}} + (160 + 1)12$$

$$= 5932\ \Omega \approx 5.9k\Omega$$

$$= 25 + \frac{646.11}{(160+1)}$$

$$= 29.01\Omega$$

For the input stage, we use a common collector amplifier. A common collector amplifier has the highest input resistance among all the configurations, and it has a unity voltage gain.

Now, if we want to go for a stage-by-stage calculation, for the input stage, we used a common collector amplifier configuration as it has the highest input resistance among all the other configurations, and the voltage gain is almost unity, so it will not affect the overall gain of the entire circuit.

Input Stage

For input single-stage CC,

For Common Collector Amplifiers, the voltage gain is unity or ~1.
DC analysis,

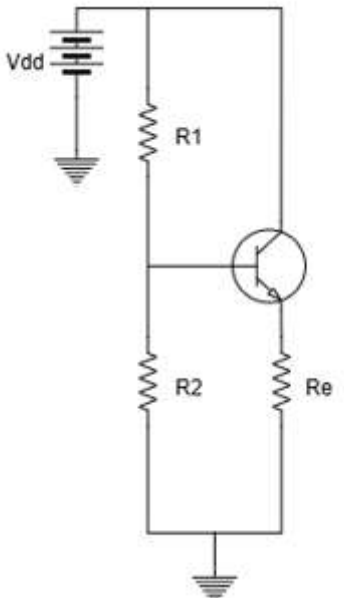


Figure: DC biasing Circuit for CC configuration.

Let us assume, I_C= 1mA

$\therefore I_E = \frac{I_C}{\alpha} = \frac{1m}{0.9937}$ = 1.00625 mA

As a rule of thumb, $V_E = \frac{1}{2} V_{CC} = 7.5\text{V}$

So,

$V_C = V_E + 0.7 = 8.2$

$\therefore R_E = \frac{V_E}{I_E} = \frac{7.5}{1m} = 7.5\text{k}\Omega$

Base Current $I_B = \frac{I_c}{\beta}$

$I_B = \frac{1m}{160}$

$= 6.25\mu A$

Make divider current $\approx 10\times I_B$ for stiffness $\rightarrow I_{div} \approx 62.5\ \mu A$

So,

Total divider resistance: $R_{total} = \frac{Vcc}{I_{div}}$

$= \frac{15\ V}{62.5\ \mu A} = 240\text{k}\Omega$

Then,

$R_2 = \frac{V_B}{V_{CC}} \times R_{total}$

$= \frac{8.2}{15} \times 240k$

$= 131200\Omega$

$\approx 131k\Omega$

$R_1 = R_{total} - R_2$

$= 240k - 131k$

$= 109k\Omega$

Now we observe the AC parameters value, which are dependent on the DC components.
Small Signal

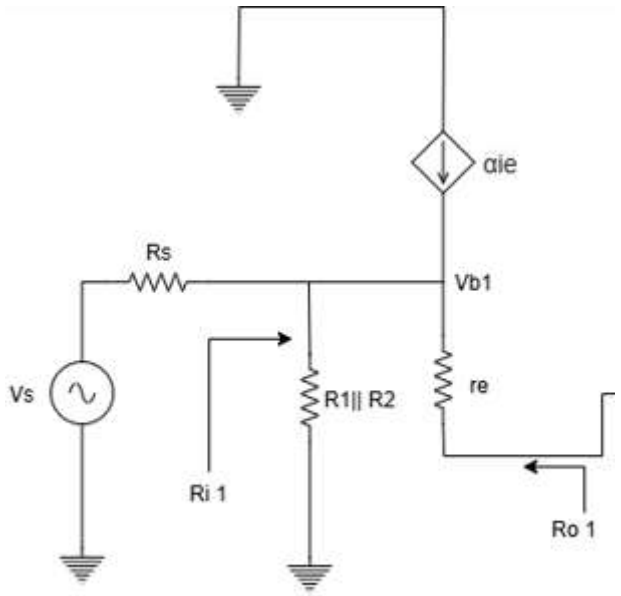


Figure: AC Equivalent Circuit for CC configuration.

Input Resistance, R_i $= (\beta+1)(r_e + R_L)$

$= (\beta+1)r_e + (\beta+1)R_L$

$= r_\pi + (\beta+1)R_L$

Output Resistance, $R_o = r_e + \frac{R_S}{(\beta+1)}$

Here, $\frac{R_S}{(\beta+1)} = \sim \Omega$, is the region of a few ohms only, and r_e is also very small, so the total output resistance is very low.

Calculations with the given value

Voltage Gain, $A_v = \frac{V_o}{V_S} = \frac{V_o}{V_b} \cdot \frac{V_b}{V_S}$

Here,

$V_b = i_e (r_e + R_L)$

$V_o = i_o R_L = i_e R_L$

$\frac{V_o}{V_b} = \frac{i_e R_L}{i_e (r_e + R_L)} = \frac{R_L}{r_e + R_L}$

$\frac{V_b}{V_s} = \frac{R_i}{R_i + R_S}$ [Using Voltage Division Rule]

$$\therefore A_{vi} = \frac{V_o}{V_b} \cdot \frac{V_b}{V_S} = \frac{R_L}{r_e + R_L} \cdot \frac{R_i}{R_i + R_S}$$
$$= \frac{R_{i_5}}{r_{e_5} + R_{i_5}} \cdot \frac{R_i}{R_i + R_S}$$
$$= \frac{4000}{25 + 4000} \cdot \frac{648k}{648k + 10k}$$
$$= 0.99 \cdot 0.98 = 0.97 < 1$$

Gain Stage:

We are using two CE amplifiers in the gain part. Let's do a single-stage CE amplifier breakdown first.

Our expected gain is around 311.
It is very hard to get this much gain from a single-stage amplifier, so we are using two CE stages
So, Av for each CE would be,

$$Av = \sqrt{311} = 17.63 \approx 18$$

We know for CE gain. $Av = -g_{m_1}(r_o \,||\, R_L)$

$$= -g_{m_1}(R_L) \qquad [r_o >> R_L]$$

So,

$$18 = -g_{m_1}(R_L)$$

In our case, R_L of the first CE amplifier is R_{i_3}. From the previous calculation. We got

$R_{i_3} = 4k\Omega$

So,

$$18 = -g_{m_1}(R_{i_3})$$
$$18 = -\frac{I_C}{V_T}(4000)$$
$$4.55 \times 10^{-3} = \frac{I_C}{25 \times 10^{-3}}$$
$$I_C = 0.14\text{mA}$$

So, let's assume I_C = 0.2mA

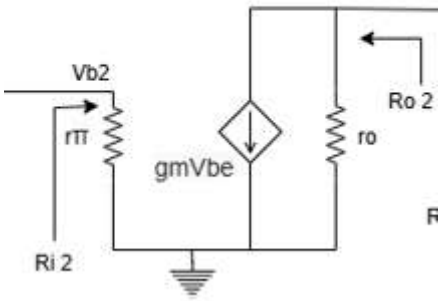
For the First CE amplifier circuit:

AC Equivalent Circuit of 1st CE amplifier,
Here,

$$I_C = 0.2mA$$

$$g_m = \frac{I_C}{V_T} = \frac{0.2m}{25m} = 0.008$$

$$r_{o_3} = \frac{V_A}{I_C} = \frac{100}{0.2m} = 500k$$



Input Resistance, $R_i = r_\pi$

Output Resistance, $R_o = r_o$

Voltage Gain, $A_v = \frac{V_o}{V_S} = \frac{V_o}{V_b} \cdot \frac{V_b}{V_S}$

Here,

$V_b = v_{be}$

$V_o = -g_m v_{be}(r_o \parallel R_L)$

$$\frac{V_o}{V_b} = \frac{-g_m v_{be}(r_o \parallel R_L)}{v_{be}} = -g_m(r_o \parallel R_L)$$

$\frac{V_b}{V_s} = \frac{r_\pi}{r_\pi + R_S}$ [Using Voltage Division Rule]

$\therefore A_v = \frac{V_o}{V_b} \cdot \frac{V_b}{V_S} = -g_m(r_o \parallel R_L) \cdot \frac{r_\pi}{r_\pi + R_S}$

Calculations with the given value

$$A_{vg1} = \frac{V_o}{V_b} \cdot \frac{V_b}{V_S} = -\ g_m(r_o \parallel R_L) \cdot \frac{r_\pi}{r_\pi + R_S}$$
$$= -\ g_m(r_o \parallel R_L) \left[\frac{r_\pi}{r_\pi + R_S}\ is\ nothing\ but\ attenuation\right]$$

So, in the gain stage first CE amplifier.

$\frac{V_{b_3}}{V_2} = -\ g_{m_1}(r_{o_3} \parallel R_{i_3})$

Here,

I_c=0.20m

g_m= 0.008

$r_{o_2} = 500k$

So,

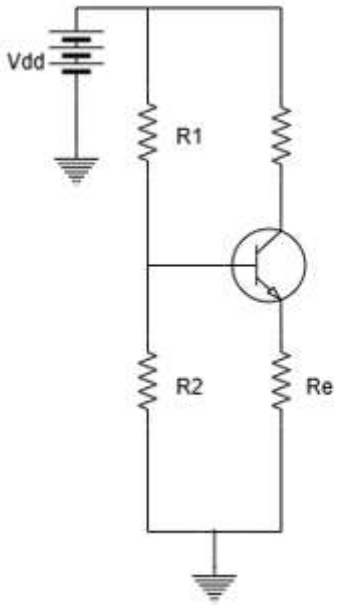
$\frac{V_{b_3}}{V_{b_2}} = -\ g_{m_2}(r_{o_2} \parallel R_{i_2})$

$= -0.008\ R_{i_2}$ $(r_{o_2} >> R_{i_2})$

$= -0.008 \times 4k$

$= -\ 32$

DC biasing of Common Emitter Amplifier,



Here,
V_{CC} = 15V
I_C = 0.2mA
β = 160
From the AC equivalent circuit we got,
$|Av| = 32$
Approximate CE amplifier gain Av= - $g_{m_1}(R_c)$

$$R_c = \frac{32}{gm} = 4k$$
$$V_{RC} = IC \cdot RC = 0.2mA \times 4k\Omega = 0.8V$$

So,

$$V_c = Vcc - V_{RC} = 15 - 0.8 = 14.2V$$
$$VE \approx 14.2 - 7.5 = 6.7V$$
$$R_E = \frac{V_E}{I_E} \approx \frac{6.7}{0.2m} \approx 33.5k\Omega$$

Now,

$V_B = V_E + 0.7 = 6.7 + 0.7$
$= 7.4V$
$I_B = \frac{I_C}{\beta}$
$= \frac{0.2m}{160}$
$= 1.25\mu A$

We take the $Take\ divider\ current \approx 10\times I_B = 12.5\,\mu A$.

$$R_{th} = \frac{V_{CC}}{I_{div}} = \frac{15}{12.5\times10^{-6}}$$

$$= 1.2\text{M}\Omega$$

$$R_2 = \frac{V_B}{V_{CC}} R_{th} = 592k\Omega$$

$$R_1 = R_{th} - R_2 = 1.2M - 592k$$

$$\approx 608k\Omega$$

For the second CE amplifier circuit

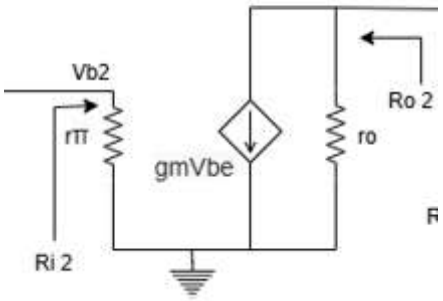
AC Equivalent Circuit,

Here,

$$I_C = 0.2mA$$

$$g_m = \frac{I_C}{V_T} = \frac{0.2m}{25m} = 0.008$$

$$r_{o_3} = \frac{V_A}{I_C} = \frac{100}{0.2m} = 500k$$



Input Resistance, $R_i = r_\pi$

Output Resistance, $R_o = r_o$

Voltage Gain, $A_v = \frac{V_o}{V_S} = \frac{V_o}{V_b} \cdot \frac{V_b}{V_S}$

Here,

$V_b = v_{be}$

$V_o = -g_m v_{be}(r_o \parallel R_L)$

$$\frac{V_o}{V_b} = \frac{-g_m v_{be}(r_o \parallel R_L)}{v_{be}} = -g_m(r_o \parallel R_L)$$

$$\frac{V_b}{V_s} = \frac{r_\pi}{r_\pi + R_S}$$ [Using Voltage Division Rule]

$$\therefore A_v = \frac{V_o}{V_b} \cdot \frac{V_b}{V_S} = -g_m(r_o \parallel R_L) \cdot \frac{r_\pi}{r_\pi + R_S}$$

Calculations with the given value

$$A_{vg2} = \frac{V_o}{V_b} \cdot \frac{V_b}{V_S} = -\ g_m(r_o \parallel R_L) \cdot \frac{r_\pi}{r_\pi + R_S}$$

$$= -\ g_m(r_o \parallel R_L) \left[\frac{r_\pi}{r_\pi + R_S}\ is\ nothing\ but\ attenuation\right]$$

So, in the gain stage first CE amplifier.

$$\frac{V_{b_4}}{V_{b_3}} = -\ g_{m_1}(r_{o_3} \parallel R_{i_3})$$

Here,

I_c=0.20m

g_m= 0.008

$r_{o_3} = 500k$

So,

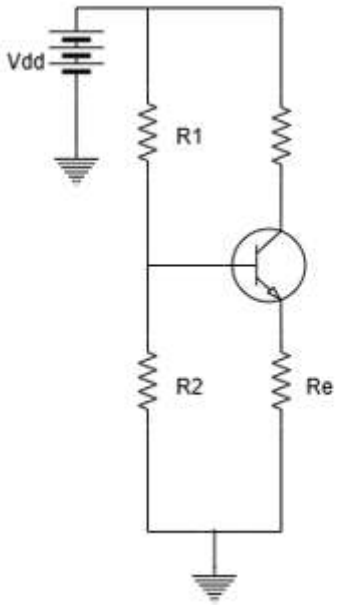
$$\frac{V_{b_4}}{V_{b_3}} = -\ g_{m_2}(r_{o_3} \parallel R_{i_3})$$

$= -0.008\ R_{i_3}$ $(r_{o_3} >> R_{i_3})$

$= -0.008 \times 4k$

$= -\ 32$

DC biasing of Common Emitter Amplifier,



Here,
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From the AC equivalent circuit we got,
$|Av| = 32$
Approximate CE amplifier gain Av= - $g_{m_1}(R_c)$

$$R_c = \frac{32}{gm} = 4k$$
$$V_{RC} = IC \cdot RC = 0.2mA \times 4k\Omega = 0.8V$$

So,

$$V_c = Vcc - V_{RC} = 15 - 0.8 = 14.2V$$
$$VE \approx 14.2 - 7.5 = 6.7V$$
$$R_E = \frac{V_E}{I_E} \approx \frac{6.7}{0.2m} \approx 33.5k\Omega$$

Now,

$V_B = V_E + 0.7 = 6.7 + 0.7$
$= 7.4V$
$I_B = \frac{I_C}{\beta}$
$= \frac{0.2m}{160}$
$= 1.25\mu A$

We take the $Take\ divider\ current \approx 10\times I_B = 12.5\,\mu A$.

$$R_{th} = \frac{V_{CC}}{I_{div}} = \frac{15}{12.5\times10^{-6}}$$

$$= 1.2\text{MΩ}$$

$$R_2 = \frac{V_B}{V_{CC}} R_{th} = 592k\Omega$$

$$R_1 = R_{th} - R_2 = 1.2M - 592k$$

$$\approx 608k\Omega$$

Output Stage:

We are using two CC amplifiers in the output. Same as the input stage, let us assume I_C= 1mA

$\therefore I_E = \frac{I_C}{\alpha} = \frac{1m}{0.9937}$ = 1.00625 mA

So, **the DC biasing Circuit for the output stage will be the same as before (input Stage).**

So,

First CC amplifier Circuit:

AC equivalent Circuit:

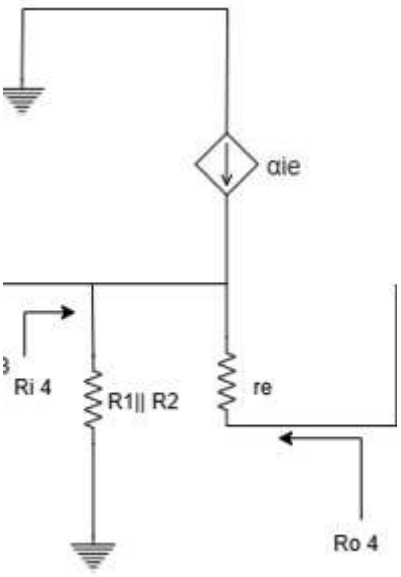


Figure: AC Equivalent Circuit for CC configuration.

Input Resistance, R_i = (β+1)(r_e+ R_L)

$$R_{i_4} = r_{\pi_4} + (\beta + 1) R_{i_5}$$
$$= \frac{25\times10^{-3}}{6.25\times10^{-6}} + (160+1)\times5932\ \Omega$$
$$= 959052\Omega \approx 960k\Omega$$

Output Resistance, $R_o = r_e + \frac{R_S}{(\beta+1)}$

$$R_{o_4} = r_{e_5} + \frac{R_{o_3}}{(\beta+1)}$$
$$= 25 + \frac{100\times10^3}{(160+1)}$$
$$= 646.11\Omega$$

Here, $\frac{R_S}{(\beta+1)}$ is in the region of a few ohms only, and r_e is also very small, so the total output resistance is very low.

Calculations with the given value

Voltage Gain, $A_v = \frac{V_o}{V_S} = \frac{V_o}{V_b} \cdot \frac{V_b}{V_S}$

Here,

$V_b = i_e (r_e + R_L)$

$V_o = i_o R_L = i_e R_L$

$\frac{V_o}{V_b} = \frac{i_e R_L}{i_e (r_e + R_L)} = \frac{R_L}{r_e + R_L}$

$\frac{V_b}{V_s} = \frac{R_i}{R_i + R_S}$ [Using Voltage Division Rule]

$\therefore A_{vi} = \frac{V_o}{V_b} \cdot \frac{V_b}{V_S} = \frac{R_L}{r_e + R_L} \cdot \frac{R_i}{R_i + R_S}$

$= \frac{R_{i_5}}{r_{e_5} + R_{i_5}} \cdot \frac{R_{i_4}}{R_{i_4} + R_{o_3}}$

$= \frac{5.9k}{25 + 5.9k} \cdot \frac{960k}{960k + 646.11}$

$= 0.995 \cdot 0.999 = 0.994 < 1$

The DC biasing Circuit for the output stage will be the same as before (input Stage), and it is shown in the input stage.

Second CC amplifier Circuit:

Second AC equivalent Circuit:

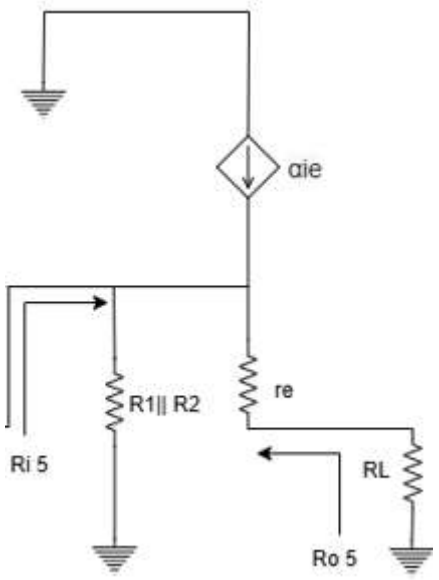


Figure: AC Equivalent Circuit for CC configuration.

Input Resistance, $R_i = (\beta+1)(r_e + R_L)$

$$R_{i_5} = r_{\pi_5} + (\beta + 1) R_L$$

$$= \frac{V_T}{I_B} + (160 + 1)12$$

$$= \frac{25\times10^{-3}}{6.25\times10^{-6}} + (160 + 1)12$$

$$= 5932\ \Omega \approx 5.9k\Omega$$

Output Resistance, $R_o = r_e + \frac{R_S}{(\beta+1)}$

$$R_{o_5} = r_{e_5} + \frac{R_{o_4}}{(\beta+1)}$$

$$= 25 + \frac{646.11}{(160+1)}$$

$$= 29.01\Omega$$

Here, $\frac{R_S}{(\beta+1)}$ is in the region of a few ohms only, and r_e is also very small, so the total output resistance is very low.

Calculations with the given value

Voltage Gain, $A_v = \frac{V_o}{V_S} = \frac{V_o}{V_b} \cdot \frac{V_b}{V_S}$

Here,

$V_b = i_e (r_e + R_L)$

$V_o = i_o R_L = i_e R_L$

$\frac{V_o}{V_b} = \frac{i_e R_L}{i_e (r_e + R_L)} = \frac{R_L}{r_e + R_L}$

$\frac{V_b}{V_s} = \frac{R_i}{R_i + R_S}$ [Using Voltage Division Rule]

$$\therefore A_{vi} = \frac{V_o}{V_b} \cdot \frac{V_b}{V_S} = \frac{R_L}{r_e + R_L} \cdot \frac{R_i}{R_i + R_S}$$

$$= \frac{R_L}{r_{e_5} + R_L} \cdot \frac{R_{i_5}}{R_{i_5} + R_{o_4}}$$

$$= \frac{12}{25 + 12} \cdot \frac{5.9k}{5.9k + 646.11}$$

$$= 0.324 \cdot 0.9 = 0.29$$

The DC biasing Circuit for the output stage will be the same as before (input Stage), and it is shown in the input stage.

4. Verification of the Designed Circuit:

Verification of the overall Gain,

Entire Voltage Gain, $A_v = \frac{V_o}{V_S} = \frac{V_o}{V_{b_5}} \cdot \frac{V_{b_5}}{V_{b_4}} \cdot \frac{V_{b_4}}{V_{b_3}} \cdot \frac{V_{b_3}}{V_{b_2}} \cdot \frac{V_{b_2}}{V_{b_1}} \cdot \frac{V_{b_1}}{V_s}$

$\frac{V_o}{V_{b_5}} = \frac{R_L}{r_{e_5} + R_L}$ $= \frac{12}{25+ 12} = 0.324$
$\frac{V_{b_5}}{V_{b_4}} = \frac{R_{i_5}}{r_{e_5} + R_{i_5}}$ $= \frac{5932}{25 + 5932}$ $= 0.99$
$\frac{V_{b_4}}{V_{b_3}} = - g_{m_1}(r_{o_3} \parallel R_{i_3})$ This stage is the CE stage. Here, I_c=0.20m g_m= 0.008 $r_{o_3} = 500k$ So, $\frac{V_{b_3}}{V_{b_2}} = - g_{m_2}(r_{o_2} \parallel R_{i_2})$ $= -0.008\ R_{i_3}$ $(R_{i_3} >> r_{o_3})$ $= -0.008\ 4k$ $= - 32$
$\frac{V_{b_3}}{V_{b_2}} = - g_{m_2}(r_{o_2} \parallel R_{i_2})$ This stage is the CE stage. Here, I_c=0.20m g_m= 0.008

$$r_{o_3} = 500k$$

So,

$$\frac{V_{b_3}}{V_{b_2}} = -g_{m_2}(r_{o_2} \parallel R_{i_2})$$

$$= -0.008\, R_{i_3} \quad (R_{i_3} >> r_{o_3})$$

$$= -0.008\, R_{i_3} \quad (R_{i_3} >> r_{o_3})$$

$$= -0.008\, 4k$$

$$= -32$$

$$\frac{V_{b_2}}{V_{b_1}} = \frac{r_{\pi_2}}{r_{e_1} + r_{\pi_2}}$$

$$= \frac{4000}{25 + 4000}$$

$$= 0.99$$

$$\frac{V_{b_1}}{V_s} = \frac{R_i}{R_i + R_S}$$

$$= \frac{648k}{648k + 10k}$$

$$= 0.98$$

Verification of DC Biasing Circuits,

Input Stage:

We know that for amplification, the Base to Emitter terminal has to be forward-biased and the Collector to Base terminal has to be reverse-biased. For the input stage, common collector amplifiers.

$$V_B = \frac{R_2}{R_1 + R_2} \times V_{CC}$$

$$= \frac{131}{109 + 131} \times 15$$

$$= 8.2V$$

Again,

$V_E = V_B - V_{BE}$
$= 8.2 - 0.7$
$= 7.5V$

$I_E = \frac{V_E}{R_E}$

$= \frac{7.5}{7.5}$

$= 1mA$

$I_C = \alpha I_E$
$= 0.99 \times 1$
$= 0.99$
$\approx 1mA$

Here, the collector terminal is directly connected to the V_{CC}. So, $V_C = 15V$

So, $V_C > V_B$ $[V_C=15V; V_B=8.2V]$
$\therefore V_{CB}$ is reverse-biased.
Also, $V_B < V_E$ $[V_E=7.5V; V_B=8.2V]$

$\therefore V_{BE}$ is Forward-biased.

Moreover,
We know, $V_C > v_{omax} + V_B$

v_{omax} = 1.1V from the previous calculations. This is the voltage of the AC output.

$\therefore v_{omax} + V_B = 1.1 + 8.2 = 9.3V$ which is less than 15V. So, even with the maximum AC output voltage, the CB terminal will be reverse-biased.

Simulation Results:

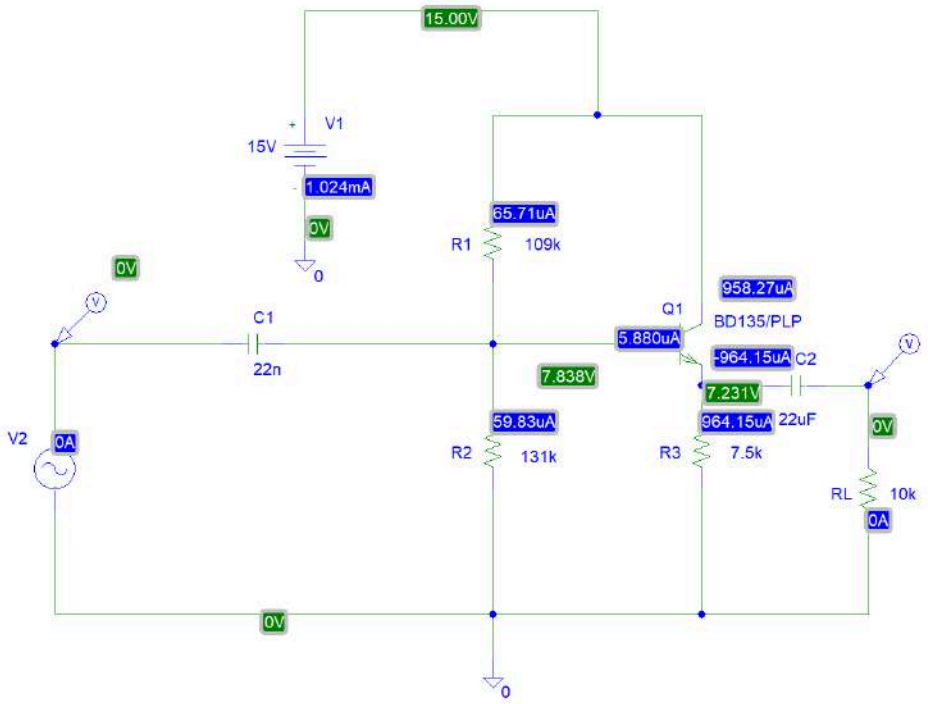


Figure: DC Biasing Currents for Input Stage

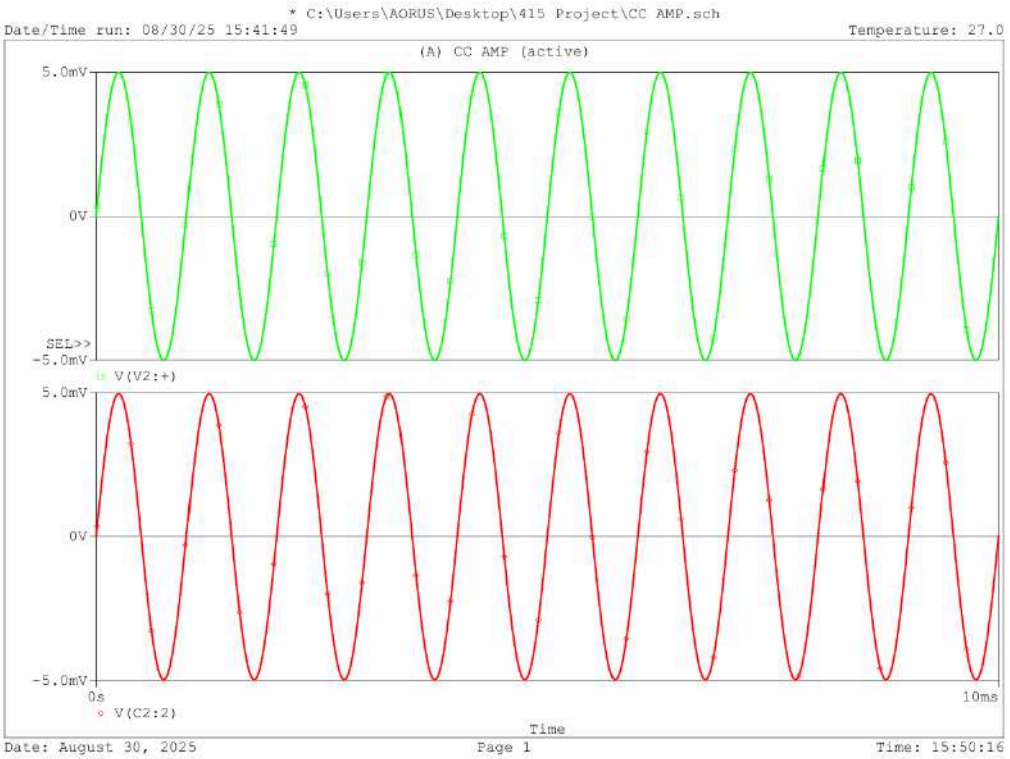


Figure: Input and Output Waveforms of CC amplifier.

Gain stage

$V_B = \frac{R_2}{R_1 + R_2} \times V_{CC}$

$= \frac{592k}{608k+592k} \times 15$

$= 7.4V$

Again,

$V_E = V_B - V_{BE}$

$= 7.4 - 0.7$

$= 6.7\ V$

$I_E = \frac{V_E}{R_E}$

$= \frac{6.7}{33.5}$

$= 0.2mA$

$I_C = \alpha I_E$

$= 0.993 \cdot 0.2$

$= 0.1986mA$

$V_C = V_{CC} - I_C R_C$

$= 15 - 0.19m \cdot 4k$

$= 14.24$

So, $V_C > V_B$ $[V_C=14.24V; V_B=7.4V]$

∴ V_{CB} is reverse-biased.

Also, $V_B < V_E$ $[V_E=6.7V; V_B=7.4V]$

∴ V_{EB} is Forward-biased.

Moreover,

We know, $V_C > v_{omax} + V_B$ and $I_C R_C > v_{omax}$

v_{omax} = 1.1V from the previous calculations. This is the voltage of the AC output.

∴ $v_{omax} + V_B = 1.1 + 7.4 = 8.5V$ which is less than 15V. So, even with the maximum AC output voltage, the CB terminal will be reverse-biased. Additionally, $I_C R_C = 0.19m \cdot 4k = 0.76V$, which is greater than 1.1V. So, in both cases, the CB terminal remains reverse-biased.

Simulation Results:

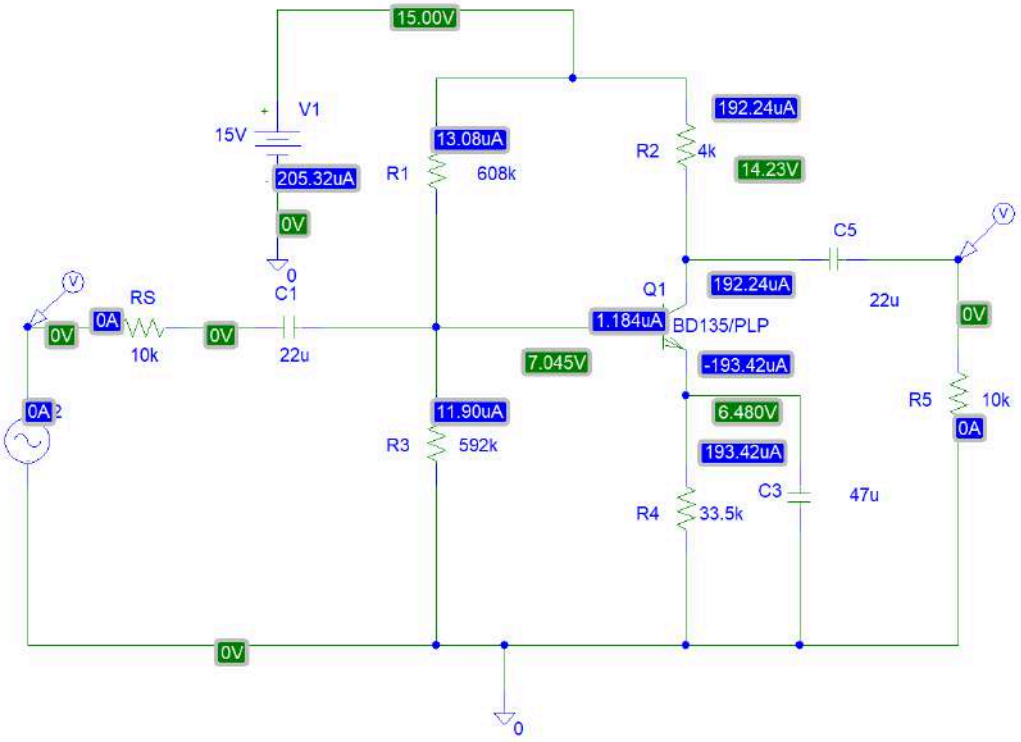


Figure: DC Biasing Currents for Gain Stage

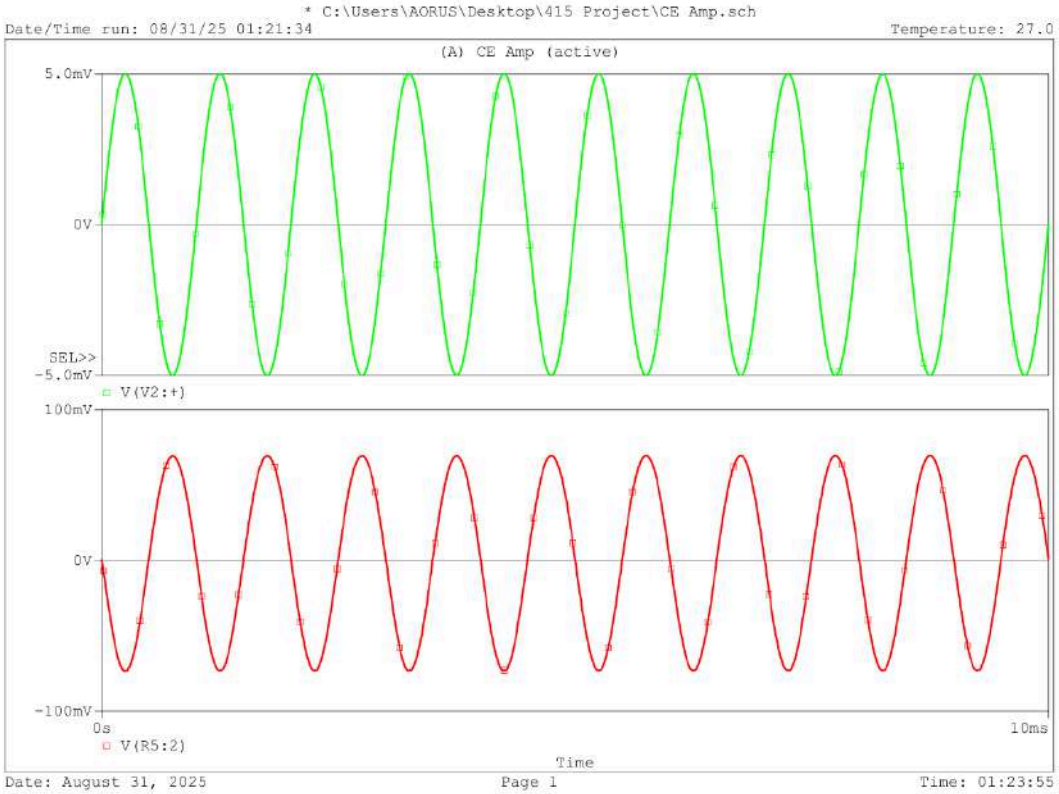


Figure: Input and Output Waveforms of the CE amplifier.

Output stage:

We know that for amplification, the Base to Emitter terminal has to be forward-biased and the Collector to Base terminal has to be reverse-biased. For the input stage, common collector amplifiers.

$$V_B = \frac{R_2}{R_1 + R_2} \times V_{CC}$$

$$= \frac{131}{109 + 131} \times 15$$

$$= 8.2V$$

Again,

$$V_E = V_B - V_{BE}$$
$$= 8.2 - 0.7$$
$$= 7.5V$$
$$I_E = \frac{V_E}{R_E}$$
$$= \frac{7.5}{7.5}$$
$$= 1mA$$
$$I_C = \alpha I_E$$
$$= 0.99 \times 1$$
$$= 0.99$$
$$\approx 1mA$$

Here, the collector terminal is directly connected to the V_{CC}. So, $V_C = 15V$

So, $V_C > V_B$ $[V_C=15V; V_B=8.2V]$
$\therefore V_{CB}$ is reverse-biased.
Also, $V_B < V_E$ $[V_E=7.5V; V_B=8.2V]$

$\therefore V_{BE}$ is Forward-biased.

Moreover,
We know, $V_C > v_{omax} + V_B$

v_{omax} = 1.1V from the previous calculations. This is the voltage of the AC output.

$\therefore v_{omax} + V_B = 1.1 + 8.2 = 9.3V$ which is less than 15V. So, even with the maximum AC output voltage, the CB terminal will be reverse-biased.

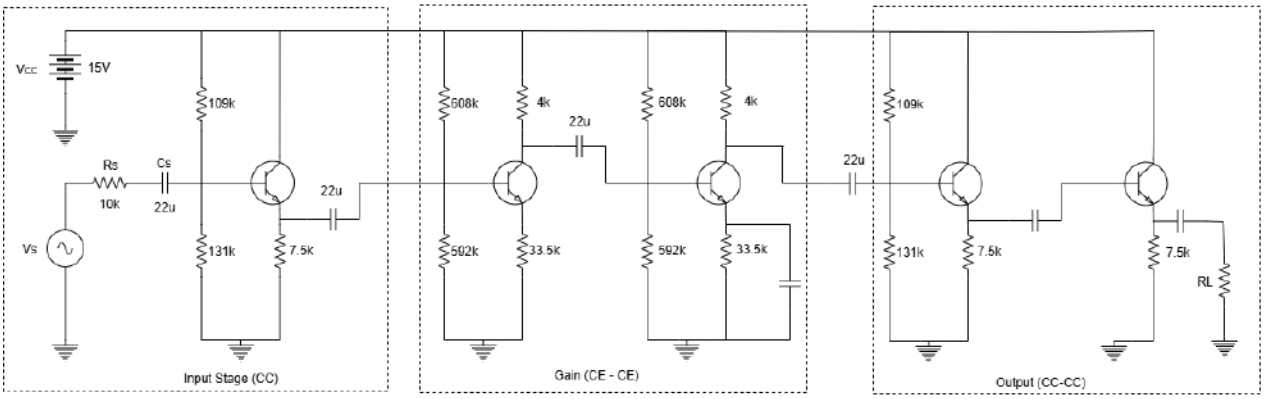
It will be the same for both CE.

5. Corrections and Modifications

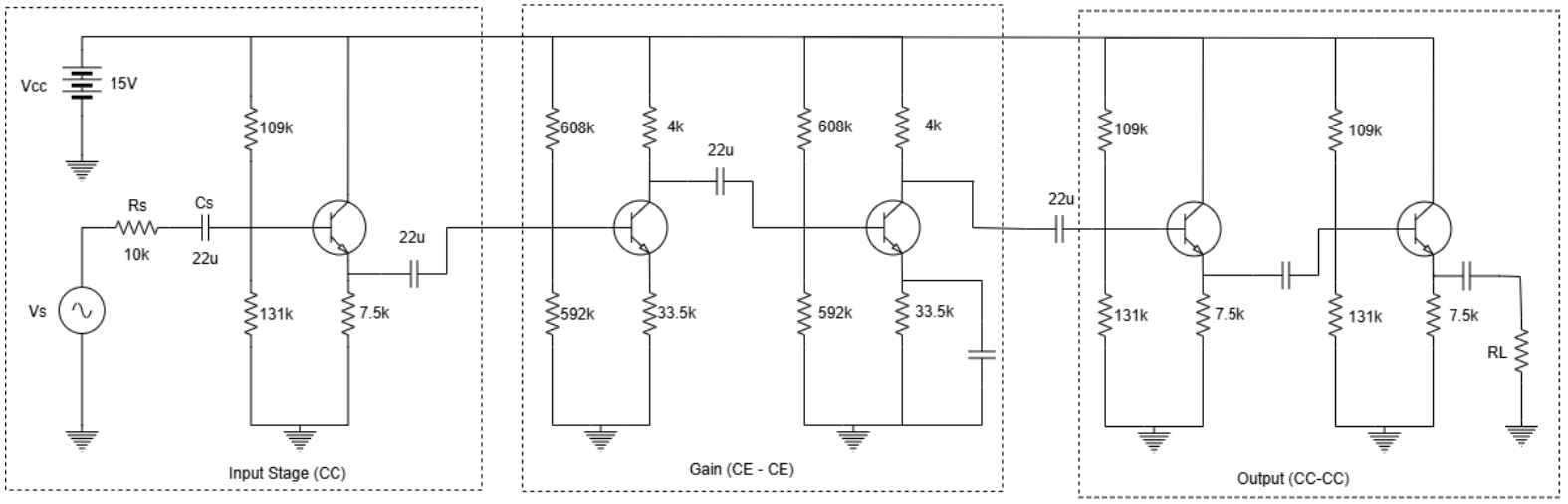
Target A_v = 311 V/V, calculated ≈ 318 V/V, error ≈ 2.2% (<5%).

So, we do not need any modifications.

But we can attach the Darlington pair at the end. As we know, the Darlington pair is a super follower. So there won't be any loss of gain in the output stage.



6. The Complete Circuit Diagram



All resistors' values:

Input stage	Gain Stage		Output Stage	
CC	CE	CE	CC	CC
R_1=109kΩ	R_1=608kΩ	R_1=608kΩ	R_1=109kΩ	R_1=109kΩ
R_2=131kΩ	R_2=592kΩ	R_2=592kΩ	R_2=131kΩ	R_2=131kΩ
R_E=7.5kΩ	R_E=33.5kΩ	R_E=33.5kΩ	R_E=7.5kΩ	R_E=7.5kΩ
R_C = -	R_C = 4kΩ	R_C = 4kΩ	R_C = -	R_C = -

7. Comments:

The main points of the amplifier design are its multistage topology and the successful meeting of performance targets. The design uses a Common-Collector (CC), Common-Emitter (CE), and two cascaded CC stages to achieve the required high input impedance, voltage gain, and low output resistance. The CE stage provides the primary amplification, while the output CC stages efficiently drive the 12 Ω speaker. The final design achieved an overall voltage gain of approximately 318 V/V, which is very close to the target of 311.615 V/V, resulting in a low error of about 2.2%. The project demonstrated a solid understanding of analog circuit design principles and successfully met its objectives.

Conclusion:

The multistage amplifier design detailed in this project is robust and effective. The combination of CC and CE stages provides a well-balanced solution for the project's objective of amplifying a low-level signal to drive a loudspeaker. The detailed calculations and verification steps demonstrate a thorough understanding of analog circuit design principles, including biasing, impedance matching, and gain-stage optimization. The design's performance, as verified by the analysis, shows a minimal error from the target specifications, highlighting the success of the chosen methodology.