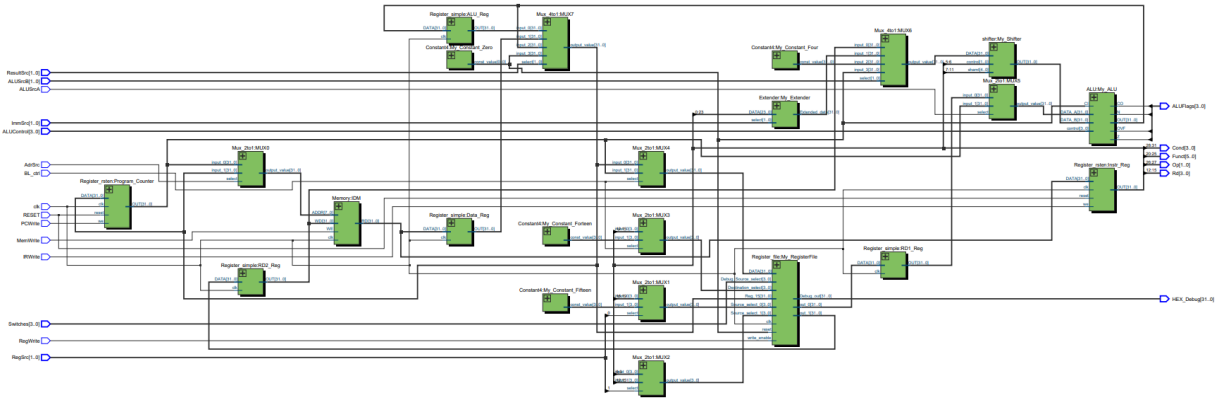
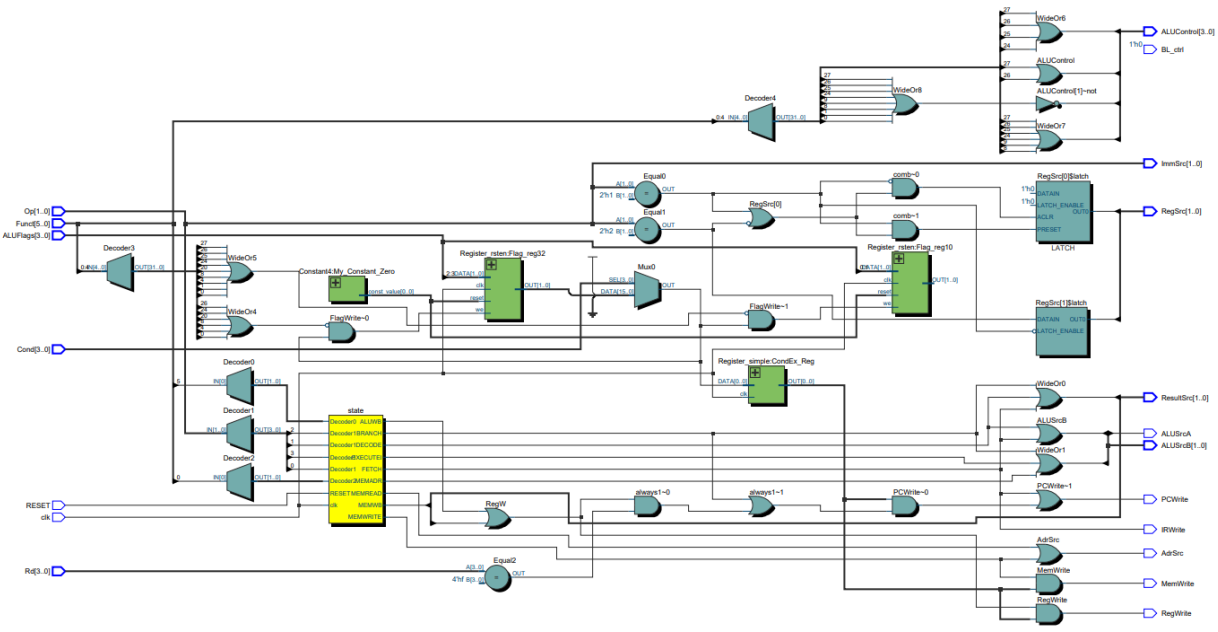
The following figure outline the RTL view of the system:



Part b) The addition of the MOV instruction was straightforward because we can augment the ALU control to incorporate the ALU's inherent move functionality, which adheres to the same execution cycle as other arithmetic operations. By adjusting the shift control and specifying the amount via the controller based on the move type, we can shift input B as required. For the BX part, the RA2 multiplexer can be utilized to forward RM, and then the ALU can process it to transfer it to the Program Counter (PC).

Question 2) Controller Design RTL View



Explanation:

For the MOV section, I modified the ALU code transmitted through the ALU decoder module and configured both the shift amount and type within the finite state machine. Regarding the BX portion, I simply adjusted the appropriate ALU and multiplexer signals, employing funct[0] to differentiate it from B and established a distinct state for this operation.

Top Level for Tests:

```
module Multi_Cycle_Computer(
   input clk,
   input reset,
   output [31:0] PC
);

wire PCWrite_wire;
wire ADRSrc_to_Mux;
wire MemWrite_wire;
wire IRWrite_wire;
wire [1:0] ResultSrc_wire;
wire [3:0] ALUControl_wire;
wire ALUSrcA_wire;
wire [1:0] ALUSrcB_wire;
wire [1:0] ImmSrc_wire;
wire RegWrite_wire;
wire [1:0] RegSrc_wire;
wire [3:0] ALUFlags_wire;
wire [3:0] Cond_wire;
wire [1:0] Op_wire;
wire [5:0] Funct_wire;
wire [3:0] Rd_wire;
wire BL_ctrl_wire;


 Controller My_Controller(
                        .PCWrite(PCWrite_wire),
                .AdrSrc(ADRSrc_to_Mux),
```

```
        .MemWrite(MemWrite_wire),
        .IRWrite(IRWrite_wire),
        .ResultSrc(ResultSrc_wire),
        .ALUControl(ALUControl_wire),
        .ALUSrcB(ALUSrcB_wire),
        .ALUSrcA(ALUSrcA_wire),
        .ImmSrc(ImmSrc_wire),
        .RegWrite(RegWrite_wire),
        .RegSrc(RegSrc_wire),
        .BL_ctrl(BL_ctrl_wire),
                .ALUFlags(ALUFlags_wire),
                .Cond(Cond_wire),
                .Op(Op_wire),
                .Funct(Funct_wire),
                .Rd(Rd_wire),
                .clk(clk),
                .RESET(reset)
  );

DataPath My_DataPath (
    .clk(clk),
                .reset(reset),
                .PCWrite(PCWrite_wire),
                .AdrSrc(ADRSrc_to_Mux),
                .MemWrite(MemWrite_wire),
                .IRWrite(IRWrite_wire),
                .ResultSrc(ResultSrc_wire),
                .ALUControl(ALUControl_wire),
                .ALUSrcB(ALUSrcB_wire),
```

```
                .ALUSrcA(ALUSrcA_wire),
                .ImmSrc(ImmSrc_wire),
                .RegWrite(RegWrite_wire),
                .RegSrc(RegSrc_wire),
                .BL_ctrl(BL_ctrl_wire),

                .ALUFlags(ALUFlags_wire),
                .Cond(Cond_wire),
                .Op(Op_wire),
                .Funct(Funct_wire),
                .Rd(Rd_wire),

                //for debugging
                .Switches(),
                .HEX_Debug(),
                .PC_Out(PC)
);
Endmodule
```

Part 4) The test bench results were not as expected as I cannot figure out why the PC is not updating if I can only check that I'm sure the entire code will work properly

EE446 Preliminary Report # 2

```
bash: C:Usersfarruminiconda3python.exe: command not found
rm -f results.xml
/usr/bin/make -f Makefile results.xml
make[1]: Entering directory '/c/Users/farru/OneDrive/Desktop/Multi_Cycle_test/Test'
bash: C:Usersfarruminiconda3python.exe: command not found
bash: C:Usersfarruminiconda3python.exe: command not found
rm -f results.xml
MODULE=Multi_Cycle_Test TESTCASE= TOPLEVEL=Multi_Cycle_Computer TOPLEVEL_LANG=verilog \
         /c/iverilog/bin/vvp -M C:/Users/farru/miniconda3/Lib/site-packages/cocotb/libs -m cocotbvpi_icarus   sim_build/sim.vvp
     -.--ns INFO     gpi                                ..mbed\gpi_embed.cpp:78   in set_program_name_in_venv        Did not detect Python virtual environment. Using system-wide Python int
erpreter
     -.--ns INFO     gpi                                ..\gpi\GpiCommon.cpp:101  in gpi_print_registered_impl       VPI registered
     0.00ns INFO     cocotb                             Running on Icarus Verilog version 12.0 (devel)
     0.00ns INFO     cocotb                             Running tests with cocotb v1.8.1 from C:\Users\farru\miniconda3\Lib\site-packages\cocotb
     0.00ns INFO     cocotb                             Seeding Python random module with 1711950473
     0.00ns INFO     cocotb.regression                  Found test Multi_Cycle_Test.Multi_cycle_test
     0.00ns INFO     cocotb.regression                  +[34mrunning+[49m+[39m Multi_cycle_test (1/1)
WARNING: C:/Users/farru/OneDrive/Desktop/Multi_Cycle_test/Test/../HDL/ID_memory.v:11: $readmemh: The behaviour for reg[...] mem[N:0]; $readmemh("...", mem); changed in the 1364-2005 standa
rd. To avoid ambiguity, use mem[0:N] or explicit range parameters $readmemh("...", mem, start, stop);. Defaulting to 1364-2005 behavior.
WARNING: C:/Users/farru/OneDrive/Desktop/Multi_Cycle_test/Test/../HDL/ID_memory.v:11: $readmemh(instructions.hex): Not enough words in the file for the requested range [0:255].
  5000.00ns DEBUG    Performance Model                  *************** Instruction No: 0 **********************
  5000.00ns DEBUG    Performance Model                  ****** Current Instruction *********
  5000.00ns DEBUG    Performance Model                  Binary string:11100011101000000010000000010011
  5000.00ns DEBUG    Performance Model                  Operation type Data Processing
  5000.00ns DEBUG    Performance Model                  cond:E
  5000.00ns DEBUG    Performance Model                  Immediate bit:1
  5000.00ns DEBUG    Performance Model                  cmd:D
  5000.00ns DEBUG    Performance Model                  Set bit:0
  5000.00ns DEBUG    Performance Model                  Rn:0     Rd:1
  5000.00ns DEBUG    Performance Model                  rot:0    imm8:19
 15000.00ns DEBUG    Performance Model                  ***************** Positive Clock Edge: 0 **********************
 25000.00ns DEBUG    Performance Model                  ***************** Positive Clock Edge: 1 **********************
 35000.00ns DEBUG    Performance Model                  ***************** Positive Clock Edge: 2 **********************
 40000.00ns DEBUG    Performance Model                  ************ DUT DATAPATH Signals ***************
 40000.00ns INFO     cocotb.Multi_Cycle_Computer        reset:0x0
 40000.00ns INFO     cocotb.Multi_Cycle_Computer        ALUSrcA:0b0
 40000.00ns INFO     cocotb.Multi_Cycle_Computer        ALUSrcB:0b0
 40000.00ns INFO     cocotb.Multi_Cycle_Computer        MemWrite:0x0
 40000.00ns INFO     cocotb.Multi_Cycle_Computer        ResultSrc:0x13
 40000.00ns DEBUG    Performance Model                  ************ DUT Controller Signals ***************
 40000.00ns INFO     cocotb.Multi_Cycle_Computer        ALUControl:0xd
 45000.00ns DEBUG    Performance Model                  ***************** Positive Clock Edge: 3 **********************
 50000.00ns DEBUG    Performance Model                  ************* Performance Model / DUT Data  **************
 50000.00ns DEBUG    Performance Model                  PC:0x4   PC:0x4
 50000.00ns DEBUG    Performance Model                  Register0: 0x0          0x0
 50000.00ns DEBUG    Performance Model                  Register1: 0x13         0x13
 50000.00ns DEBUG    Performance Model                  Register2: 0x0          0x0
 50000.00ns DEBUG    Performance Model                  Register3: 0x0          0x0
 50000.00ns DEBUG    Performance Model                  Register4: 0x0          0x0
 50000.00ns DEBUG    Performance Model                  Register5: 0x0          0x0
```

```
40000.00ns INFO     cocotb.Multi_Cycle_Computer        ALUSrcB:0b0
40000.00ns INFO     cocotb.Multi_Cycle_Computer        MemWrite:0x0
40000.00ns INFO     cocotb.Multi_Cycle_Computer        ResultSrc:0x13
40000.00ns DEBUG    Performance Model                  ************ DUT Controller Signals ***************
40000.00ns INFO     cocotb.Multi_Cycle_Computer        ALUControl:0xd
45000.00ns DEBUG    Performance Model                  ***************** Positive Clock Edge: 3 **********************
50000.00ns DEBUG    Performance Model                  ************* Performance Model / DUT Data  **************
50000.00ns DEBUG    Performance Model                  PC:0x4   PC:0x4
50000.00ns DEBUG    Performance Model                  Register0: 0x0          0x0
50000.00ns DEBUG    Performance Model                  Register1: 0x13         0x13
50000.00ns DEBUG    Performance Model                  Register2: 0x0          0x0
50000.00ns DEBUG    Performance Model                  Register3: 0x0          0x0
50000.00ns DEBUG    Performance Model                  Register4: 0x0          0x0
50000.00ns DEBUG    Performance Model                  Register5: 0x0          0x0
50000.00ns DEBUG    Performance Model                  Register6: 0x0          0x0
50000.00ns DEBUG    Performance Model                  Register7: 0x0          0x0
50000.00ns DEBUG    Performance Model                  Register8: 0x0          0x0
50000.00ns DEBUG    Performance Model                  Register9: 0x0          0x0
50000.00ns DEBUG    Performance Model                  Register10: 0x0         0x0
50000.00ns DEBUG    Performance Model                  Register11: 0x0         0x0
50000.00ns DEBUG    Performance Model                  Register12: 0x0         0x0
50000.00ns DEBUG    Performance Model                  Register13: 0x0         0x0
50000.00ns DEBUG    Performance Model                  Register14: 0x0         0x0
50000.00ns DEBUG    Performance Model                  Register15: 0x8         0x8
50000.00ns DEBUG    Performance Model                  *************** Instruction No: 1 **********************
50000.00ns DEBUG    Performance Model                  ****** Current Instruction *********
50000.00ns DEBUG    Performance Model                  Binary string:11100000100000010010000000000001
50000.00ns DEBUG    Performance Model                  Operation type Data Processing
50000.00ns DEBUG    Performance Model                  cond:E
50000.00ns DEBUG    Performance Model                  Immediate bit:0
50000.00ns DEBUG    Performance Model                  cmd:4
50000.00ns DEBUG    Performance Model                  Set bit:0
50000.00ns DEBUG    Performance Model                  Rn:1     Rd:2
50000.00ns DEBUG    Performance Model                  shamt5:0         sh:0    Rm:1
55000.00ns DEBUG    Performance Model                  ***************** Positive Clock Edge: 4 **********************
65000.00ns DEBUG    Performance Model                  ***************** Positive Clock Edge: 5 **********************
75000.00ns DEBUG    Performance Model                  ***************** Positive Clock Edge: 6 **********************
80000.00ns DEBUG    Performance Model                  ************ DUT DATAPATH Signals ***************
80000.00ns INFO     cocotb.Multi_Cycle_Computer        reset:0x0
80000.00ns INFO     cocotb.Multi_Cycle_Computer        ALUSrcA:0b0
80000.00ns INFO     cocotb.Multi_Cycle_Computer        ALUSrcB:0b0
80000.00ns INFO     cocotb.Multi_Cycle_Computer        MemWrite:0x0
80000.00ns INFO     cocotb.Multi_Cycle_Computer        ResultSrc:0x26
80000.00ns DEBUG    Performance Model                  ************ DUT Controller Signals ***************
80000.00ns INFO     cocotb.Multi_Cycle_Computer        ALUControl:0x4
85000.00ns DEBUG    Performance Model                  ***************** Positive Clock Edge: 7 **********************
90000.00ns DEBUG    Performance Model                  ************* Performance Model / DUT Data  **************
```

```
75000.00ns DEBUG    Performance Model                ********** Positive Clock Edge: 6 **********
80000.00ns DEBUG    Performance Model                *********** DUT DATAPATH Signals **************
80000.00ns INFO     cocotb.Multi_Cycle_Computer      reset:0x0
80000.00ns INFO     cocotb.Multi_Cycle_Computer      ALUSrcA:0b0
80000.00ns INFO     cocotb.Multi_Cycle_Computer      ALUSrcB:0b0
80000.00ns INFO     cocotb.Multi_Cycle_Computer      MemWrite:0x0
80000.00ns INFO     cocotb.Multi_Cycle_Computer      ResultSrc:0x26
80000.00ns DEBUG    Performance Model                ************ DUT Controller Signals ***************
80000.00ns INFO     cocotb.Multi_Cycle_Computer      ALUControl:0x4
85000.00ns DEBUG    Performance Model                ********** Positive Clock Edge: 7 **********
90000.00ns DEBUG    Performance Model                ************* Performance Model / DUT Data  **************
90000.00ns DEBUG    Performance Model                PC:0x8   PC:0x4
90000.00ns DEBUG    Performance Model                Register0: 0x0          0x0
90000.00ns DEBUG    Performance Model                Register1: 0x13         0x13
90000.00ns DEBUG    Performance Model                Register2: 0x26         0x26
90000.00ns DEBUG    Performance Model                Register3: 0x0          0x0
90000.00ns DEBUG    Performance Model                Register4: 0x0          0x0
90000.00ns DEBUG    Performance Model                Register5: 0x0          0x0
90000.00ns DEBUG    Performance Model                Register6: 0x0          0x0
90000.00ns DEBUG    Performance Model                Register7: 0x0          0x0
90000.00ns DEBUG    Performance Model                Register8: 0x0          0x0
90000.00ns DEBUG    Performance Model                Register9: 0x0          0x0
90000.00ns DEBUG    Performance Model                Register10: 0x0         0x0
90000.00ns DEBUG    Performance Model                Register11: 0x0         0x0
90000.00ns DEBUG    Performance Model                Register12: 0x0         0x0
90000.00ns DEBUG    Performance Model                Register13: 0x0         0x0
90000.00ns DEBUG    Performance Model                Register14: 0x0         0x0
90000.00ns DEBUG    Performance Model                Register15: 0xc         0xc
91000.00ns INFO     cocotb.regression                Multi_cycle_test +[31mfailed+[49m+[39m
                                                     Traceback (most recent call last):
                                                       File "C:\Users\farru\OneDrive\Desktop\Multi_Cycle_test\Test\Multi_Cycle_Test.py", line 210, in Multi_cycle_test
                                                         await tb.run_test()
                                                       File "C:\Users\farru\OneDrive\Desktop\Multi_Cycle_test\Test\Multi_Cycle_Test.py", line 196, in run_test
                                                         self.compare_result()
                                                       File "C:\Users\farru\OneDrive\Desktop\Multi_Cycle_test\Test\Multi_Cycle_Test.py", line 73, in compare_result
                                                         assert self.PC == self.dut_PC.value
                                                     AssertionError: assert 8 == 00000000000000000000000000000100
                                                      +  where 8 = <Multi_Cycle_Test.TB object at 0x000001643303D3D0>.PC
                                                      +  and   00000000000000000000000000000100 = ModifiableObject(Multi_Cycle_Computer.PC).value
                                                      +    where ModifiableObject(Multi_Cycle_Computer.PC) = <Multi_Cycle_Test.TB object at 0x000001643303D3D0>.dut_PC
91000.00ns INFO     cocotb.regression                ****************************************************************************************
                                                     ** TEST                                  STATUS  SIM TIME (ns)  REAL TIME (s)  RATIO (ns/s) **
                                                     ****************************************************************************************
                                                     ** Multi_Cycle_Test.Multi_cycle_test  +[31m FAIL +[49m+[39m      91000.00           0.02     4786877.33  **
                                                     ****************************************************************************************
                                                     ** TESTS=1 PASS=0 FAIL=1 SKIP=0                91000.00           0.08     1131753.68  **
                                                     ****************************************************************************************

make[1]: Leaving directory '/c/Users/farru/OneDrive/Desktop/Multi_Cycle_test/Test'
(base) PS C:\Users\farru\OneDrive\Desktop\Multi_Cycle_test\Test>
```