EE446 Computer Architecture II
Preliminary Report

Datapath Design

1) The code is given in the Verilog files uploaded and the RTL view is also in the given files as well as shown in the diagram below.

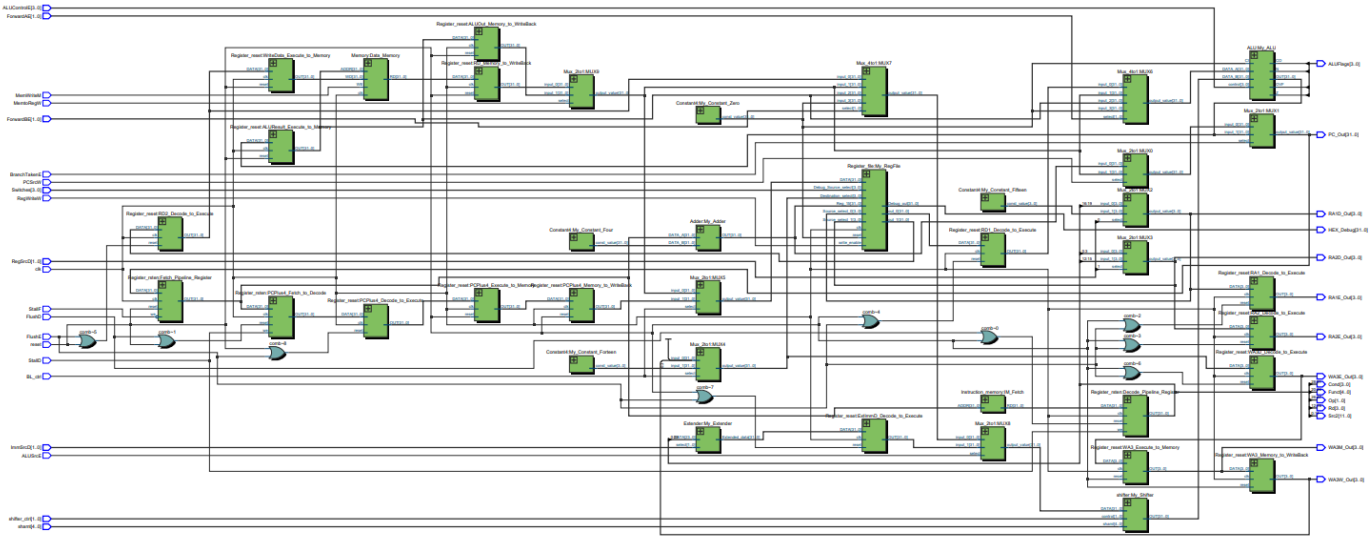

Fig 1 Datapath RTL view

2) The following picture shows the modified data path view for the additional instructions:

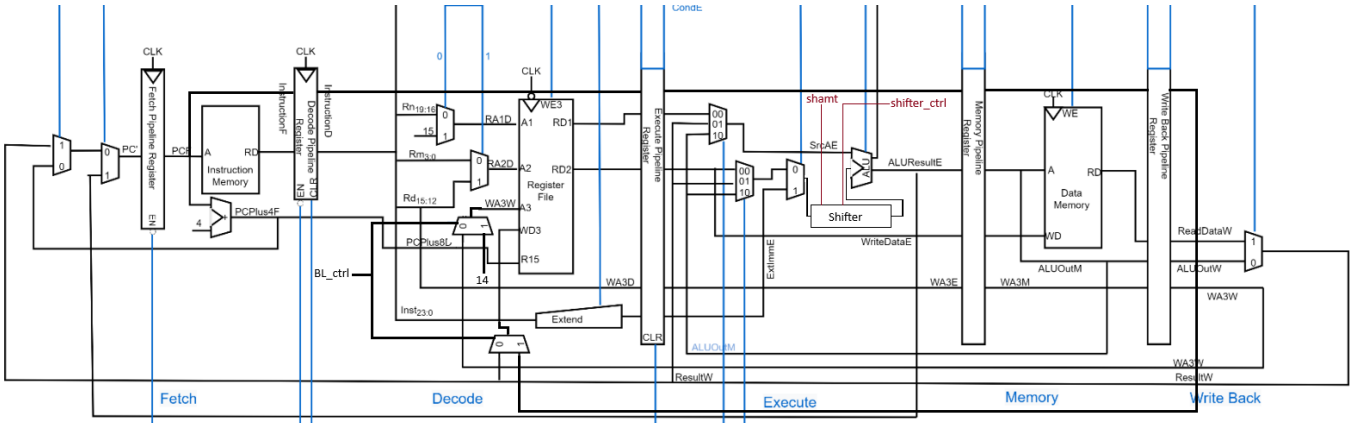

Fig 1 Modified Data Path

Register shifted immediate operations are managed by a shifter positioned just before the ALU. The controller determines the control signals for the shifter, instructing it to either shift by 5, rotate by 1, or leave the data unchanged, depending on the instruction. For both MOV operations, the ALU's mov functionality is utilized. Distinguishing between the two mov instructions involves adjusting the control signals for the shifter and the multiplexer, allowing selection from either the extension or the register operand. As for the BX instruction, the ALU's mov functionality is employed to directly transfer the contents of Rm to the write-back stage. From there, it proceeds to the program counter without the need for any hardware modifications. For the BL instruction, the pipeline registers convey pc+4 to the write-back stage. If the instruction requires branching, two new multiplexers positioned in the decode stage enable the writing of pc+4 to Rm.

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Controller Design

1) The following diagram shows the Controller synthesized RTL view.

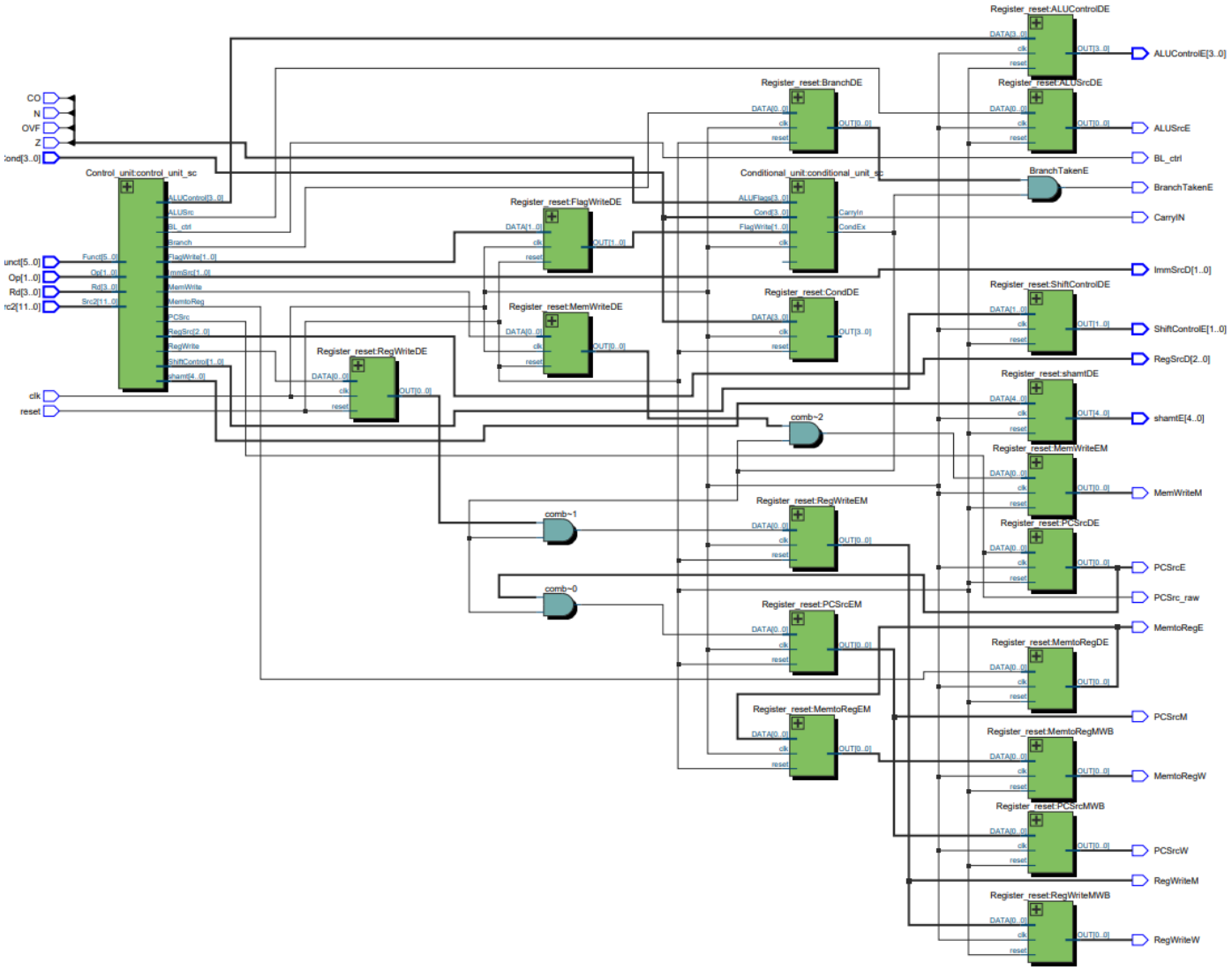

Fig 3 Controller Synthesized RTL view

2) Code Explanation for Additional Branching and Move operations:

- Register Shifted Immediate Operations: It's not explicitly shown how immediate values are handled in the control unit as the provided module focuses on signal generation for pipeline stages. However, if shifted immediate operations require a specific control signal, it might involve extending the Control_unit to generate the appropriate signals for these operations.
- MOV Operations: Similar to the immediate operations, specific control logic would be required for MOV operations to ensure that the move instruction does not conflict with data that is yet to be written back. It may involve creating new control signals that can distinguish MOV operations and apply the necessary controls in the pipeline stages.
- BL and BX Instructions: For these branch instructions, the control logic should ensure that the PC is correctly updated. This might involve new control signals (like BL_ctrl seen in the controller code) that handle the updating of the link register and the PC. The BranchTakenE signal is part of the logic that ensures the PC is set correctly after a conditional branch instruction is resolved.

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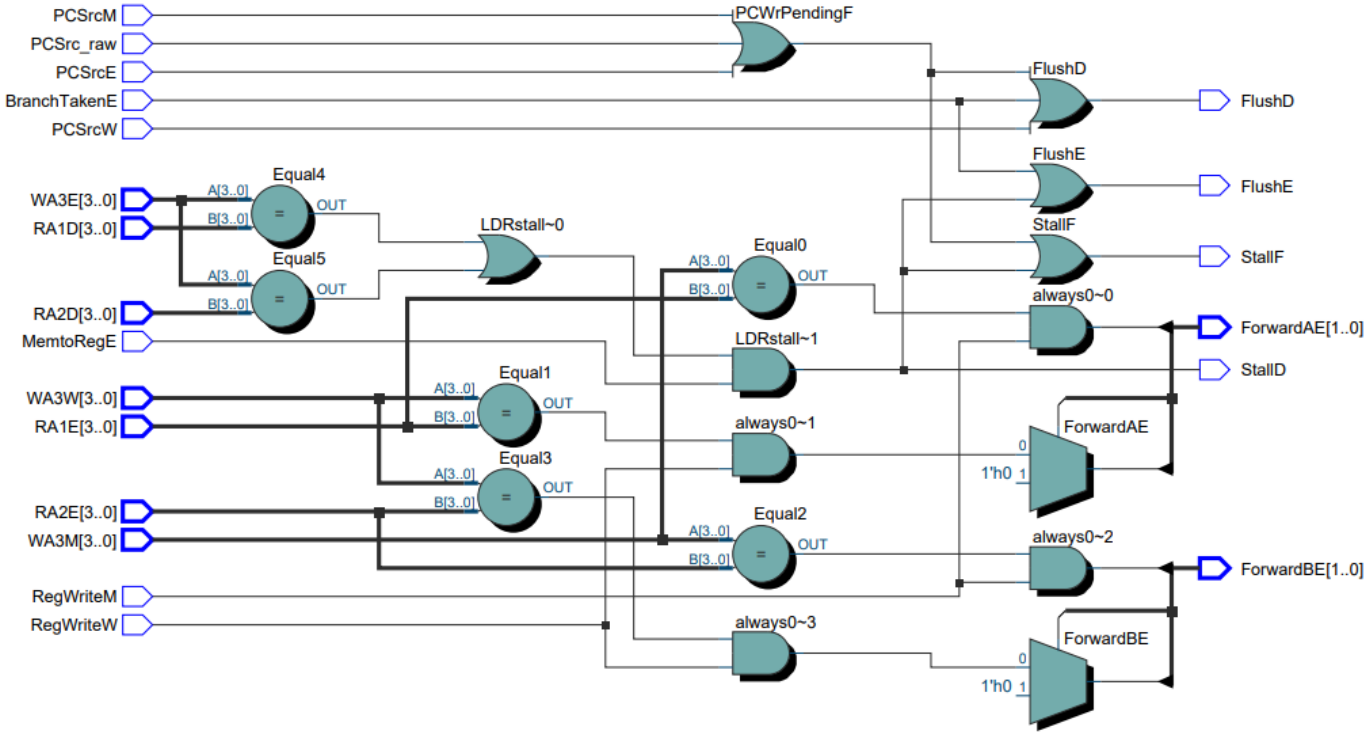
Hazard Control

1) The following diagram shows the Hazard Control RTL view.



Code Explanation for Additional Operations:

- Register Shifted Immediate Operations: These operations involve using a register value that might not be written back yet due to pipeline stages. In the provided Hazard unit, this is handled by checking for data dependencies between executing and memory/writing stages (with ForwardAE and ForwardBE signals). If a register that is needed in the execute stage (RA1E or RA2E) is about to be written in the memory (WA3M) or write-back stage (WA3W), the forwarding logic ensures that the most recent value is used, thereby avoiding stalls.
- MOV Operations: There are two types of MOV operations – one that moves a register value to another and one that moves an immediate value to a register. The hazard would occur if the source register is involved in an operation in the memory or write-back stage. The provided logic ensures that if the source register is the same as WA3M or WA3W, and a write-back is pending (RegWriteM or RegWriteW is high), the data is forwarded appropriately to prevent a hazard.
- BL (Branch with Link) and BX (Branch and Exchange): These instructions affect the program counter (PC) and possibly the link register. The Hazard unit needs to consider that BL and BX could be affected by previous instructions that haven't completed. The PCSrc_raw, PCSrcE, PCSrcM, and BranchTakenE signals seem to indicate the detection of branch instructions. A stall (StallF or StallD) is initiated if a branch is detected, allowing time for the PC to be correctly set before fetching and decoding new instructions. Additionally, FlushD and FlushE are set high to clear out any instructions that were fetched or decoded but should not be executed due to the branch.

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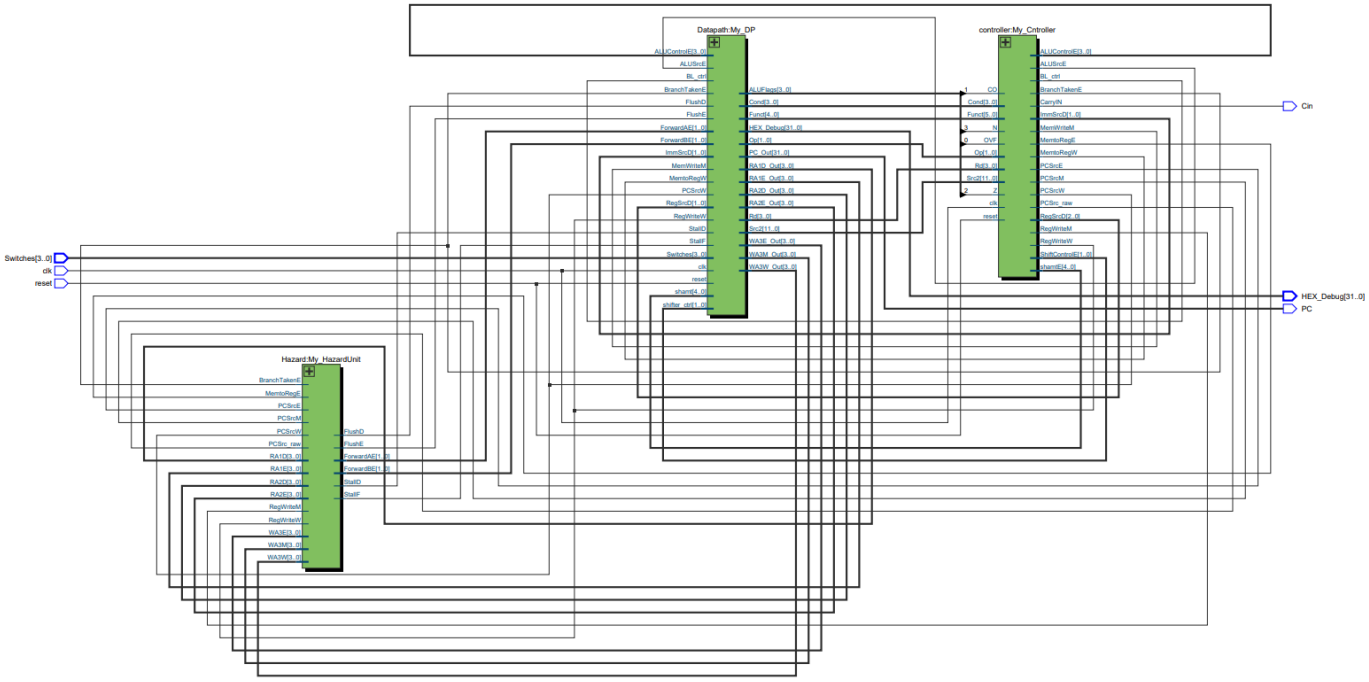
Top Level Design

1) The following diagram shows the Top Level RTL view.



Code Explanation:

- The module Pipeline_Test integrates the data path, controller, and hazard detection unit of a pipelined processor.
- The Datapath module manages data movement and processing within the pipeline stages.
- The Controller module decodes instructions and generates control signals based on the instruction type.
- The Hazard module detects hazards in the pipeline and takes necessary actions to resolve them, such as stalling or flushing pipeline stages.
- Together, these components work in tandem to execute instructions efficiently and handle potential hazards that may arise in a pipelined processor design.

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Test Bench Results:

The code for the Testbench was executed and the results were given below:

(base) PS C:\Users\farru\OneDrive\Desktop\2417152_EE446_Prelim#4\Test> make

bash: C:Usersfarruminiconda3python.exe: command not found

bash: C:Usersfarruminiconda3python.exe: command not found

rm -f results.xml

/usr/bin/make -f Makefile results.xml

make[1]: Entering directory '/c/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test'

bash: C:Usersfarruminiconda3python.exe: command not found

bash: C:Usersfarruminiconda3python.exe: command not found

/c/iverilog/bin/iverilog -o sim_build/sim.vvp -D COCOTB_SIM=1 -s Pipeline_Test -f sim_build/cmds.f -g2012 /c/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/*.v

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:115: warning: Port 2 (RD) of Instruction_memory expects 32 bits, got 1.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:115: : Padding 31 high bits of the port.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:128: warning: Port 4 (DATA) of Register_rsten expects 32 bits, got 1.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:128: : Padding 31 high bits of the port.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:138: warning: Port 5 (OUT) of Register_rsten expects 32 bits, got 1.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:138: : Padding 31 high bits of the port.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:163: warning: Port 3 (input_1) of Mux_2to1 expects 32 bits, got 4.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:163: : Padding 28 high bits of the port.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:163: warning: Port 4 (output_value) of Mux_2to1 expects 32 bits, got 1.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:163: : Padding 31 high bits of the port.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:171: warning: Port 3 (input_1) of Mux_2to1 expects 32 bits, got 1.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:171: : Padding 31 high bits of the port.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:171: warning: Port 4 (output_value) of Mux_2to1 expects 32 bits, got 1.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:171: : Padding 31 high bits of the port.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:180: warning: Port 7 (Destination_select) of Register_file expects 4 bits, got 1.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:180: : Padding 3 high bits of the port.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:180: warning: Port 8 (DATA) of Register_file expects 32 bits, got 1.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:180: : Padding 31 high bits of the port.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:241: warning: Port 3 (DATA) of Register_reset expects 4 bits, got 1.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:241: : Padding 3 high bits of the port.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:259: warning: Port 3 (DATA) of Register_reset expects 32 bits, got 1.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:259: : Padding 31 high bits of the port.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:259: warning: Port 4 (OUT) of Register_reset expects 32 bits, got 1.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:259: : Padding 31 high bits of the port.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:270: warning: Port 4 (input_2) of Mux_4to1 expects 32 bits, got 1.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:270: : Padding 31 high bits of the port.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:270: warning: Port 5 (input_3) of Mux_4to1 expects 32 bits, got 1.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:270: : Padding 31 high bits of the port.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:270: warning: Port 6 (output_value) of Mux_4to1 expects 32 bits, got 1.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:270: : Padding 31 high bits of the port.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:280: warning: Port 4 (input_2) of Mux_4to1 expects 32 bits, got 1.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:280: : Padding 31 high bits of the port.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:280: warning: Port 5 (input_3) of Mux_4to1 expects 32 bits, got 1.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:280: : Padding 31 high bits of the port.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:290: warning: Port 4 (output_value) of Mux_2to1 expects 32 bits, got 1.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:290: : Padding 31 high bits of the port.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:298: warning: Port 3 (DATA) of shifter expects 32 bits, got 1.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:298: : Padding 31 high bits of the port.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:298: warning: Port 4 (OUT) of shifter expects 32 bits, got 1.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:298: : Padding (signed) 31 high bits of the port.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:306: warning: Port 3 (DATA_A) of ALU expects 32 bits, got 1.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:306: : Padding 31 high bits of the port.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:306: warning: Port 4 (DATA_B) of ALU expects 32 bits, got 1.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:306: : Padding 31 high bits of the port.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:320: warning: Port 3 (DATA) of Register_reset expects 32 bits, got 1.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:320: : Padding 31 high bits of the port.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:320: warning: Port 4 (OUT) of Register_reset expects 32 bits, got 1.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:320: : Padding 31 high bits of the port.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:329: warning: Port 4 (OUT) of Register_reset expects 4 bits, got 32.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:329: : Padding 28 high bits of the expression.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:338: warning: Port 4 (OUT) of Register_reset expects 32 bits, got 1.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:338: : Padding 31 high bits of the port.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:347: warning: Port 4 (OUT) of Register_reset expects 32 bits, got 1.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:347: : Padding 31 high bits of the port.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:356: warning: Port 3 (ADDR) of Memory expects 32 bits, got 1.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:356: : Padding 31 high bits of the port.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:356: warning: Port 4 (WD) of Memory expects 32 bits, got 1.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:356: : Padding 31 high bits of the port.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:366: warning: Port 4 (OUT) of Register_reset expects 32 bits, got 1.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:366: : Padding 31 high bits of the port.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:376: warning: Port 3 (DATA) of Register_reset expects 32 bits, got 1.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:376: : Padding 31 high bits of the port.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:376: warning: Port 4 (OUT) of Register_reset expects 32 bits, got 1.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:376: : Padding 31 high bits of the port.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:386: warning: Port 3 (DATA) of Register_reset expects 4 bits, got 32.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:386: : Pruning 28 high bits of the expression.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:386: warning: Port 4 (OUT) of Register_reset expects 4 bits, got 32.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:386: : Padding 28 high bits of the expression.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:395: warning: Port 3 (DATA) of Register_reset expects 32 bits, got 1.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:395: : Padding 31 high bits of the port.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:395: warning: Port 4 (OUT) of Register_reset expects 32 bits, got 1.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:395: : Padding 31 high bits of the port.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:403: warning: Port 2 (input_0) of Mux_2to1 expects 32 bits, got 1.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:403: : Padding 31 high bits of the port.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:403: warning: Port 3 (input_1) of Mux_2to1 expects 32 bits, got 1.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:403: : Padding 31 high bits of the port.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:423: warning: Port 1 (const_value) of Constant4 expects 32 bits, got 1.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Datapath.v:423: : Padding 31 high bits of the port.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Pipeline_Test.v:23: warning: Port 5 (RegSrcD) of Datapath expects 2 bits, got 1.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Pipeline_Test.v:23: : Padding 1 high bits of the port.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Pipeline_Test.v:23: warning: Port 12 (ImmSrcD) of Datapath expects 2 bits, got 1.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Pipeline_Test.v:23: : Padding 1 high bits of the port.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Pipeline_Test.v:23: warning: Port 18 (ForwardAE) of Datapath expects 2 bits, got 1.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Pipeline_Test.v:23: : Padding 1 high bits of the port.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Pipeline_Test.v:23: warning: Port 19 (ForwardBE) of Datapath expects 2 bits, got 1.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Pipeline_Test.v:23: : Padding 1 high bits of the port.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Pipeline_Test.v:23: warning: Port 20 (ALUControlE) of Datapath expects 4 bits, got 1.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Pipeline_Test.v:23: : Padding 3 high bits of the port.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Pipeline_Test.v:23: warning: Port 21 (Op) of Datapath expects 2 bits, got 1.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Pipeline_Test.v:23: : Padding 1 high bits of the port.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Pipeline_Test.v:23: warning: Port 22 (Funct) of Datapath expects 5 bits, got 1.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Pipeline_Test.v:23: : Padding 4 high bits of the port.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Pipeline_Test.v:23: warning: Port 23 (Rd) of Datapath expects 4 bits, got 1.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Pipeline_Test.v:23: : Padding 3 high bits of the port.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Pipeline_Test.v:23: warning: Port 24 (Cond) of Datapath expects 4 bits, got 1.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Pipeline_Test.v:23: : Padding 3 high bits of the port.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Pipeline_Test.v:23: warning: Port 25 (Src2) of Datapath expects 12 bits, got 1.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Pipeline_Test.v:23: : Padding 11 high bits of the port.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/controller.v:53: warning: Port 4 (OUT) of Register_reset expects 2 bits, got 1.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/controller.v:53: : Padding 1 high bits of the port.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/controller.v:56: warning: Port 4 (OUT) of Register_reset expects 4 bits, got 1.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/controller.v:56: : Padding 3 high bits of the port.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/controller.v:59: warning: Port 5 (FlagWrite) of Conditional_unit expects 2 bits, got 1.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/controller.v:59: : Padding 1 high bits of the port.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Pipeline_Test.v:67: warning: Port 3 (Op) of controller expects 2 bits, got 1.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Pipeline_Test.v:67: : Padding 1 high bits of the port.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Pipeline_Test.v:67: warning: Port 4 (Funct) of controller expects 6 bits, got 1.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Pipeline_Test.v:67: : Padding 5 high bits of the port.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Pipeline_Test.v:67: warning: Port 5 (Rd) of controller expects 4 bits, got 1.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Pipeline_Test.v:67: : Padding 3 high bits of the port.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Pipeline_Test.v:67: warning: Port 6 (Src2) of controller expects 12 bits, got 1.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Pipeline_Test.v:67: : Padding 11 high bits of the port.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Pipeline_Test.v:67: warning: Port 7 (Cond) of controller expects 4 bits, got 1.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Pipeline_Test.v:67: : Padding 3 high bits of the port.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Pipeline_Test.v:67: warning: Port 12 (ImmSrcD) of controller expects 2 bits, got 1.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Pipeline_Test.v:67: : Padding 1 high bits of the port.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Pipeline_Test.v:67: warning: Port 14 (RegSrcD) of controller expects 3 bits, got 1.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Pipeline_Test.v:67: : Padding 2 high bits of the port.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Pipeline_Test.v:67: warning: Port 15 (ALUControlE) of controller expects 4 bits, got 1.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Pipeline_Test.v:67: : Padding 3 high bits of the port.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Pipeline_Test.v:100: warning: Port 20 (ForwardAE) of Hazard expects 2 bits, got 1.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Pipeline_Test.v:100: : Padding 1 high bits of the port.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Pipeline_Test.v:100: warning: Port 21 (ForwardBE) of Hazard expects 2 bits, got 1.

C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Pipeline_Test.v:100: : Padding 1 high bits of the port.

rm -f results.xml

MODULE=Pipeline_Test TESTCASE= TOPLEVEL=Pipeline_Test TOPLEVEL_LANG=verilog \

/c/iverilog/bin/vvp -M C:/Users/farru/miniconda3/Lib/site-packages/cocotb/libs -m cocotbvpi_icarus sim_build/sim.vvp

-.--ns INFO gpi ..mbed\gpi_embed.cpp:78 in set_program_name_in_venv Did not detect Python virtual environment. Using system-wide Python interpreter

-.--ns INFO gpi ..\gpi\GpiCommon.cpp:101 in gpi_print_registered_impl VPI registered

0.00ns INFO cocotb Running on Icarus Verilog version 12.0 (devel)

0.00ns INFO cocotb Running tests with cocotb v1.8.1 from C:\Users\farru\miniconda3\Lib\site-packages\cocotb

0.00ns INFO cocotb Seeding Python random module with 1713764846

0.00ns INFO cocotb.regression Found test Pipeline_Test.Pipeline_test

0.00ns INFO cocotb.regression running Pipeline_test (1/1)

WARNING: C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Instruction_memory.v:9: $readmemh: The behaviour for reg[...] mem[N:0]; $readmemh("...", mem); changed in the 1364-2005 standard. To avoid ambiguity, use mem[0:N] or explicit range parameters $readmemh("...", mem, start, stop);. Defaulting to 1364-2005 behavior.

WARNING: C:/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test/../HDL/Instruction_memory.v:9: $readmemh(instructions.hex): Not enough words in the file for the requested range [0:255].

10000.00ns DEBUG Performance Model Current Instruction is not executed

4 [0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0] DATA <Helper_lib.Instruction object at 0x000001D7A66FF470>

8 [0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0] DATA <Helper_lib.Instruction object at 0x000001D7A66ED2B0>

12 [0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0] DATA <Helper_lib.Instruction object at 0x000001D7A66EDC40>

16 [0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0] STALLFLUSH -1

20 [0, 19, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 8] STALLFLUSH -1

20 [0, 19, 38, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 12] BRANCH <Helper_lib.Instruction object at 0x000001D7A66ED040>

24 [0, 19, 38, 2, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 16] DATA <Helper_lib.Instruction object at 0x000001D7A6713D10>

28 [0, 19, 38, 2, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 16] DATA <Helper_lib.Instruction object at 0x000001D7A6713140>

32 [0, 19, 38, 2, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 16] DATA <Helper_lib.Instruction object at 0x000001D7A6712A50>

36 [0, 19, 38, 2, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 20] DATA <Helper_lib.Instruction object at 0x000001D7A6713D70>

40 [0, 19, 38, 2, 76, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 28] STR <Helper_lib.Instruction object at 0x000001D7A67132F0>

44 [0, 19, 38, 2, 76, 10, 0, 0, 0, 0, 0, 0, 0, 0, 0, 32] LDR <Helper_lib.Instruction object at 0x000001D7A6713E60>

48 [0, 19, 38, 2, 76, 10, 2147483650, 0, 0, 0, 0, 0, 0, 0, 0, 36] STALLFLUSH -1

48 [0, 19, 38, 2, 76, 10, 2147483650, 4294967288, 0, 0, 0, 0, 0, 0, 0, 40] DATA <Helper_lib.Instruction object at 0x000001D7A67131A0>

52 [0, 19, 38, 2, 76, 10, 2147483650, 4294967288, 0, 0, 0, 0, 0, 0, 0, 44] NOTEXECUTED <Helper_lib.Instruction object at 0x000001D7A663AA80>

56 [0, 19, 38, 2, 76, 10, 2147483650, 4294967288, 38, 0, 0, 0, 0, 0, 0, 48] STALLFLUSH -1

60 [0, 19, 38, 2, 76, 10, 2147483650, 4294967288, 38, 0, 0, 0, 0, 0, 0, 48] STALLFLUSH -1

60 [0, 19, 38, 2, 76, 10, 2147483650, 4294967288, 38, 0, 0, 0, 0, 0, 0, 52] BRANCH <Helper_lib.Instruction object at 0x000001D7A67393D0>

64 [0, 19, 38, 2, 76, 10, 2147483650, 4294967288, 38, 0, 0, 0, 0, 0, 0, 56] STALLFLUSH -1

68 [0, 19, 38, 2, 76, 10, 2147483650, 4294967288, 38, 0, 0, 0, 0, 0, 0, 56] STALLFLUSH -1

76 [0, 19, 38, 2, 76, 10, 2147483650, 4294967288, 38, 0, 0, 0, 0, 0, 0, 56] BRANCH <Helper_lib.Instruction object at 0x000001D7A6738170>

80 [0, 19, 38, 2, 76, 10, 2147483650, 4294967288, 38, 0, 0, 0, 0, 0, 0, 60] STALLFLUSH -1

84 [0, 19, 38, 2, 76, 10, 2147483650, 4294967288, 38, 0, 0, 0, 0, 0, 0, 60] STALLFLUSH -1

64 [0, 19, 38, 2, 76, 10, 2147483650, 4294967288, 38, 0, 0, 0, 0, 0, 0, 60] BRANCH <Helper_lib.Instruction object at 0x000001D7A6738B30>

68 [0, 19, 38, 2, 76, 10, 2147483650, 4294967288, 38, 0, 0, 0, 0, 0, 64, 68] DATA <Helper_lib.Instruction object at 0x000001D7A67381D0>

-1 [0, 19, 38, 2, 76, 10, 2147483650, 4294967288, 38, 0, 0, 0, 0, 0, 64, 68] STALLFLUSH -1

-1 [0, 19, 38, 2, 76, 10, 2147483650, 4294967288, 38, 0, 0, 0, 0, 0, 64, 68] STALLFLUSH -1

-1 [0, 19, 38, 2, 76, 10, 2147483650, 4294967288, 38, 0, 0, 0, 0, 0, 64, 84] STALLFLUSH -1

-1 [816, 19, 38, 2, 76, 10, 2147483650, 4294967288, 38, 0, 0, 0, 0, 0, 64, 72] STALLFLUSH -1

10000.00ns DEBUG Performance Model ********** Clock cycle: 0 **********

10000.00ns DEBUG Performance Model ****** Current Instruction *********

10000.00ns DEBUG Performance Model Binary string:11100011101000000001000000010011

10000.00ns DEBUG Performance Model Operation type Data Processing

10000.00ns DEBUG Performance Model cond:E

10000.00ns DEBUG Performance Model Immediate bit:1

10000.00ns DEBUG Performance Model cmd:D

10000.00ns DEBUG Performance Model Set bit:0

10000.00ns DEBUG Performance Model Rn:0 Rd:1

10000.00ns DEBUG Performance Model rot:0 imm8:19

15000.00ns DEBUG Performance Model ********** DUT DATAPATH Signals **********

My_DP.A = 0

My_DP.ALUControlE = 0000

My_DP.ALUFlags = 0001

My_DP.ALUOutW = 0

My_DP.ALUResultE = 0x00000000

My_DP.ALUSrcE = 0

My_DP.BL_ctrl = x

My_DP.BranchTakenE = 0

My_DP.Cond = 0000

My_DP.Const_Fifteen = 1111

My_DP.Const_Forteen = 1110

My_DP.Const_Four = 0x00000004

My_DP.Const_Zero = 0

My_DP.ExtImmD = 0x00000000

My_DP.ExtImmE = 0x00000000

My_DP.FlushD = 0

My_DP.FlushE = 0

My_DP.ForwardAE = 00

My_DP.ForwardBE = 00

My_DP.Funct = 00000

My_DP.HEX_Debug = 0x00000000

My_DP.ImmSrcD = 00

My_DP.InstructionD = 0x00000000

My_DP.InstructionF = 1

My_DP.MUX0_Out = 0x00000004

My_DP.MUX7_Out = 0x00000000

My_DP.MemWriteM = 0

My_DP.MemtoRegW = 0

My_DP.Op = 00

My_DP.PCD = 0

My_DP.PCE = 0

My_DP.PCF = 0x00000000

My_DP.PCM = 0

My_DP.PCPlus4F = 0x00000004

My_DP.PCSrcW = 0

My_DP.PCWB = 0

My_DP.PC_Out = 0x00000000

My_DP.PC_prime = 0x00000004

My_DP.RA1D = 0000

My_DP.RA1D_Out = 0000

My_DP.RA1E = 0000

My_DP.RA1E_Out = 0000

My_DP.RA2D = 0000

My_DP.RA2D_Out = 0000

My_DP.RA2E = 0000

My_DP.RA2E_Out = 0000

My_DP.RD1D = 0x00000000

My_DP.RD1E = 0x00000000

My_DP.RD2D = 0x00000000

My_DP.RD2E = 0x00000000

My_DP.Rd = 0000

My_DP.ReadDataM = xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx

My_DP.ReadDataW = 0

My_DP.RegSrcD = 00

My_DP.RegWriteW = 0

My_DP.ResultW = 0x00000000

My_DP.Src2 = 000000000000

My_DP.SrcAE = 0

My_DP.StallD = 0

My_DP.StallF = 0

My_DP.Switches = zzzz

My_DP.WA3D = 0

My_DP.WA3E = 0000

My_DP.WA3E_Out = 0000

My_DP.WA3M = 0x00000000

My_DP.WA3M_Out = 0000

My_DP.WA3W = 0x00000000

My_DP.WA3W_Out = 0000

My_DP.WD = 0

My_DP.WD3 = 0

My_DP.clk = 1

My_DP.reset = 0

My_DP.shamt = 00000

My_DP.shift_input = 0

My_DP.shift_output = 0

My_DP.shifter_ctrl = 00

15000.00ns DEBUG Performance Model ********** DUT Controller Signals **********

My_Cntroller.ALUControlE = 0000

My_Cntroller.ALUControl_raw = 0000

My_Cntroller.ALUSrcE = 0

My_Cntroller.ALUSrc_raw = 0

My_Cntroller.BL_ctrl = x

My_Cntroller.BranchE = 0

My_Cntroller.BranchTakenE = 0

My_Cntroller.Branch_raw = x

My_Cntroller.CO = 0

My_Cntroller.CarryIN = 0

My_Cntroller.Cond = 0000

My_Cntroller.CondE = 0

My_Cntroller.CondEx = 0

My_Cntroller.FlagWriteE = 0

My_Cntroller.FlagWrite_raw = 00

My_Cntroller.Funct = 000000

My_Cntroller.ImmSrcD = 00

My_Cntroller.MemWriteE = 0

My_Cntroller.MemWriteM = 0

My_Cntroller.MemWrite_raw = 0

My_Cntroller.MemtoRegE = 0

My_Cntroller.MemtoRegM = 0

My_Cntroller.MemtoRegW = 0

My_Cntroller.MemtoReg_raw = 0

My_Cntroller.N = 0

My_Cntroller.OVF = 1

My_Cntroller.Op = 00

My_Cntroller.PCSrcE = 0

My_Cntroller.PCSrcM = 0

My_Cntroller.PCSrcW = 0

My_Cntroller.PCSrc_raw = 0

My_Cntroller.Rd = 0000

My_Cntroller.RegSrcD = 000

My_Cntroller.RegWriteE = 0

My_Cntroller.RegWriteM = 0

My_Cntroller.RegWriteW = 0

My_Cntroller.RegWrite_raw = 1

My_Cntroller.ShiftControlE = 00

My_Cntroller.ShiftControl_raw= 00

My_Cntroller.Src2 = 000000000000

My_Cntroller.Z = 0

My_Cntroller.clk = 1

My_Cntroller.reset = 0

My_Cntroller.shamtE = 00000

My_Cntroller.shamt_raw = 00000

16000.00ns DEBUG Performance Model ********** Performance Model / DUT Data **********

16000.00ns DEBUG Performance Model PC:0x4 PC:0x4

16000.00ns DEBUG Performance Model Register:0: 0x0 0x0

16000.00ns DEBUG Performance Model Register:1: 0x0 0x0

16000.00ns DEBUG Performance Model Register:2: 0x0 0x0

16000.00ns DEBUG Performance Model Register:3: 0x0 0x0

16000.00ns DEBUG Performance Model Register:4: 0x0 0x0

16000.00ns DEBUG Performance Model Register:5: 0x0 0x0

16000.00ns DEBUG Performance Model Register:6: 0x0 0x0

16000.00ns DEBUG Performance Model Register:7: 0x0 0x0

16000.00ns DEBUG Performance Model Register:8: 0x0 0x0

16000.00ns DEBUG Performance Model Register:9: 0x0 0x0

16000.00ns DEBUG Performance Model Register:10: 0x0 0x0

16000.00ns DEBUG Performance Model Register:11: 0x0 0x0

16000.00ns DEBUG Performance Model Register:12: 0x0 0x0

16000.00ns DEBUG Performance Model Register:13: 0x0 0x0

16000.00ns DEBUG Performance Model Register:14: 0x0 0x0

16000.00ns DEBUG Performance Model Register:15: Not checked 0x8

16000.00ns DEBUG Performance Model ********** Clock cycle: 1 **********

16000.00ns DEBUG Performance Model ****** Current Instruction *********

16000.00ns DEBUG Performance Model Binary string:11100000100000010010000000000001

16000.00ns DEBUG Performance Model Operation type Data Processing

16000.00ns DEBUG Performance Model cond:E

16000.00ns DEBUG Performance Model Immediate bit:0

16000.00ns DEBUG Performance Model cmd:4

16000.00ns DEBUG Performance Model Set bit:0

16000.00ns DEBUG Performance Model Rn:1 Rd:2

16000.00ns DEBUG Performance Model shamt5:0 sh:0 Rm:1

25000.00ns DEBUG Performance Model ********** DUT DATAPATH Signals **********

My_DP.A = 0

My_DP.ALUControlE = 0000

My_DP.ALUFlags = 0001

My_DP.ALUOutW = 0

My_DP.ALUResultE = 0x00000000

My_DP.ALUSrcE = 0

My_DP.BL_ctrl = x

My_DP.BranchTakenE = 0

My_DP.Cond = 0000

My_DP.Const_Fifteen = 1111

My_DP.Const_Forteen = 1110

My_DP.Const_Four = 0x00000004

My_DP.Const_Zero = 0

My_DP.ExtImmD = 0x00000000

My_DP.ExtImmE = 0x00000000

My_DP.FlushD = 0

My_DP.FlushE = 0

My_DP.ForwardAE = 00

My_DP.ForwardBE = 00

My_DP.Funct = 00000

My_DP.HEX_Debug = 0x00000000

My_DP.ImmSrcD = 00

My_DP.InstructionD = 0x00000000

My_DP.InstructionF = 1

My_DP.MUX0_Out = 0x00000008

My_DP.MUX7_Out = 0x00000000

My_DP.MemWriteM = 0

My_DP.MemtoRegW = 0

My_DP.Op = 00

My_DP.PCD = 0

My_DP.PCE = 0

My_DP.PCF = 0x00000004

My_DP.PCM = 0

My_DP.PCPlus4F = 0x00000008

My_DP.PCSrcW = 0

My_DP.PCWB = 0

My_DP.PC_Out = 0x00000004

My_DP.PC_prime = 0x00000008

My_DP.RA1D = 0000

My_DP.RA1D_Out = 0000

My_DP.RA1E = 0000

My_DP.RA1E_Out = 0000

My_DP.RA2D = 0000

My_DP.RA2D_Out = 0000

My_DP.RA2E = 0000

My_DP.RA2E_Out = 0000

My_DP.RD1D = 0x00000000

My_DP.RD1E = 0x00000000

My_DP.RD2D = 0x00000000

My_DP.RD2E = 0x00000000

My_DP.Rd = 0000

My_DP.ReadDataM = xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx

My_DP.ReadDataW = x

My_DP.RegSrcD = 00

My_DP.RegWriteW = 0

My_DP.ResultW = 00000000000000000000000000000000x

My_DP.Src2 = 000000000000

My_DP.SrcAE = 0

My_DP.StallD = 0

My_DP.StallF = 0

My_DP.Switches = zzzz

My_DP.WA3D = 0

My_DP.WA3E = 0000

My_DP.WA3E_Out = 0000

My_DP.WA3M = 0x00000000

My_DP.WA3M_Out = 0000

My_DP.WA3W = 0x00000000

My_DP.WA3W_Out = 0000

My_DP.WD = 0

My_DP.WD3 = x

My_DP.clk = 1

My_DP.reset = 0

My_DP.shamt = 00000

My_DP.shift_input = 0

My_DP.shift_output = 0

My_DP.shifter_ctrl = 00

25000.00ns DEBUG Performance Model ********** DUT Controller Signals **********

My_Cntroller.ALUControlE = 0000

My_Cntroller.ALUControl_raw = 0000

My_Cntroller.ALUSrcE = 0

My_Cntroller.ALUSrc_raw = 0

My_Cntroller.BL_ctrl = x

My_Cntroller.BranchE = x

My_Cntroller.BranchTakenE = 0

My_Cntroller.Branch_raw = x

My_Cntroller.CO = 0

My_Cntroller.CarryIN = 0

My_Cntroller.Cond = 0000

My_Cntroller.CondE = 0

My_Cntroller.CondEx = 0

My_Cntroller.FlagWriteE = 0

My_Cntroller.FlagWrite_raw = 00

My_Cntroller.Funct = 000000

My_Cntroller.ImmSrcD = 00

My_Cntroller.MemWriteE = 0

My_Cntroller.MemWriteM = 0

My_Cntroller.MemWrite_raw = 0

My_Cntroller.MemtoRegE = 0

My_Cntroller.MemtoRegM = 0

My_Cntroller.MemtoRegW = 0

My_Cntroller.MemtoReg_raw = 0

My_Cntroller.N = 0

My_Cntroller.OVF = 1

My_Cntroller.Op = 00

My_Cntroller.PCSrcE = 0

My_Cntroller.PCSrcM = 0

My_Cntroller.PCSrcW = 0

My_Cntroller.PCSrc_raw = 0

My_Cntroller.Rd = 0000

My_Cntroller.RegSrcD = 000

My_Cntroller.RegWriteE = 1

My_Cntroller.RegWriteM = 0

My_Cntroller.RegWriteW = 0

My_Cntroller.RegWrite_raw = 1

My_Cntroller.ShiftControlE = 00

My_Cntroller.ShiftControl_raw= 00

My_Cntroller.Src2 = 000000000000

My_Cntroller.Z = 0

My_Cntroller.clk = 1

My_Cntroller.reset = 0

My_Cntroller.shamtE = 00000

My_Cntroller.shamt_raw = 00000

26000.00ns DEBUG Performance Model ********** Performance Model / DUT Data **********

26000.00ns DEBUG Performance Model PC:0x8 PC:0x8

26000.00ns DEBUG Performance Model Register:0: 0x0 0x0

26000.00ns DEBUG Performance Model Register:1: 0x0 0x0

26000.00ns DEBUG Performance Model Register:2: 0x0 0x0

26000.00ns DEBUG Performance Model Register:3: 0x0 0x0

26000.00ns DEBUG Performance Model Register:4: 0x0 0x0

26000.00ns DEBUG Performance Model Register:5: 0x0 0x0

```
26000.00ns DEBUG    Performance Model          Register:6: 0x0        0x0
26000.00ns DEBUG    Performance Model          Register:7: 0x0        0x0
26000.00ns DEBUG    Performance Model          Register:8: 0x0        0x0
26000.00ns DEBUG    Performance Model          Register:9: 0x0        0x0
26000.00ns DEBUG    Performance Model          Register:10: 0x0       0x0
26000.00ns DEBUG    Performance Model          Register:11: 0x0       0x0
26000.00ns DEBUG    Performance Model          Register:12: 0x0       0x0
26000.00ns DEBUG    Performance Model          Register:13: 0x0       0x0
26000.00ns DEBUG    Performance Model          Register:14: 0x0       0x0
26000.00ns DEBUG    Performance Model          Register:15: Not checked       0xc
26000.00ns DEBUG    Performance Model          ********** Clock cycle: 2 **********
26000.00ns DEBUG    Performance Model          ****** Current Instruction *********
26000.00ns DEBUG    Performance Model          Binary string:11100000000000010011000000000010
26000.00ns DEBUG    Performance Model          Operation type Data Processing
26000.00ns DEBUG    Performance Model          cond:E
26000.00ns DEBUG    Performance Model          Immediate bit:0
26000.00ns DEBUG    Performance Model          cmd:0
26000.00ns DEBUG    Performance Model          Set bit:0
26000.00ns DEBUG    Performance Model          Rn:1    Rd:3
26000.00ns DEBUG    Performance Model          shamt5:0       sh:0    Rm:2
35000.00ns DEBUG    Performance Model          ********** DUT DATAPATH Signals **********
My_DP.A             = 0
My_DP.ALUControlE   = 0000
My_DP.ALUFlags      = 0001
My_DP.ALUOutW       = 0
My_DP.ALUResultE    = 0x00000000
My_DP.ALUSrcE       = 0
My_DP.BL_ctrl       = x
My_DP.BranchTakenE  = 0
My_DP.Cond          = 0000
My_DP.Const_Fifteen = 1111
My_DP.Const_Forteen = 1110
My_DP.Const_Four    = 0x00000004
```

My_DP.Const_Zero = 0

My_DP.ExtImmD = 0x00000000

My_DP.ExtImmE = 0x00000000

My_DP.FlushD = 0

My_DP.FlushE = 0

My_DP.ForwardAE = 00

My_DP.ForwardBE = 00

My_DP.Funct = 00000

My_DP.HEX_Debug = 0x00000000

My_DP.ImmSrcD = 00

My_DP.InstructionD = 0x00000000

My_DP.InstructionF = 0

My_DP.MUX0_Out = 0x0000000c

My_DP.MUX7_Out = 0x00000000

My_DP.MemWriteM = 0

My_DP.MemtoRegW = 0

My_DP.Op = 00

My_DP.PCD = 0

My_DP.PCE = 0

My_DP.PCF = 0x00000008

My_DP.PCM = 0

My_DP.PCPlus4F = 0x0000000c

My_DP.PCSrcW = 0

My_DP.PCWB = 0

My_DP.PC_Out = 0x00000008

My_DP.PC_prime = 0x0000000c

My_DP.RA1D = 0000

My_DP.RA1D_Out = 0000

My_DP.RA1E = 0000

My_DP.RA1E_Out = 0000

My_DP.RA2D = 0000

My_DP.RA2D_Out = 0000

My_DP.RA2E = 0000

My_DP.RA2E_Out = 0000

My_DP.RD1D = 0x00000000

My_DP.RD1E = 0x00000000

My_DP.RD2D = 0x00000000

My_DP.RD2E = 0x00000000

My_DP.Rd = 0000

My_DP.ReadDataM = xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx

My_DP.ReadDataW = x

My_DP.RegSrcD = 00

My_DP.RegWriteW = 0

My_DP.ResultW = 00000000000000000000000000000000x

My_DP.Src2 = 000000000000

My_DP.SrcAE = 0

My_DP.StallD = 0

My_DP.StallF = 0

My_DP.Switches = zzzz

My_DP.WA3D = 0

My_DP.WA3E = 0000

My_DP.WA3E_Out = 0000

My_DP.WA3M = 0x00000000

My_DP.WA3M_Out = 0000

My_DP.WA3W = 0x00000000

My_DP.WA3W_Out = 0000

My_DP.WD = 0

My_DP.WD3 = x

My_DP.clk = 1

My_DP.reset = 0

My_DP.shamt = 00000

My_DP.shift_input = 0

My_DP.shift_output = 0

My_DP.shifter_ctrl = 00

35000.00ns DEBUG Performance Model ********** DUT Controller Signals **********

My_Cntroller.ALUControlE = 0000

My_Cntroller.ALUControl_raw = 0000

My_Cntroller.ALUSrcE = 0

My_Cntroller.ALUSrc_raw = 0

My_Cntroller.BL_ctrl = x

My_Cntroller.BranchE = x

My_Cntroller.BranchTakenE = 0

My_Cntroller.Branch_raw = x

My_Cntroller.CO = 0

My_Cntroller.CarryIN = 0

My_Cntroller.Cond = 0000

My_Cntroller.CondE = 0

My_Cntroller.CondEx = 0

My_Cntroller.FlagWriteE = 0

My_Cntroller.FlagWrite_raw = 00

My_Cntroller.Funct = 000000

My_Cntroller.ImmSrcD = 00

My_Cntroller.MemWriteE = 0

My_Cntroller.MemWriteM = 0

My_Cntroller.MemWrite_raw = 0

My_Cntroller.MemtoRegE = 0

My_Cntroller.MemtoRegM = 0

My_Cntroller.MemtoRegW = 0

My_Cntroller.MemtoReg_raw = 0

My_Cntroller.N = 0

My_Cntroller.OVF = 1

My_Cntroller.Op = 00

My_Cntroller.PCSrcE = 0

My_Cntroller.PCSrcM = 0

My_Cntroller.PCSrcW = 0

My_Cntroller.PCSrc_raw = 0

My_Cntroller.Rd = 0000

My_Cntroller.RegSrcD = 000

My_Cntroller.RegWriteE = 1

My_Cntroller.RegWriteM = 0

My_Cntroller.RegWriteW = 0

My_Cntroller.RegWrite_raw = 1

My_Cntroller.ShiftControlE = 00

My_Cntroller.ShiftControl_raw= 00

My_Cntroller.Src2 = 000000000000

My_Cntroller.Z = 0

My_Cntroller.clk = 1

My_Cntroller.reset = 0

My_Cntroller.shamtE = 00000

My_Cntroller.shamt_raw = 00000

36000.00ns DEBUG Performance Model ********** Performance Model / DUT Data **********

36000.00ns DEBUG Performance Model PC:0xc PC:0xc

36000.00ns DEBUG Performance Model Register:0: 0x0 0x0

36000.00ns DEBUG Performance Model Register:1: 0x0 0x0

36000.00ns DEBUG Performance Model Register:2: 0x0 0x0

36000.00ns DEBUG Performance Model Register:3: 0x0 0x0

36000.00ns DEBUG Performance Model Register:4: 0x0 0x0

36000.00ns DEBUG Performance Model Register:5: 0x0 0x0

36000.00ns DEBUG Performance Model Register:6: 0x0 0x0

36000.00ns DEBUG Performance Model Register:7: 0x0 0x0

36000.00ns DEBUG Performance Model Register:8: 0x0 0x0

36000.00ns DEBUG Performance Model Register:9: 0x0 0x0

36000.00ns DEBUG Performance Model Register:10: 0x0 0x0

36000.00ns DEBUG Performance Model Register:11: 0x0 0x0

36000.00ns DEBUG Performance Model Register:12: 0x0 0x0

36000.00ns DEBUG Performance Model Register:13: 0x0 0x0

36000.00ns DEBUG Performance Model Register:14: 0x0 0x0

36000.00ns DEBUG Performance Model Register:15: Not checked 0x10

36000.00ns DEBUG Performance Model ********** Clock cycle: 3 **********

36000.00ns DEBUG Performance Model Computer is stalled for this cycle

45000.00ns DEBUG Performance Model ********** DUT DATAPATH Signals **********

My_DP.A = 0

My_DP.ALUControlE = 0000

My_DP.ALUFlags = 0001

My_DP.ALUOutW = 0

My_DP.ALUResultE = 0x00000000

My_DP.ALUSrcE = 0

My_DP.BL_ctrl = x

My_DP.BranchTakenE = 0

My_DP.Cond = 0000

My_DP.Const_Fifteen = 1111

My_DP.Const_Forteen = 1110

My_DP.Const_Four = 0x00000004

My_DP.Const_Zero = 0

My_DP.ExtImmD = 0x00000000

My_DP.ExtImmE = 0x00000000

My_DP.FlushD = 0

My_DP.FlushE = 0

My_DP.ForwardAE = 00

My_DP.ForwardBE = 00

My_DP.Funct = 00000

My_DP.HEX_Debug = 0x00000000

My_DP.ImmSrcD = 00

My_DP.InstructionD = 0x00000000

My_DP.InstructionF = 0

My_DP.MUX0_Out = 0x00000010

My_DP.MUX7_Out = 0x00000000

My_DP.MemWriteM = 0

My_DP.MemtoRegW = 0

My_DP.Op = 00

My_DP.PCD = 0

My_DP.PCE = 0

My_DP.PCF = 0x0000000c

My_DP.PCM = 0

My_DP.PCPlus4F = 0x00000010

My_DP.PCSrcW = 0

My_DP.PCWB = 0

My_DP.PC_Out = 0x0000000c

My_DP.PC_prime = 0x00000010

My_DP.RA1D = 0000

My_DP.RA1D_Out = 0000

My_DP.RA1E = 0000

My_DP.RA1E_Out = 0000

My_DP.RA2D = 0000

My_DP.RA2D_Out = 0000

My_DP.RA2E = 0000

My_DP.RA2E_Out = 0000

My_DP.RD1D = 0x00000000

My_DP.RD1E = 0x00000000

My_DP.RD2D = 0x00000000

My_DP.RD2E = 0x00000000

My_DP.Rd = 0000

My_DP.ReadDataM = xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx

My_DP.ReadDataW = x

My_DP.RegSrcD = 00

My_DP.RegWriteW = 0

My_DP.ResultW = 00000000000000000000000000000000x

My_DP.Src2 = 000000000000

My_DP.SrcAE = 0

My_DP.StallD = 0

My_DP.StallF = 0

My_DP.Switches = zzzz

My_DP.WA3D = 0

My_DP.WA3E = 0000

My_DP.WA3E_Out = 0000

My_DP.WA3M = 0x00000000

My_DP.WA3M_Out = 0000

My_DP.WA3W = 0x00000000

My_DP.WA3W_Out = 0000

My_DP.WD = 0

My_DP.WD3 = x

My_DP.clk = 1

My_DP.reset = 0

My_DP.shamt = 00000

My_DP.shift_input = 0

My_DP.shift_output = 0

My_DP.shifter_ctrl = 00

45000.00ns DEBUG Performance Model ********** DUT Controller Signals **********

My_Cntroller.ALUControlE = 0000

My_Cntroller.ALUControl_raw = 0000

My_Cntroller.ALUSrcE = 0

My_Cntroller.ALUSrc_raw = 0

My_Cntroller.BL_ctrl = x

My_Cntroller.BranchE = x

My_Cntroller.BranchTakenE = 0

My_Cntroller.Branch_raw = x

My_Cntroller.CO = 0

My_Cntroller.CarryIN = 0

My_Cntroller.Cond = 0000

My_Cntroller.CondE = 0

My_Cntroller.CondEx = 0

My_Cntroller.FlagWriteE = 0

My_Cntroller.FlagWrite_raw = 00

My_Cntroller.Funct = 000000

My_Cntroller.ImmSrcD = 00

My_Cntroller.MemWriteE = 0

My_Cntroller.MemWriteM = 0

My_Cntroller.MemWrite_raw = 0

My_Cntroller.MemtoRegE = 0

My_Cntroller.MemtoRegM = 0

My_Cntroller.MemtoRegW = 0

My_Cntroller.MemtoReg_raw = 0

My_Cntroller.N = 0

My_Cntroller.OVF = 1

My_Cntroller.Op = 00

My_Cntroller.PCSrcE = 0

My_Cntroller.PCSrcM = 0

My_Cntroller.PCSrcW = 0

My_Cntroller.PCSrc_raw = 0

My_Cntroller.Rd = 0000

My_Cntroller.RegSrcD = 000

My_Cntroller.RegWriteE = 1

My_Cntroller.RegWriteM = 0

My_Cntroller.RegWriteW = 0

My_Cntroller.RegWrite_raw = 1

My_Cntroller.ShiftControlE = 00

My_Cntroller.ShiftControl_raw= 00

My_Cntroller.Src2 = 000000000000

My_Cntroller.Z = 0

My_Cntroller.clk = 1

My_Cntroller.reset = 0

My_Cntroller.shamtE = 00000

My_Cntroller.shamt_raw = 00000

46000.00ns DEBUG Performance Model ********** Performance Model / DUT Data **********

46000.00ns DEBUG Performance Model PC:0x10 PC:0x10

46000.00ns DEBUG Performance Model Register:0: 0x0 0x0

46000.00ns DEBUG Performance Model Register:1: 0x0 0x0

46000.00ns DEBUG Performance Model Register:2: 0x0 0x0

46000.00ns DEBUG Performance Model Register:3: 0x0 0x0

46000.00ns DEBUG Performance Model Register:4: 0x0 0x0

46000.00ns DEBUG Performance Model Register:5: 0x0 0x0

46000.00ns DEBUG Performance Model Register:6: 0x0 0x0

46000.00ns DEBUG Performance Model Register:7: 0x0 0x0

46000.00ns DEBUG Performance Model Register:8: 0x0 0x0

46000.00ns DEBUG Performance Model Register:9: 0x0 0x0

46000.00ns DEBUG Performance Model Register:10: 0x0 0x0

46000.00ns DEBUG Performance Model Register:11: 0x0 0x0

46000.00ns DEBUG Performance Model Register:12: 0x0 0x0

46000.00ns DEBUG Performance Model Register:13: 0x0 0x0

46000.00ns DEBUG Performance Model Register:14: 0x0 0x0

46000.00ns DEBUG Performance Model Register:15: Not checked 0x14

46000.00ns DEBUG Performance Model ********** Clock cycle: 4 **********

46000.00ns DEBUG Performance Model Computer is stalled for this cycle

55000.00ns DEBUG Performance Model ********** DUT DATAPATH Signals **********

My_DP.A = 0

My_DP.ALUControlE = 0000

My_DP.ALUFlags = 0001

My_DP.ALUOutW = 0

My_DP.ALUResultE = 0x00000000

My_DP.ALUSrcE = 0

My_DP.BL_ctrl = x

My_DP.BranchTakenE = 0

My_DP.Cond = 0000

My_DP.Const_Fifteen = 1111

My_DP.Const_Forteen = 1110

My_DP.Const_Four = 0x00000004

My_DP.Const_Zero = 0

My_DP.ExtImmD = 0x00000000

My_DP.ExtImmE = 0x00000000

My_DP.FlushD = 0

My_DP.FlushE = 0

My_DP.ForwardAE = 00

My_DP.ForwardBE = 00

My_DP.Funct = 00000

My_DP.HEX_Debug = 0x00000000

My_DP.ImmSrcD = 00

My_DP.InstructionD = 0x00000000

My_DP.InstructionF = 0

My_DP.MUX0_Out = 0x00000014

My_DP.MUX7_Out = 0x00000000

My_DP.MemWriteM = 0

My_DP.MemtoRegW = 0

My_DP.Op = 00

My_DP.PCD = 0

My_DP.PCE = 0

My_DP.PCF = 0x00000010

My_DP.PCM = 0

My_DP.PCPlus4F = 0x00000014

My_DP.PCSrcW = 0

My_DP.PCWB = 0

My_DP.PC_Out = 0x00000010

My_DP.PC_prime = 0x00000014

My_DP.RA1D = 0000

My_DP.RA1D_Out = 0000

My_DP.RA1E = 0000

My_DP.RA1E_Out = 0000

My_DP.RA2D = 0000

My_DP.RA2D_Out = 0000

My_DP.RA2E = 0000

My_DP.RA2E_Out = 0000

My_DP.RD1D = 0x00000000

My_DP.RD1E = 0x00000000

My_DP.RD2D = 0x00000000

My_DP.RD2E = 0x00000000

My_DP.Rd = 0000

My_DP.ReadDataM = xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx

My_DP.ReadDataW = x

My_DP.RegSrcD = 00

My_DP.RegWriteW = 0

My_DP.ResultW = 00000000000000000000000000000000x

My_DP.Src2 = 000000000000

My_DP.SrcAE = 0

My_DP.StallD = 0

My_DP.StallF = 0

My_DP.Switches = zzzz

My_DP.WA3D = 0

My_DP.WA3E = 0000

My_DP.WA3E_Out = 0000

My_DP.WA3M = 0x00000000

My_DP.WA3M_Out = 0000

My_DP.WA3W = 0x00000000

My_DP.WA3W_Out = 0000

My_DP.WD = 0

My_DP.WD3 = x

My_DP.clk = 1

My_DP.reset = 0

My_DP.shamt = 00000

My_DP.shift_input = 0

My_DP.shift_output = 0

My_DP.shifter_ctrl = 00

55000.00ns DEBUG Performance Model ********** DUT Controller Signals **********

My_Cntroller.ALUControlE = 0000

My_Cntroller.ALUControl_raw = 0000

My_Cntroller.ALUSrcE = 0

My_Cntroller.ALUSrc_raw = 0

My_Cntroller.BL_ctrl = x

My_Cntroller.BranchE = x

My_Cntroller.BranchTakenE = 0

My_Cntroller.Branch_raw = x

My_Cntroller.CO = 0

My_Cntroller.CarryIN = 0

My_Cntroller.Cond = 0000

My_Cntroller.CondE = 0

My_Cntroller.CondEx = 0

My_Cntroller.FlagWriteE = 0

My_Cntroller.FlagWrite_raw = 00

My_Cntroller.Funct = 000000

My_Cntroller.ImmSrcD = 00

My_Cntroller.MemWriteE = 0

My_Cntroller.MemWriteM = 0

My_Cntroller.MemWrite_raw = 0

My_Cntroller.MemtoRegE = 0

My_Cntroller.MemtoRegM = 0

My_Cntroller.MemtoRegW = 0

My_Cntroller.MemtoReg_raw = 0

My_Cntroller.N = 0

My_Cntroller.OVF = 1

My_Cntroller.Op = 00

My_Cntroller.PCSrcE = 0

My_Cntroller.PCSrcM = 0

My_Cntroller.PCSrcW = 0

My_Cntroller.PCSrc_raw = 0

My_Cntroller.Rd = 0000

My_Cntroller.RegSrcD = 000

My_Cntroller.RegWriteE = 1

My_Cntroller.RegWriteM = 0

My_Cntroller.RegWriteW = 0

My_Cntroller.RegWrite_raw = 1

My_Cntroller.ShiftControlE = 00

My_Cntroller.ShiftControl_raw= 00

My_Cntroller.Src2 = 000000000000

My_Cntroller.Z = 0

My_Cntroller.clk = 1

My_Cntroller.reset = 0

```
My_Cntroller.shamtE          = 00000

My_Cntroller.shamt_raw       = 00000

 56000.00ns DEBUG    Performance Model               ********** Performance Model / DUT Data **********

 56000.00ns DEBUG    Performance Model               PC:0x14         PC:0x14

 56000.00ns DEBUG    Performance Model               Register:0: 0x0         0x0

 56000.00ns DEBUG    Performance Model               Register:1: 0x13        0x0

 56000.00ns DEBUG    Performance Model               Register:2: 0x0         0x0

 56000.00ns DEBUG    Performance Model               Register:3: 0x0         0x0

 56000.00ns DEBUG    Performance Model               Register:4: 0x0         0x0

 56000.00ns DEBUG    Performance Model               Register:5: 0x0         0x0

 56000.00ns DEBUG    Performance Model               Register:6: 0x0         0x0

 56000.00ns DEBUG    Performance Model               Register:7: 0x0         0x0

 56000.00ns DEBUG    Performance Model               Register:8: 0x0         0x0

 56000.00ns DEBUG    Performance Model               Register:9: 0x0         0x0

 56000.00ns DEBUG    Performance Model               Register:10: 0x0        0x0

 56000.00ns DEBUG    Performance Model               Register:11: 0x0        0x0

 56000.00ns DEBUG    Performance Model               Register:12: 0x0        0x0

 56000.00ns DEBUG    Performance Model               Register:13: 0x0        0x0

 56000.00ns DEBUG    Performance Model               Register:14: 0x0        0x0

 56000.00ns DEBUG    Performance Model               Register:15: Not checked        0x18

 57000.00ns INFO     cocotb.regression               Pipeline_test failed

                                                     Traceback (most recent call last):

                                                       File "C:\Users\farru\OneDrive\Desktop\Pipeline\Test\Pipeline_Test.py", line 230,
in Pipeline_test

                                                       File "C:\Users\farru\OneDrive\Desktop\Pipeline\Test\Pipeline_Test.py", line 215,
in run_test

                                                       File "C:\Users\farru\OneDrive\Desktop\Pipeline\Test\Pipeline_Test.py", line 57,
in compare_result

                                                     AssertionError: assert 19 == 00000000000000000000000000000000

                                                      +  where 00000000000000000000000000000000 =
ModifiableObject(Pipeline_Test.My_DP.My_RegFile.Reg_Out[1]).value

 57000.00ns INFO     cocotb.regression
**************************************************************************************
```

```
                    ** TEST                    STATUS  SIM TIME (ns)  REAL TIME (s)  RATIO (ns/s)
**

*******************************************************************************

                    ** Pipeline_Test.Pipeline_test    FAIL       57000.00          0.08     685841.20  **

*******************************************************************************

                    ** TESTS=1 PASS=0 FAIL=1 SKIP=0             57000.00          0.15     384416.16
**

*******************************************************************************

make[1]: Leaving directory '/c/Users/farru/OneDrive/Desktop/2417152_EE446_Prelim#4/Test'
```