Semiconductor Engineering

:Semiconductor Physics and Devices

Summary

Chapter 3. Metal-Semiconductor Contacts

Equilibrium in electronic systems

Why metal-semiconductor contact is important?

Most of the electronic devices that make up an integrated circuit are connected by means of metal-semiconductor contacts.

the nature of the thermal equilibrium that is established when a metal and a semiconductor are in intimate contact

underlie the basic properties of **semiconductor *pn* junctions** as well as the properties of interfaces between **semiconductors and insulators** and between **metals and insulators.**

Metal-semiconductor contact

Schottky theory

→ **ohmic** and **rectifying behavior** in various metal-semiconductor system

Equilibrium in electronic systems

Metal-Semiconductor System

Using the concepts developed in Chapter 1, we recognize that these systems of allowed states can be regarded as being almost entirely populated at energies less than the Fermi energy and nearly vacant at higher energies..

When the metal and the semiconductor are remote from one another (do not interact)

→ both the systems of electronic states and their Fermi levels are independent

Let us designate the metal as state-system number 1
the semiconductor as state-system number 2.

Each system has a density of allowed states $g(E)$ per unit energy.
Of these $g(E)$ states, $n(E)$ are full and $v(E)$ are empty.

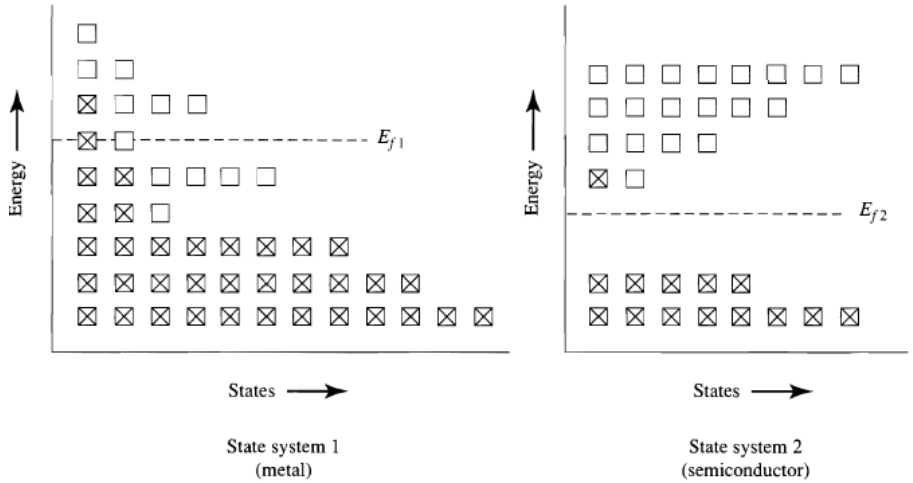


FIGURE 3.1 Allowed electronic-energy-state systems for two isolated materials. States marked with an × are filled; those unmarked are empty. System 1 is a qualitative representation of a metal; system 2 qualitatively represents a semiconductor.

Equilibrium in electronic systems

Metal-Semiconductor System

- The Fermi-Dirac distribution functions

$$f_{D1,2} = \frac{1}{1 + \exp[(E - E_{f1,2})/kT]}$$

- The filled state density $n_{1,2} = g_{1,2} \times f_{D1,2}$
- The vacant state density $v_{1,2} = g_{1,2} \times (1 - f_{D1,2})$

Because of the Pauli exclusion principle,
the available state density is not $g(E_x)$, the state density, but $v(E_x)$, the vacant-state density

The proportionality factor relating the transfer probability

is the same for transfer from system 1 to system 2 as it is for transfer from system 2 to system 1

at thermal equilibrium

$\longrightarrow \quad n_1 \times v_2 = n_2 \times v_1 \quad \Rightarrow \quad f_{D1}g_1g_2 = f_{D2}g_2g_1$

⇒ We therefore have established the important property of any two systems in thermal equilibrium: they have the same Fermi energy.

Regardless of the detailed nature of these functions, a statement that their Fermi levels are equal is equivalent to stating that the two systems are in thermal equilibrium

⇒ *At thermal equilibrium, the Fermi level* is *constant throughout a system.*

Idealized Metal-Semiconductor Junction

Band Diagram

Specific cases of the allowed energy states for gold and for silicon

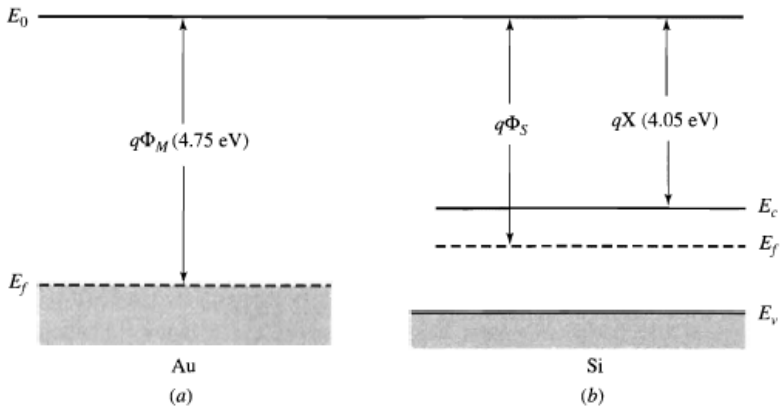


FIGURE 3.3 Pertinent energy levels for the metal gold and the semiconductor silicon. Only the work function is given for the metal, whereas the semiconductor is described by the work function $q\Phi_S$, the electron affinity $q\chi_S$, and the band gap ($E_c - E_v$).

$\boldsymbol{E_o}$: the energy that an electron would have if it were just free of the influence of the given material

⟶ a convenient reference level for energy is taken to be the vacuum or free-electron energy

Work function : The difference between E_o and E_f

usually given the symbol qΦ in energy units and often listed as Φ in volts for particular materials

Idealized Metal-Semiconductor Junction

Band Diagram

In the case of the semiconductor

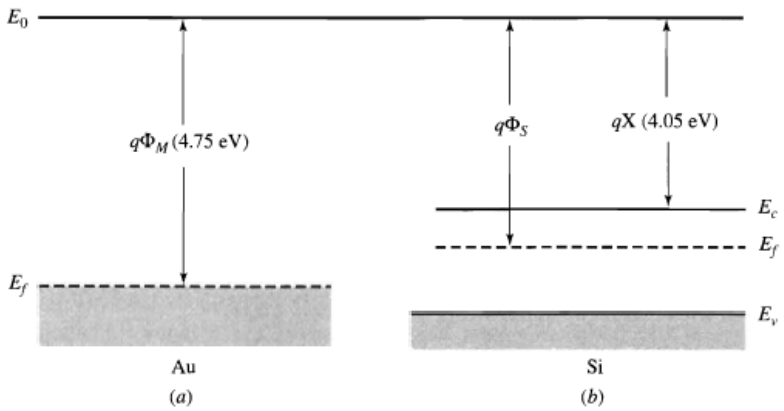


FIGURE 3.3 Pertinent energy levels for the metal gold and the semiconductor silicon. Only the work function is given for the metal, whereas the semiconductor is described by the work function $q\Phi_S$, the electron affinity $q\chi_S$, and the band gap ($E_c - E_v$).

because E_f changes position within the gap separating E_v and E_c as the doping is varied,

the difference between E_o and E_f is a function of the dopant concentration of the semiconductor

The difference between the vacuum level (E_0) and the conduction-band edge (E_c) is, however, a constant of the material. This quantity is called the *electron affinity*, and is conventionally denoted by *qX* in energy units. Tables of X in volts exist for many materials. (The symbol X is a Greek capital letter *chi.)*

Idealized Metal-Semiconductor Junction

Band Diagram

- Φ_M is less than Φ_S and the materials do not interact

  an electron in the metal has, on average, a total energy that is higher than the average total energy of an electron in the semiconductor

- Φ_M is greater than Φ_S and the materials do not interact

  the average total energy of an electron in the semiconductor is higher than it is in the metal

Consider the latter case where $\Phi_M > \Phi_S$

→ When an intimate contact is established, the <u>disparity in the average energies</u> can be expected to cause the transfer of electrons from the <u>semiconductor into the metal</u>.

Idealized Metal-Semiconductor Junction

Band Diagram

Looking at the establishment of equilibrium for this case where $\Phi_M > \Phi_S$

$$f_{D1}g_1g_2 = f_{D2}g_2g_1 \qquad \text{(Eq. 3.1.5)}$$

The left-hand side of Equation 3.1.5 in that section is proportional to the flow of electrons from state system 1 to state-system 2
while the right-hand side of the same equation is proportional to the inverse flow.

The net flow is easily seen to be in the direction 2 to 1
if $f_{D2} > f_{D1}$ or, therefore, if $E_{f2} > E_{f1}$.

➡ The charge transfer continues until equilibrium is obtained, and a single Fermi level characterizes both the metal and the semiconductor.
At equilibrium, the semiconductor, having lost electrons, is charged positively with respect to the metal

Idealized Metal-Semiconductor Junction

Band Diagram

How to draw proper band diagram?

1. the vacuum level E_o must be drawn as a continuous curve

   E_o represents the energy of a "justfree“ electron and thus must be a continuous, single-valued function in space

2. Electron affinity is a property associated with the crystal lattice like the forbidden-gap energy. Hence, it is a constant in a given material

3. Considering these three factors: constancy of E_f , continuity of E_o, and constancy of X in the semiconductor

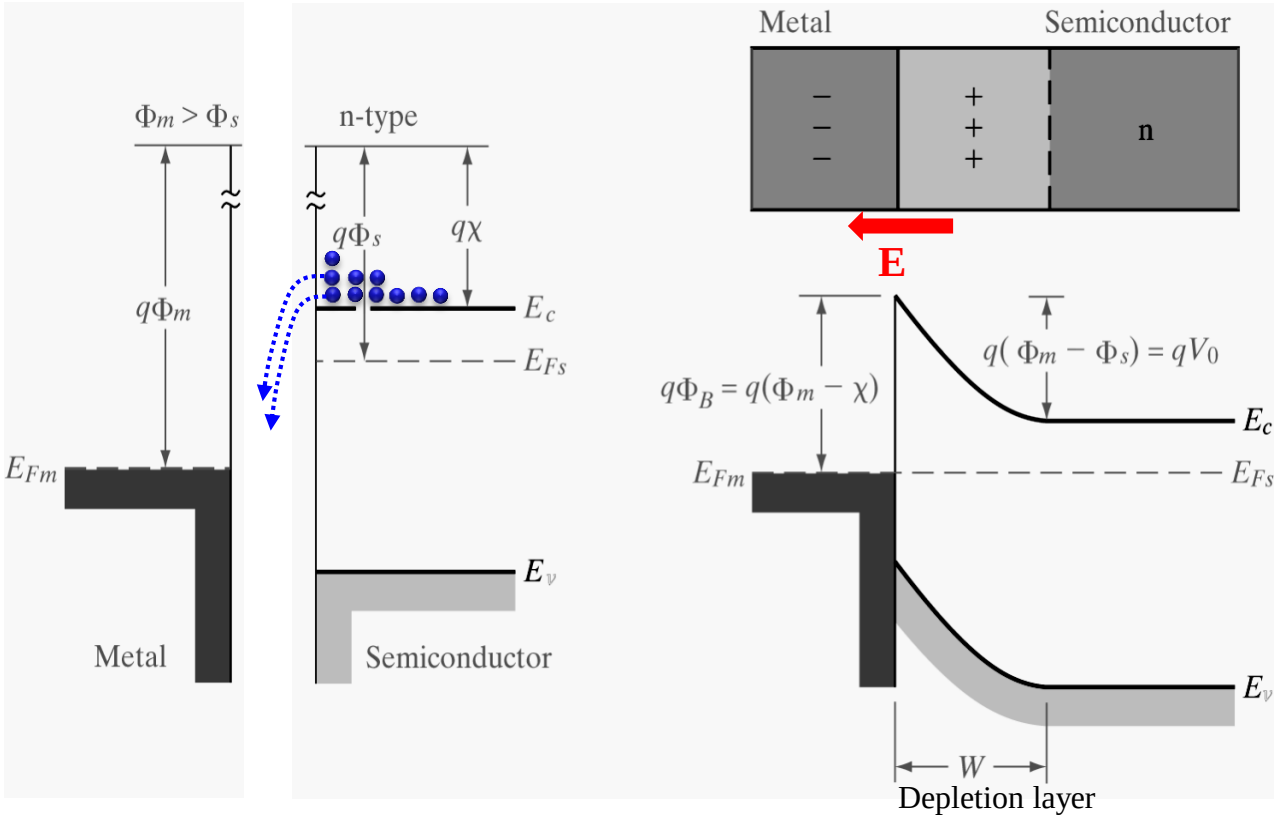
   we can sketch the general shape of the band diagram for the metal semiconductor system

Idealized Metal-Semiconductor Junction

Charge, Depletion Region and Capacitance

***n*-type semiconductor–metal** $\Phi_M > \Phi_S$ Schottky contact

Before contact **After contact**



- **Schottky barrier height**

$$\Phi_B = \Phi_M - \chi$$

: Potential barrier for e' moving fr metal to s.c.

- **Contact potential**

$$V_0 = \Phi_M - \Phi_s$$

: Potential barrier for e' moving fr s.c. to metal

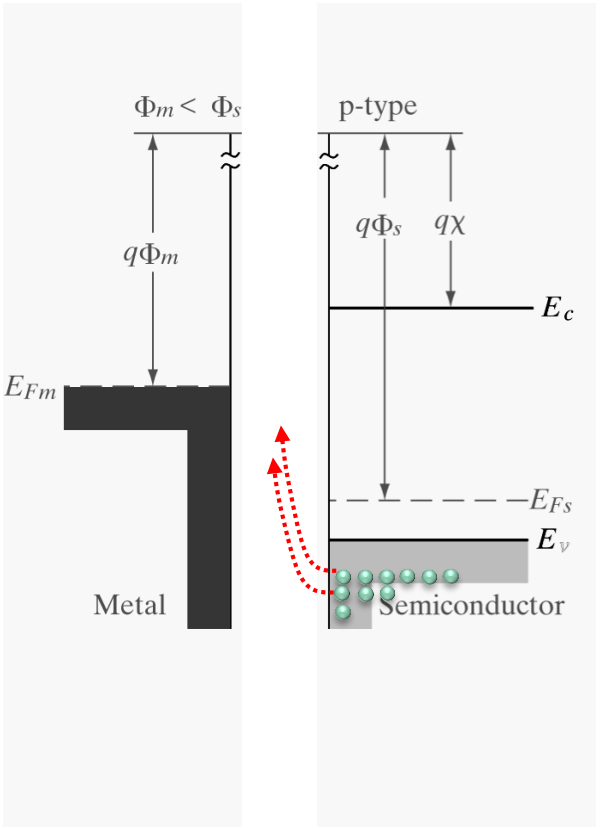
Electron transfer from semiconductor to metal until the Fermi levels align at equilibrium
⇒ positive charge of donor ion in depletion region = the negative charge on metal
⇒ contact potential (V_o) prevent electron flow from semiconductor to metal

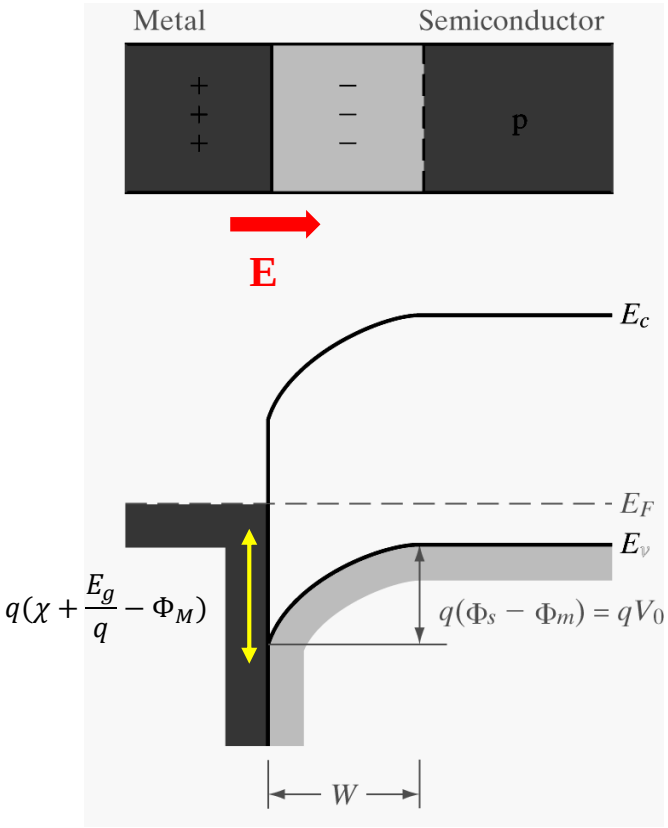
Idealized Metal-Semiconductor Junction

Charge, Depletion Region and Capacitance

***p*-type semiconductor–metal** $\Phi_M < \Phi_S$ Schottky contact

Before contact **After contact**





- **Schottky barrier height**

$$\Phi_B = \chi + \frac{E_g}{q} - \Phi_M$$

: Potential barrier for h' moving from metal to s.c.

- **Contact potential**

$$V_o = \Phi_s - \Phi_M$$

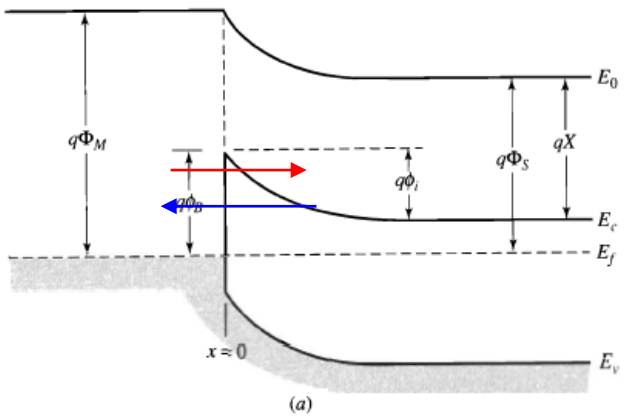
: Potential barrier for h' moving from s.c. to metal

Hole transfer from s.c. to metal until the Fermi levels align at equilibrium
⇒ negative charge of acceptor ion in depletion region = the positive charge on metal
⇒ contact potential (V_o) prevent hole flow from s.c. to metal

Idealized Metal-Semiconductor Junction

Applied Bias

- Nonequilibrium condition (at applied voltage)



At equilibrium condition

Abrupt step in allowed electron energies
at the metal-semiconductor interface

This step makes it more difficult to cause a net transfer of free electrons from the metal into the semiconductor than it is to obtain a net flow of electrons in the opposite direction

There is a barrier of $q\Phi_B$ electron volts between electrons at the Fermi level in the metal and the conduction band states in the semiconductor near its surface

→ The barrier height is independent of bias

Idealized Metal-Semiconductor Junction

Applied Bias

- Nonequilibrium condition (at applied voltage)

  An applied voltage is similarly dropped entirely within the semiconductor and alters the equilibrium-band diagram by changing the total curvature of the bands, modifying the potential drop from Φ_i

  → Electrons in the bulk of the semiconductor at the conduction-band edge are interrupted from transferring to the metal by a barrier that can be changed readily from its equilibrium value Φ_i by an applied bias.

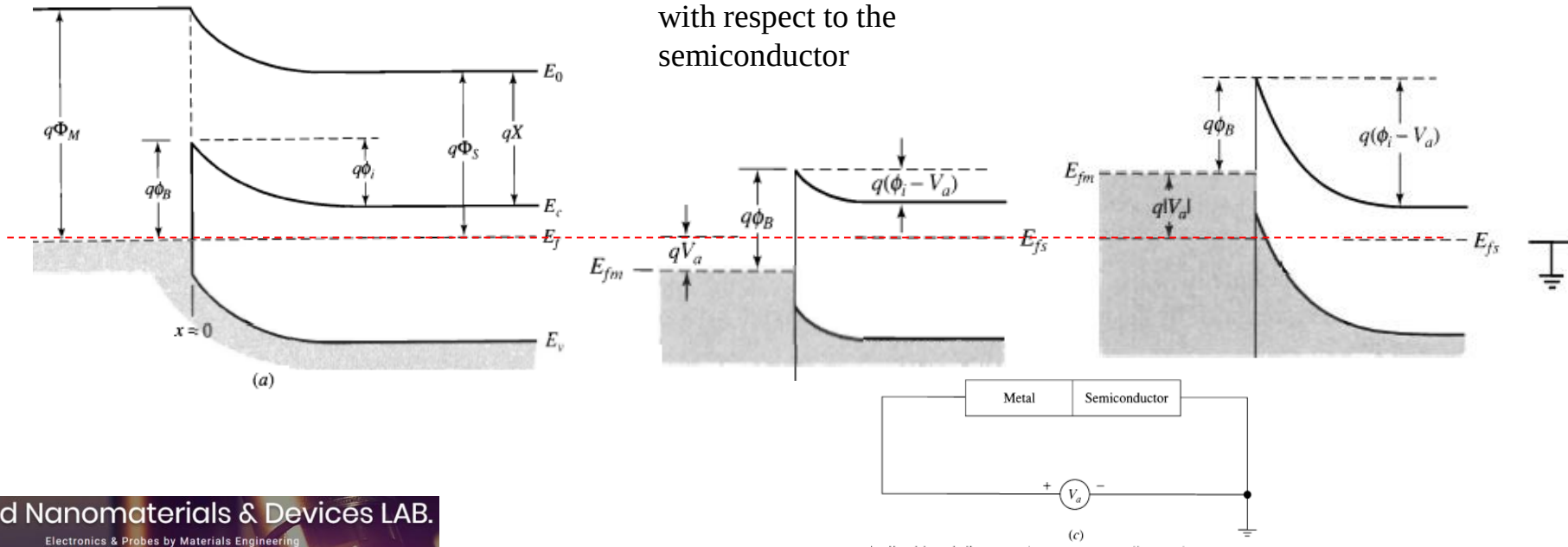
At equilibrium condition $(V_a = 0)$

Under positive Bias $(V_a > 0)$

The barrier is reduced when the metal is biased positively with respect to the semiconductor

Under negative Bias $(V_a < 0)$

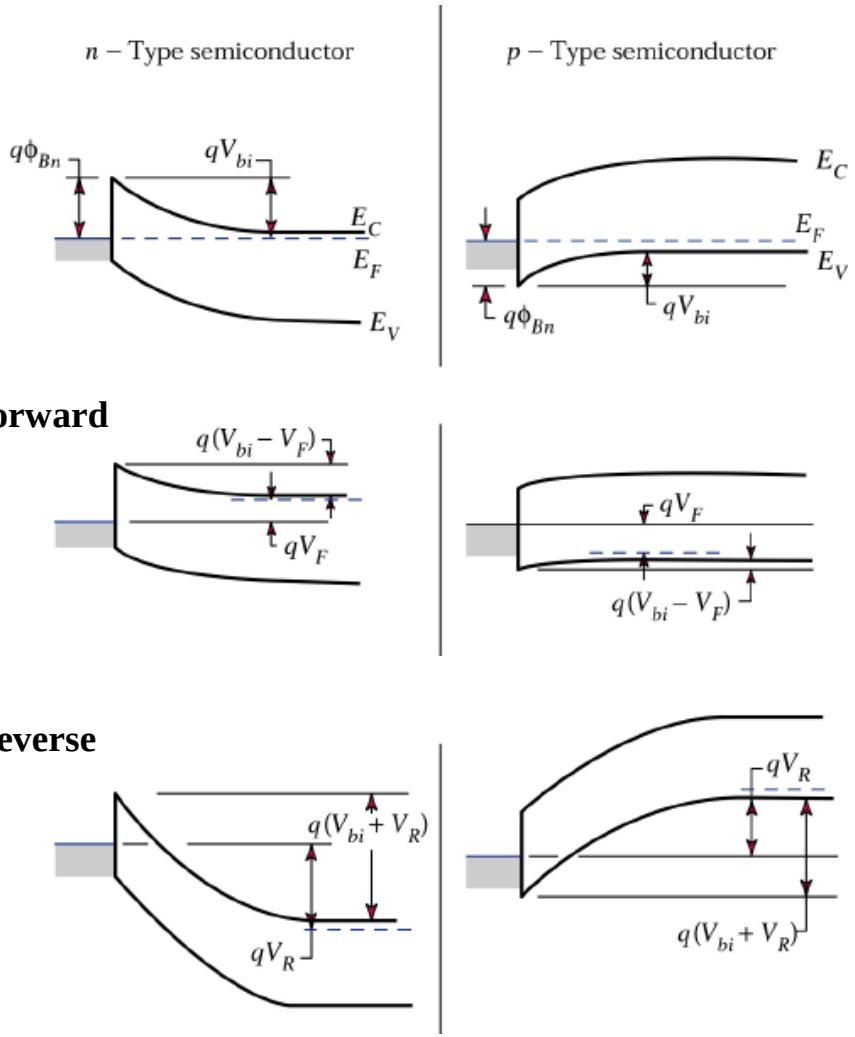
The barrier is increased when the metal is more negative.



Idealized Metal-Semiconductor Junction

Schottky contact

Rectifying contact under bias



- **Forward bias**

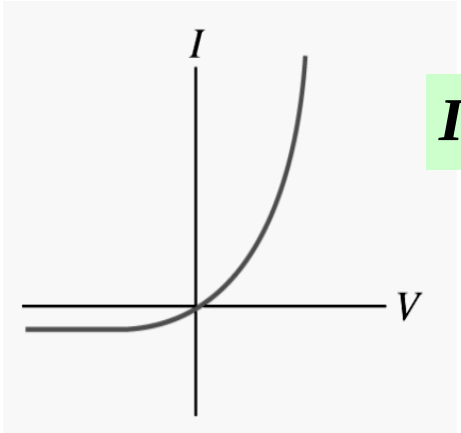
  Barrier reduce : V_o → V_o-V_F

  ⇒ Enhance *e* diffusion from s.c. to metal

- **Reverse bias**

  Barrier increase : V_o → V_o+V_r

  ⇒ Reduce *e* diffusion from s.c. to metal



$$I = I_0\left(e^{qV/kT} - 1\right)$$

$$I_0 \propto e^{-q\Phi_B/kT}$$

Φ_B : Schottky barrier height

- **Schottky diode**

  ⇒ short delay time

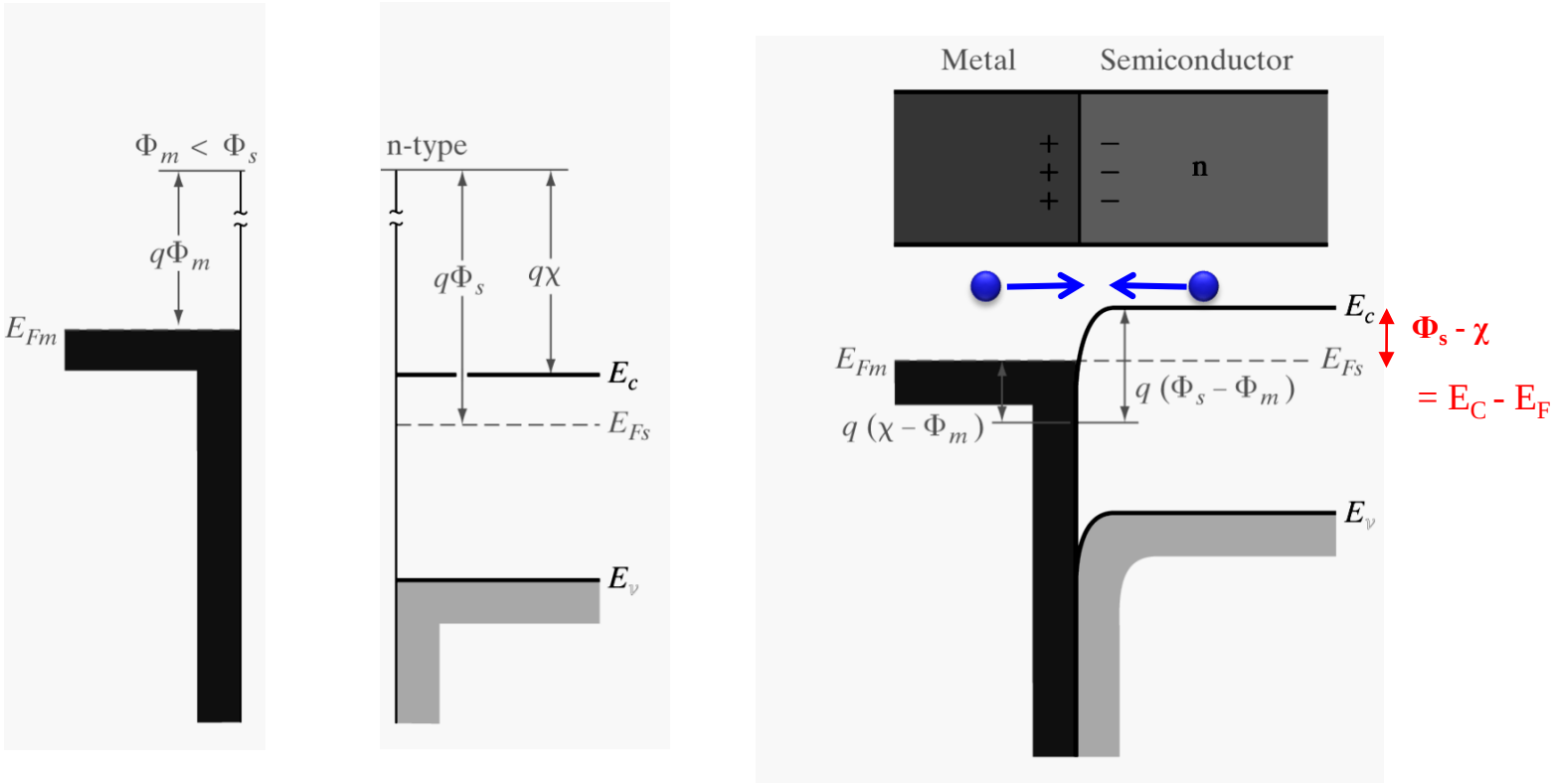
  ⇒ high-speed rectifier

Idealized Metal-Semiconductor Junction

Ohmic contact

***n*-type semiconductor–metal** $(\Phi_M < \Phi_s)$

Before contact **After contact**



Electron transfer from metal to s.c. until the Fermi levels align at equilibrium

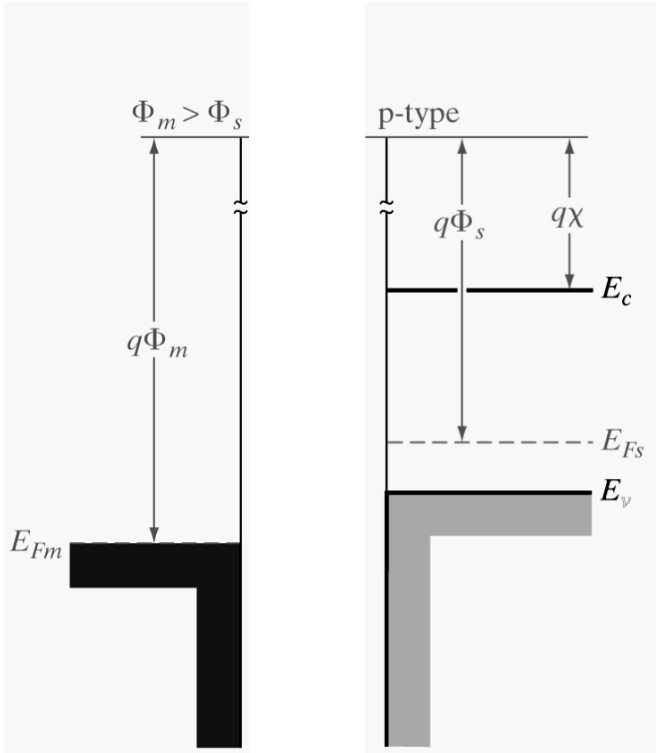
⇒ energy barrier to electron flow between metal and s.c. is much small and easily overcome by small voltage

Idealized Metal-Semiconductor Junction

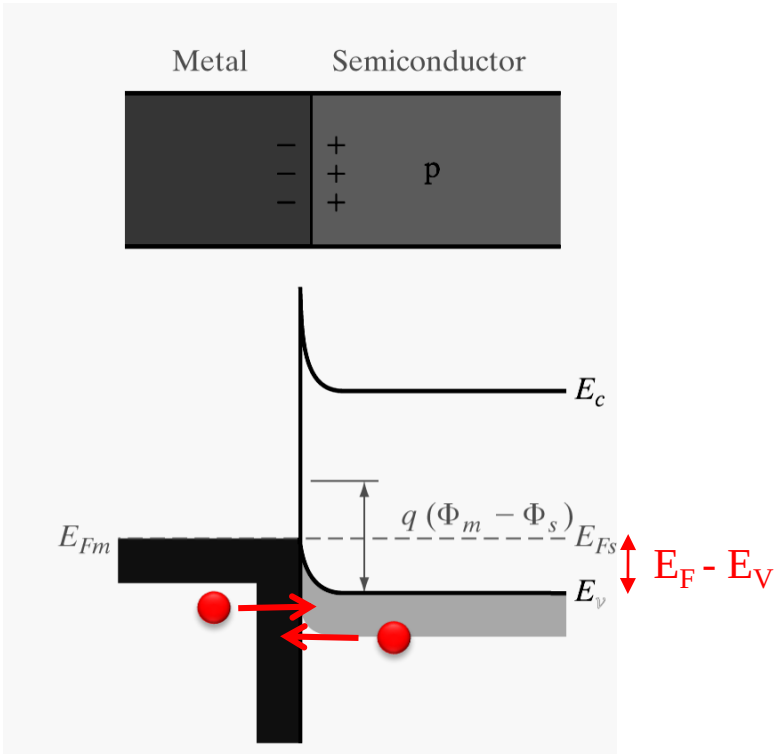
Ohmic contact

***p*-type semiconductor–metal** $(\Phi_M > \Phi_s)$

Before contact



After contact



hole transfer from metal to s.c. until the Fermi levels align at equilibrium

⇒ barrier to hole flow between metal and s.c. is much small and easily overcome by small voltage

Idealized Metal-Semiconductor Junction

Summary

	n-type	p-type
$\Phi_M > \Phi_S$	rectifying	ohmic
$\Phi_M < \Phi_S$	ohmic	rectifying

- Most of electronic devices need Ohmic junction for contact between different material, which causes minimal contact resistance
- Rectifying properties of diode need Schottky contact .

Idealized Metal-Semiconductor Junction

Summary

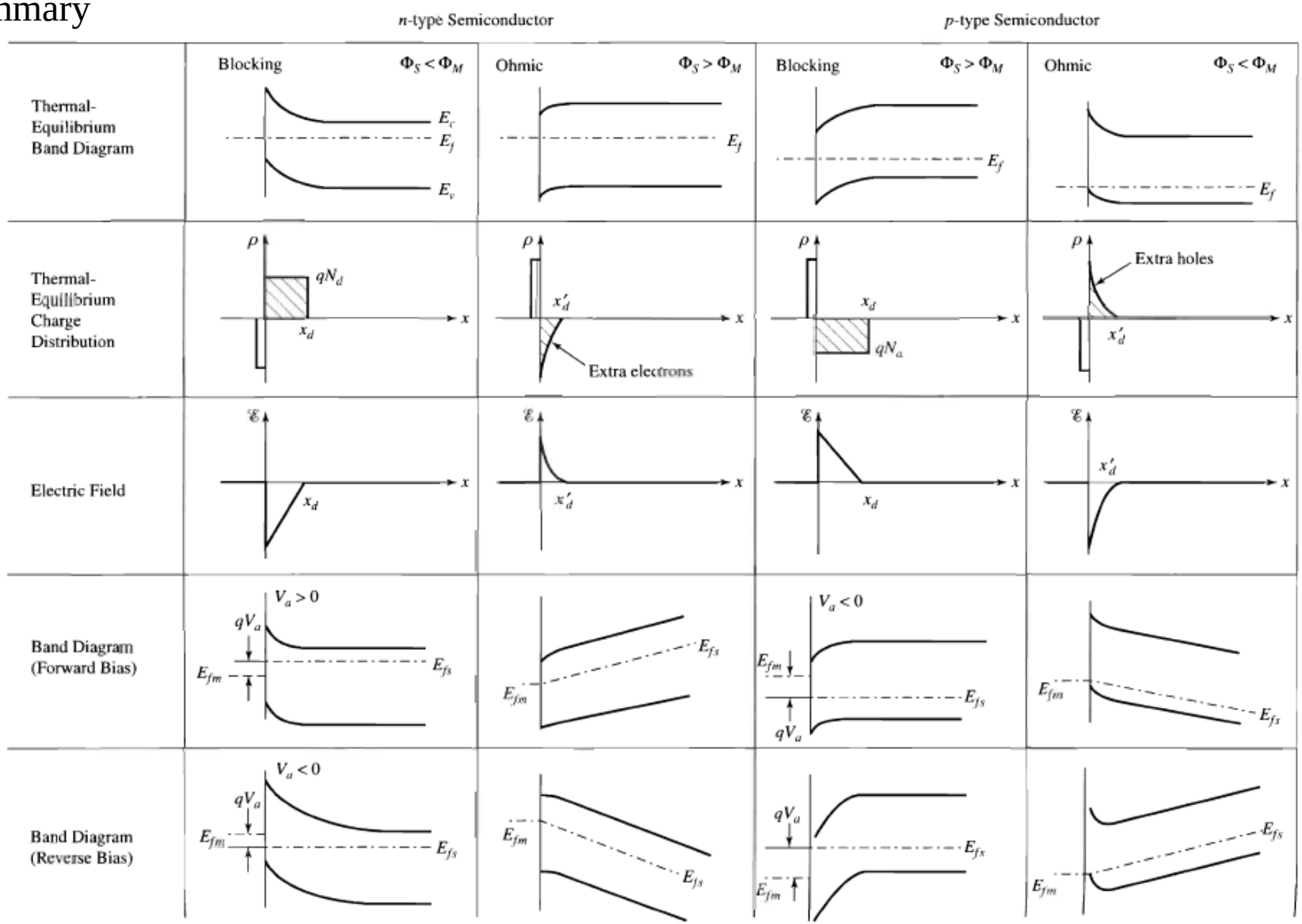
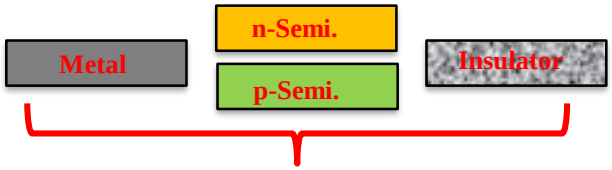


FIGURE 3.21 Diagrams for ideal metal-semiconductor Schottky diodes.

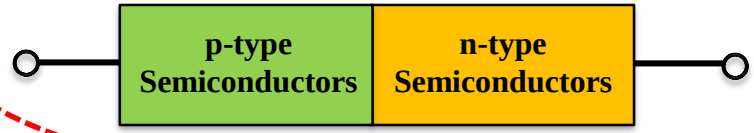
Chapter 4. p-n Junction

The pn junction

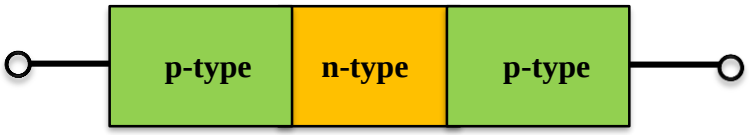
Device building block



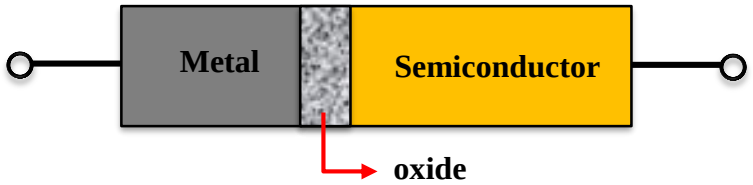
- Schottky Diode



- Diode
- Light-emitting diode
- Laser diode
- Photodiode
- Solar cell



- bipolar junction transistor



- MOS capacitor
- MOS field-effect transistor

The pn junction

To build a model for the *pn* junction

- Considering initially separated *n*- and p-type semiconductor crystals of the same material
- When these are brought into intimate contact as shown in Figure *4.3b*, the large difference in electron concentrations between the two materials causes electrons to flow from the n-type semiconductor into the *p-type* semiconductor and holes to flow from the p-type region into the n-type region.
- As these mobile carriers move into the oppositely doped material, they leave behind uncompensated dopant atoms near the junction, causing an electric field
- The field lines extend from the donor ions on the n-type side of the junction to the acceptor ions on the p-type side (Figure *4.3c).*
- This field creates a potential barrier between the two types of material.
- When equilibrium is reached, the magnitude of the field is such that the tendency of electrons to diffuse from the *n-type* region into the p-type region is exactly balanced by the tendency of electrons to drift in the opposite direction under the influence of the built-in field.

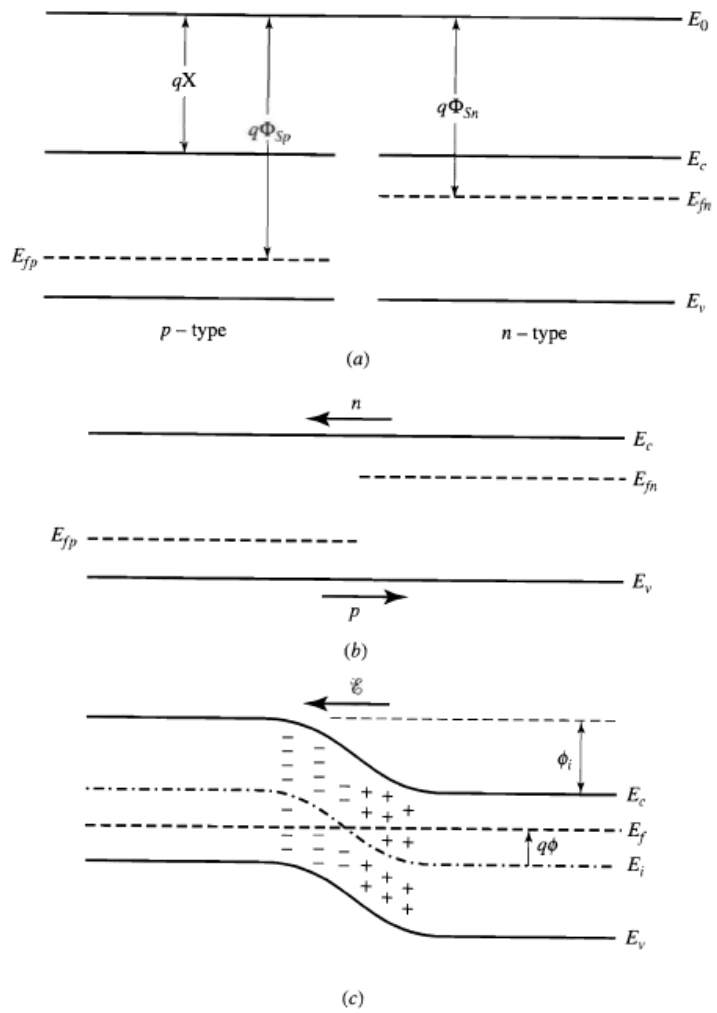
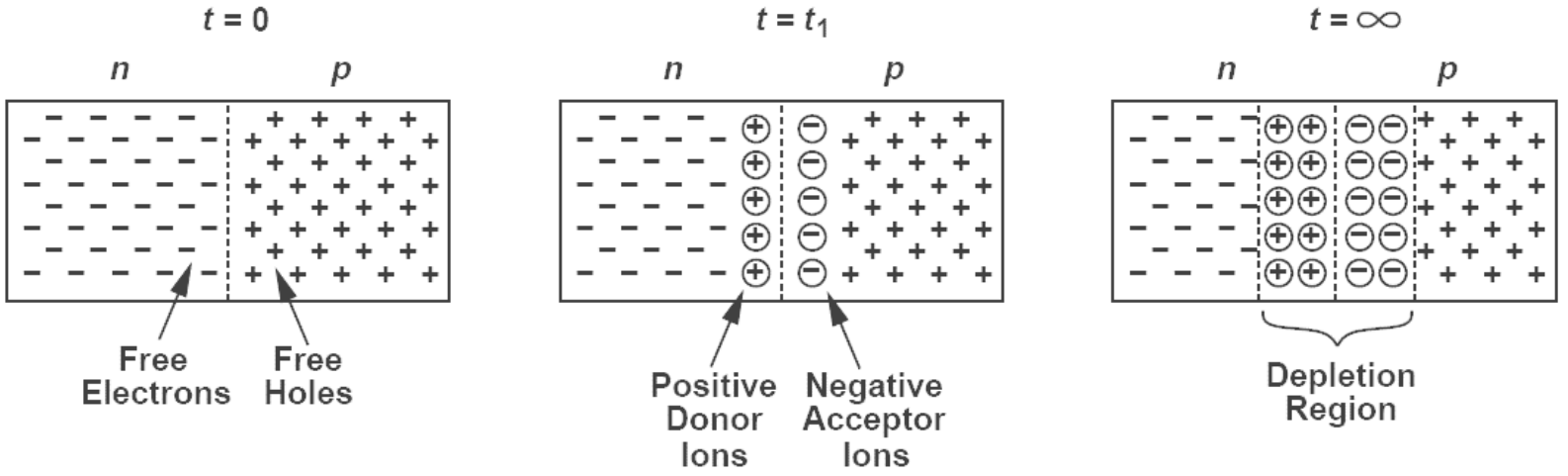


FIGURE 4.3 (*a*) *n*-type and *p*-type semiconductor regions separated and not in thermal equilibrium. (*b*) The two regions brought into intimate contact allowing diffusion of holes from the *p*-region and electrons from the *n*-region. (*c*) Transfer of free carriers leaves uncompensated dopant ions, which cause a field that opposes and balances the diffusion tendencies of holes and electrons.

The pn junction

Potential barrier



① PN junction이 생성되었다고 가정
② 전자와 정공의 농도 차이로 인해서 접합을 향해서 확산
③ 전자와 정공이 서로 만나 재결합(recombination)으로 사라짐.
④ 도펀트 이온만 노출되며 공핍영역에 전기장 형성
⑤ 도펀트 이온에 의한 전기장방향과 캐리어(전자 또는 정공)에 의한 확산 전류는 서로 반대
⑥ 확산 전류를 막아서 net current = 0이 될 때까지 전기장 증가
⑦ 확산과 드리프트 간 전류가 평형이 발생하며 그 때, built-in potential 결정

The pn junction

To build a model for the *pn* junction

- Considering initially separated *n*- and p-type semiconductor crystals of the same material
- When these are brought into intimate contact as shown in Figure *4.3b*, the large difference in electron concentrations between the two materials causes electrons to flow from the n-type semiconductor into the *p-type* semiconductor and holes to flow from the p-type region into the n-type region.
- As these mobile carriers move into the oppositely doped material, they leave behind uncompensated dopant atoms near the junction, causing an electric field
- The field lines extend from the donor ions on the n-type side of the junction to the acceptor ions on the p-type side (Figure *4.3c).*
- This field creates a potential barrier between the two types of material.
- When equilibrium is reached, the magnitude of the field is such that the tendency of electrons to diffuse from the *n-type* region into the p-type region is exactly balanced by the tendency of electrons to drift in the opposite direction under the influence of the built-in field.

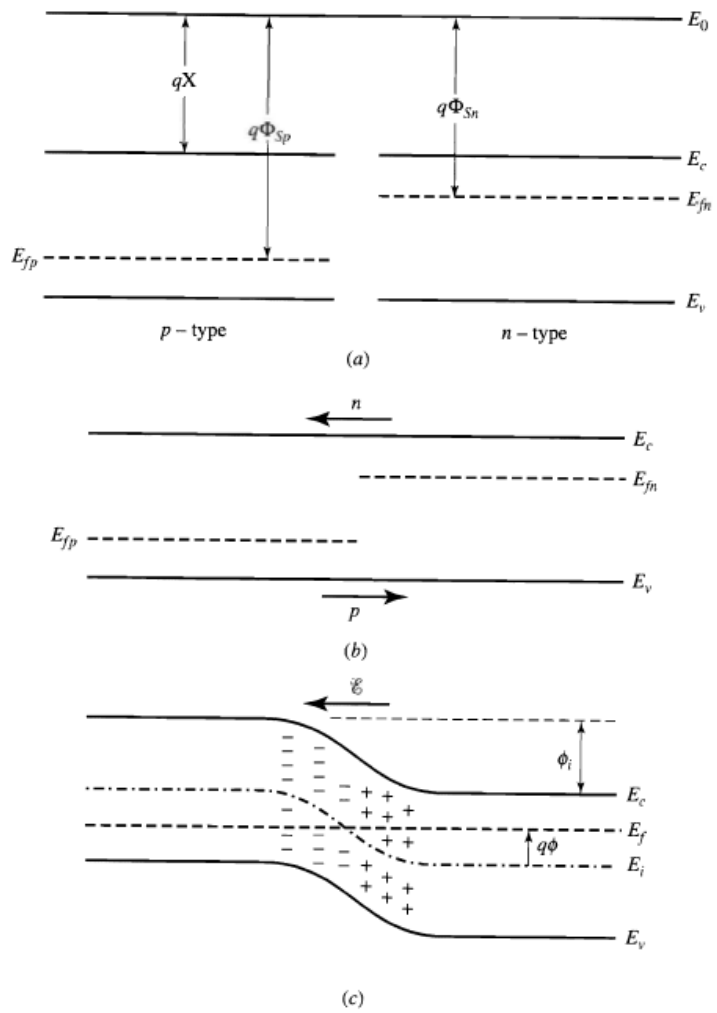
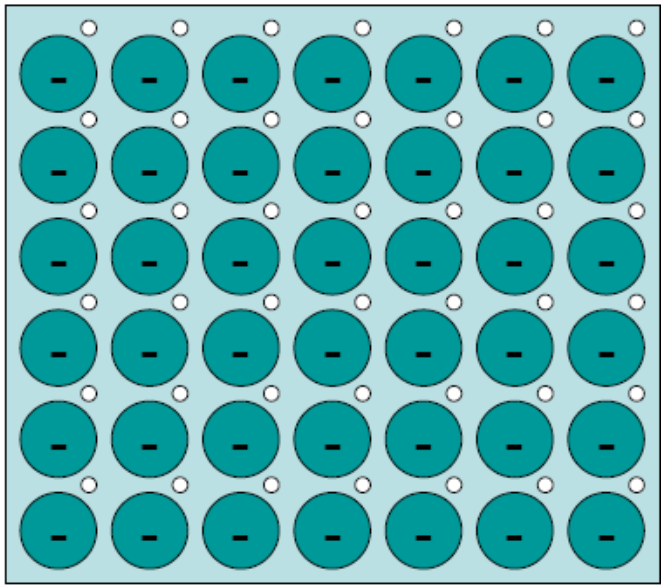


FIGURE 4.3 (*a*) *n*-type and *p*-type semiconductor regions separated and not in thermal equilibrium. (*b*) The two regions brought into intimate contact allowing diffusion of holes from the *p*-region and electrons from the *n*-region. (*c*) Transfer of free carriers leaves uncompensated dopant ions, which cause a field that opposes and balances the diffusion tendencies of holes and electrons.

The pn junction

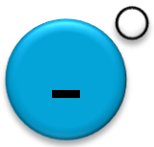
Junction formation

P-type semiconductor

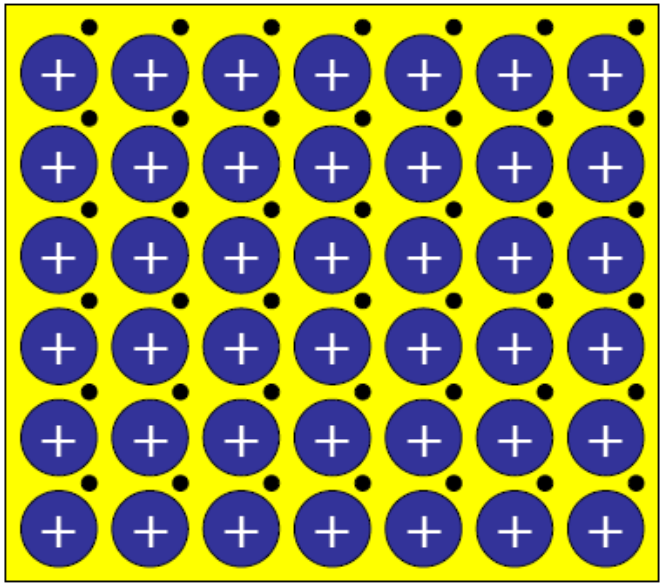


Semiconductor lattice with acceptor ions and free holes

Acceptor



N-type semiconductor

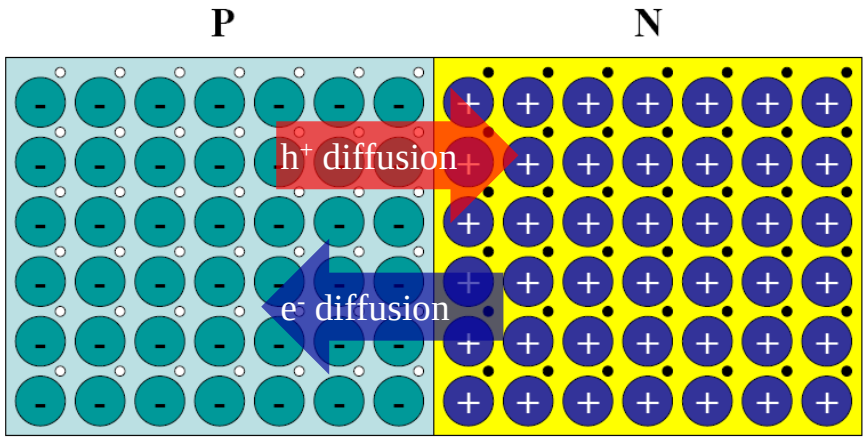


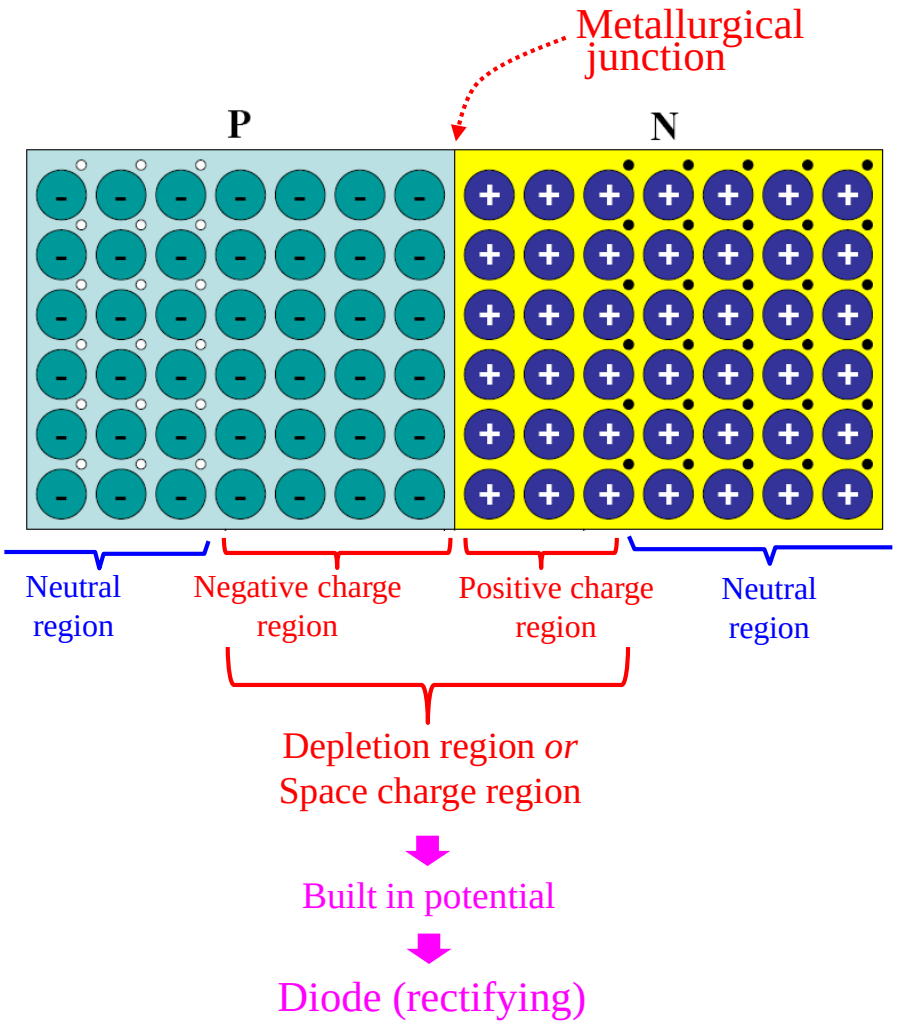
Semiconductor lattice with donor ions and free electrons

Donor

The pn junction

Junction formation : Depletion region

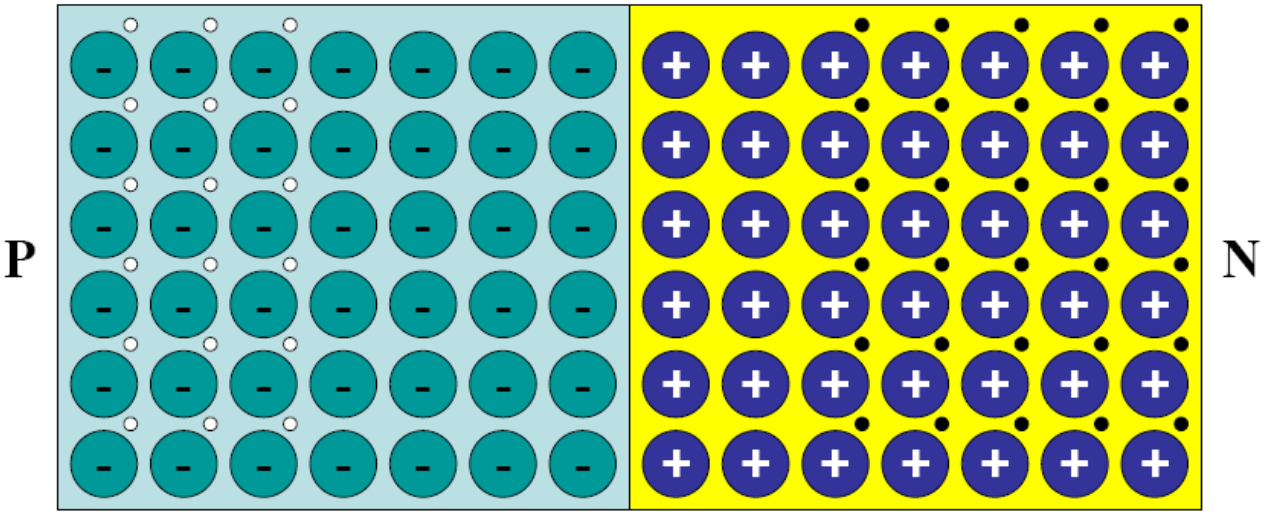


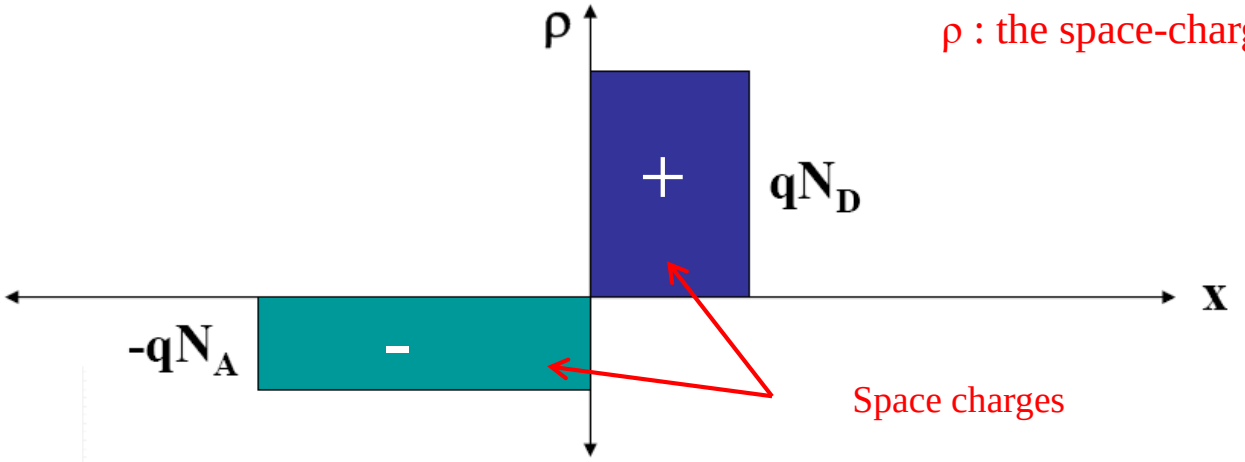


Depletion region : region where free carriers (e, h) are depleted

The pn junction

Junction formation : depletion region (space charge region)



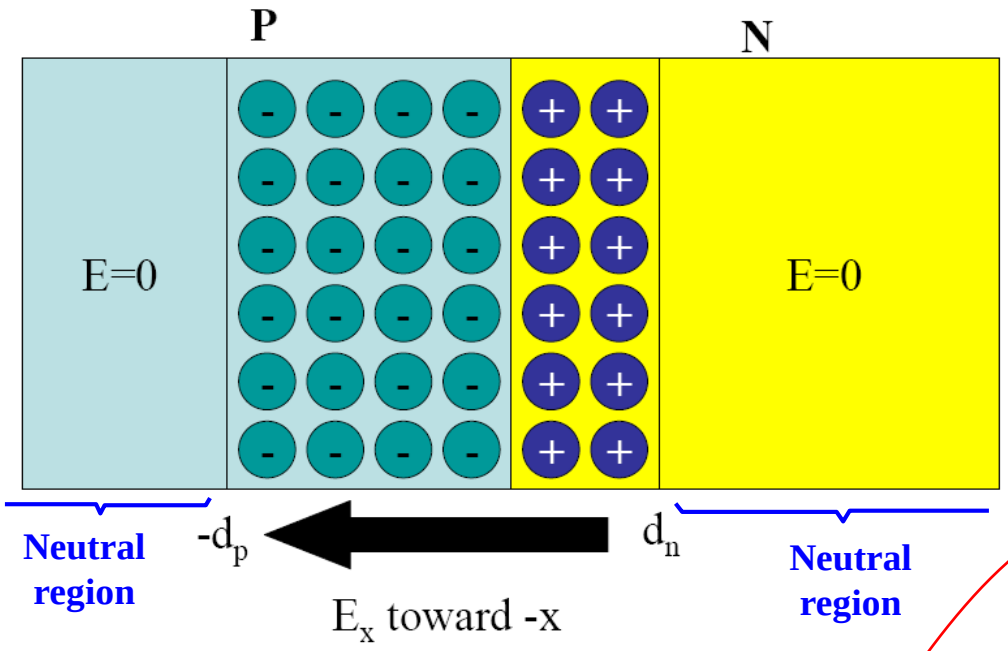


ρ : the space-charge density

When, $N_D \sim 2N_A$

The pn junction

Junction formation : electric field in the space charge region



$$-\frac{d\mathcal{E}}{dx}=-\frac{\rho_S}{\varepsilon_S}$$

$$\mathcal{E}=-\frac{d\Psi}{dx}$$

$$\frac{d^2\Psi}{dx^2}\equiv-\frac{d\mathcal{E}}{dx}=-\frac{\rho_S}{\varepsilon_S}$$

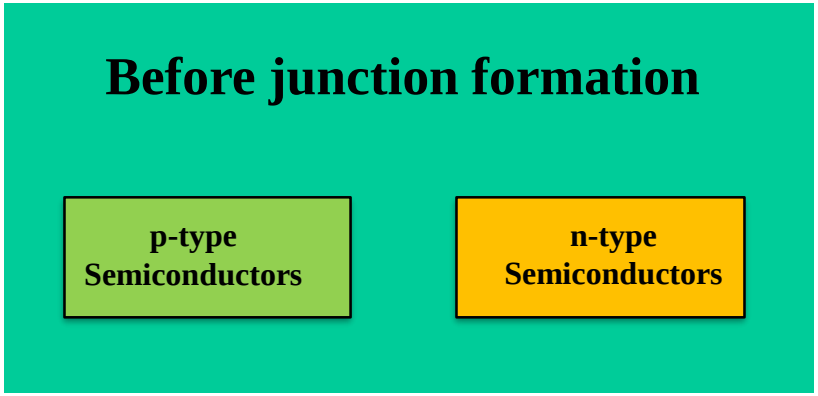
Poisson's equation

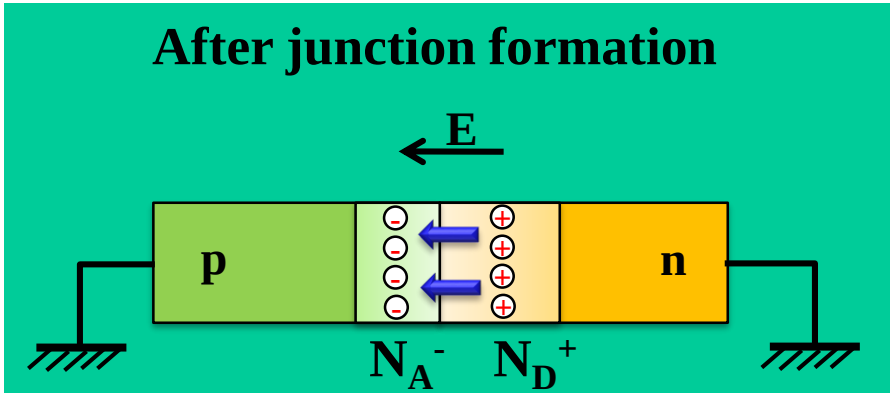
Junction formation

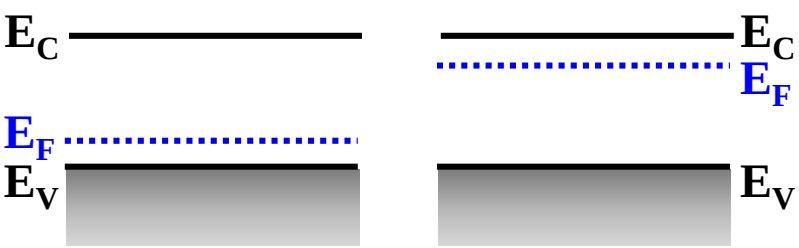
Dopant distribution → **Electrostatic potential distribution** → **Electric field distribution** → **Built-in potential Depletion width**

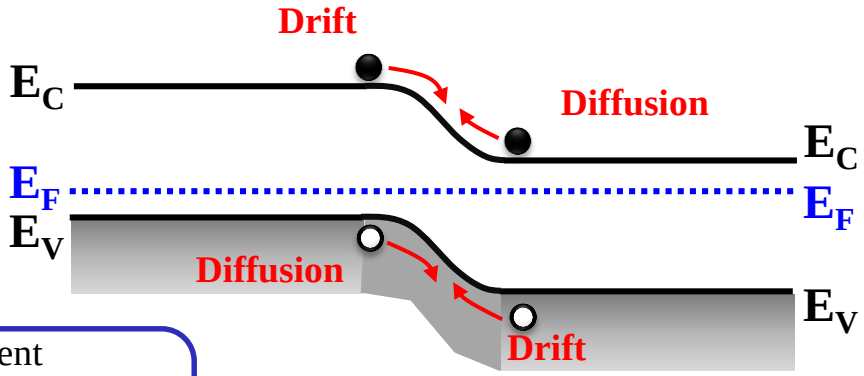
The pn junction

Junction formation (band diagram)









Diffusion of e^- & h^+ due to concentration gradient

↓

Formation of space charge region due to ionized dopants

↓

Electric field (E) induced from *n*- to *p*-side

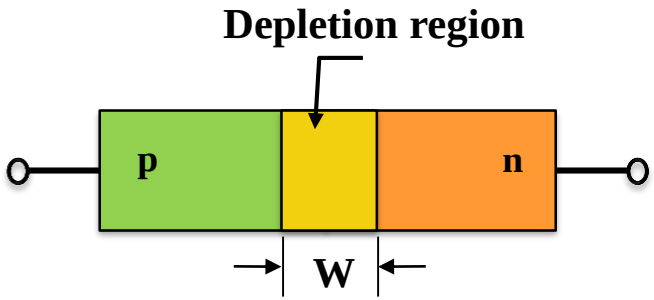
↓

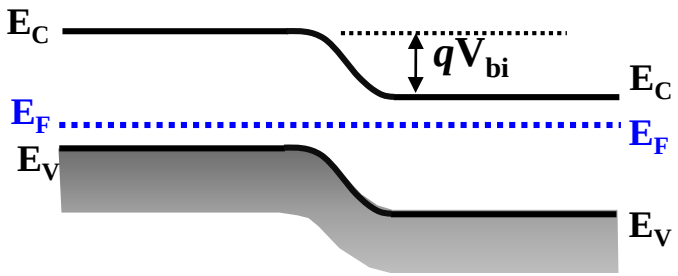
Drift current of of e^- & h^+

Chapter 5. Currents p-n Junctions

Junctions under applied bias (voltage)

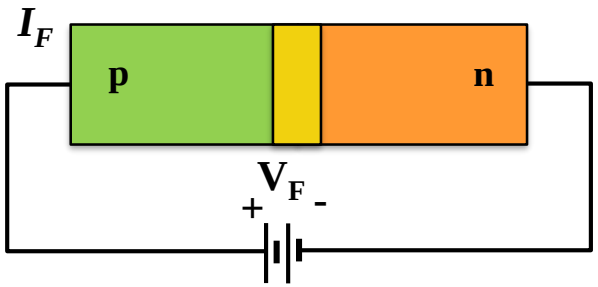
Thermal equilibrium

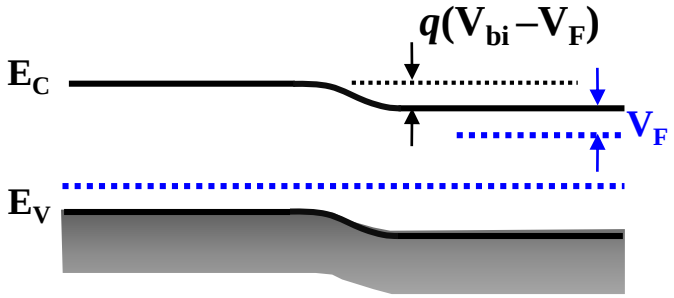




Balance between drift and diffusion currents

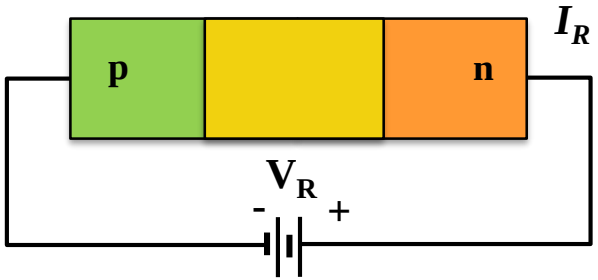
Forward bias

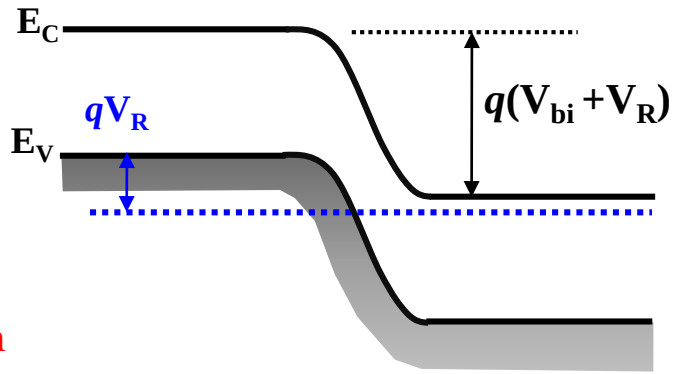




Reduce electrostatic potential difference → Enhance diffusion

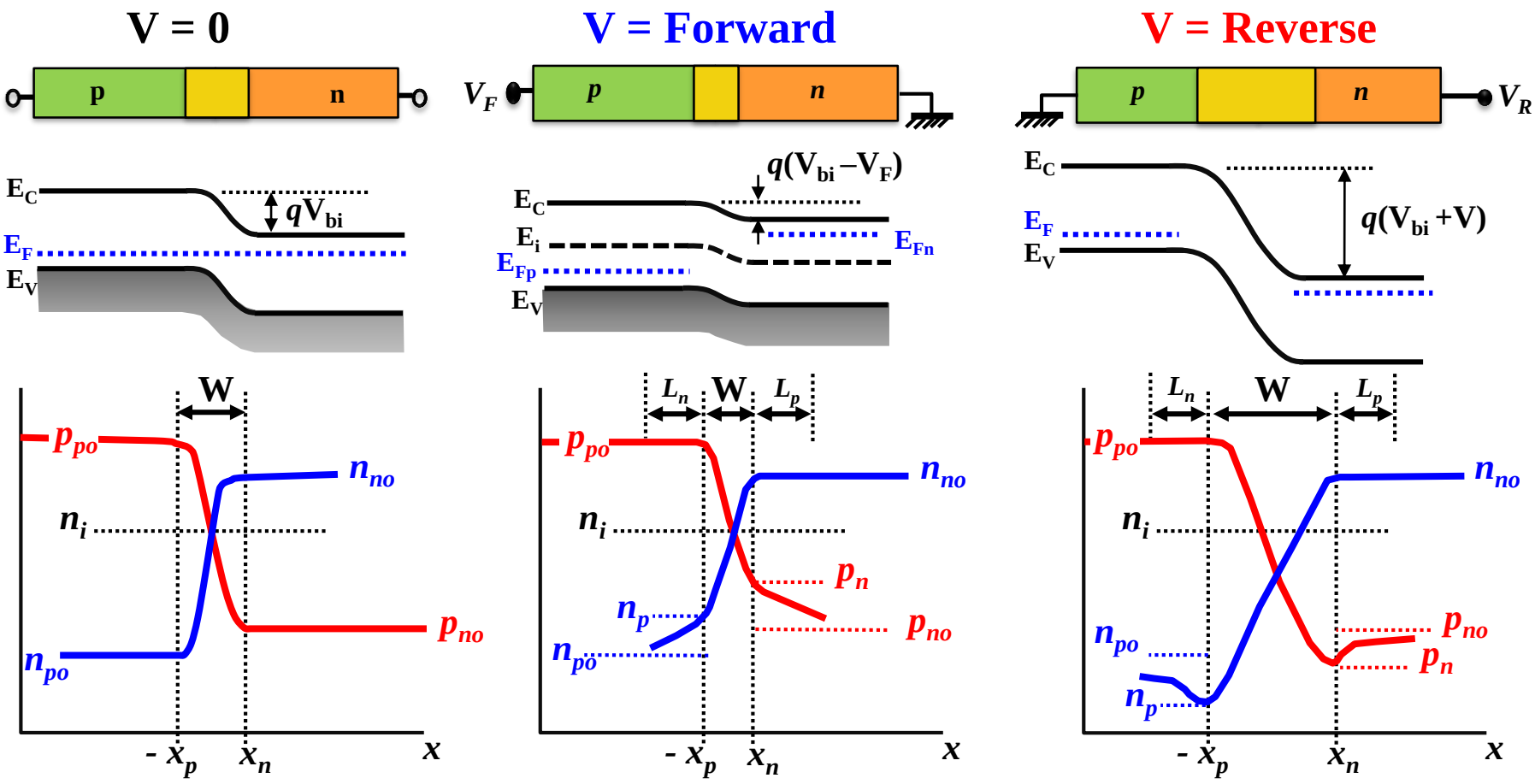
Reverse bias





Increase electrostatic potential difference → Reduce diffusion

Carrier distribution of p-n junction in ideal case



$$n_{no} = n_{po}\exp\left(\frac{qV_{bi}}{kT}\right)$$

$$p_{po} = p_{no}\exp\left(\frac{qV_{bi}}{kT}\right)$$

$$n_p = n_{po}e^{\frac{qV}{kT}}$$

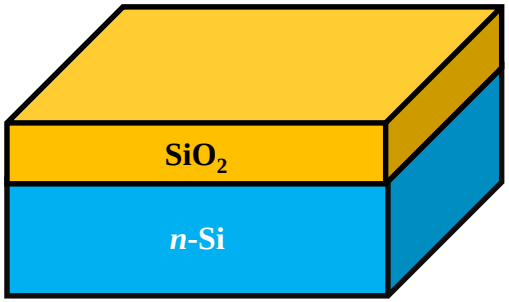
$$p_n = p_{no}e^{\frac{qV}{kT}}$$

$$n_p = n_{po}e^{-\frac{qV}{kT}}$$

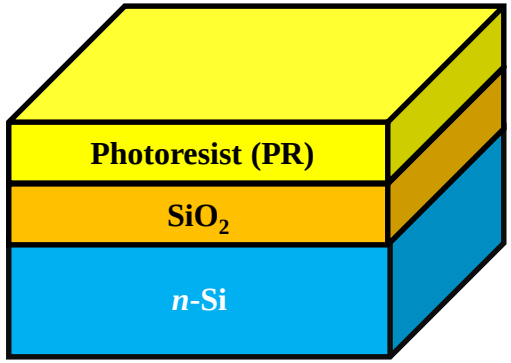
$$p_n = p_{no}e^{-\frac{qV}{kT}}$$

Fabrication process of p-n junction

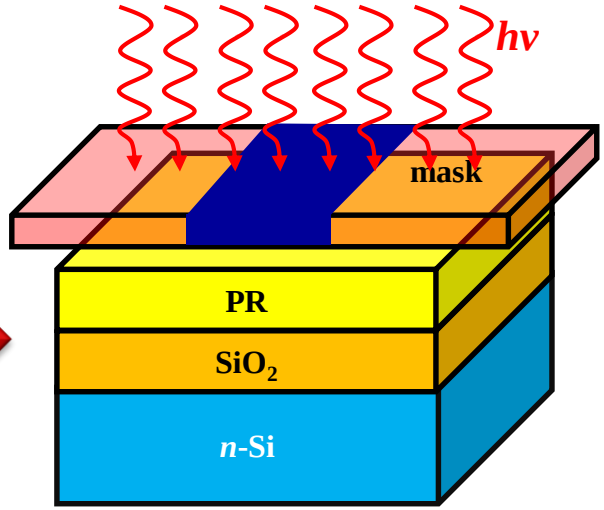
1) Wafer
2) Oxidation



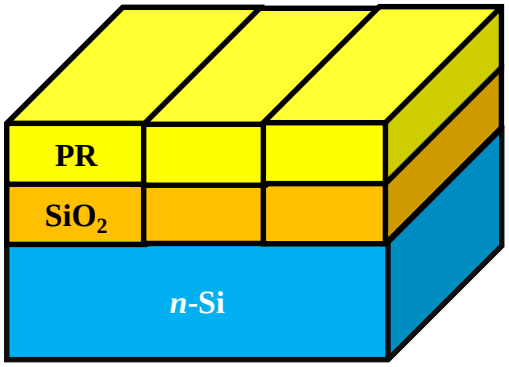
3) PR coating



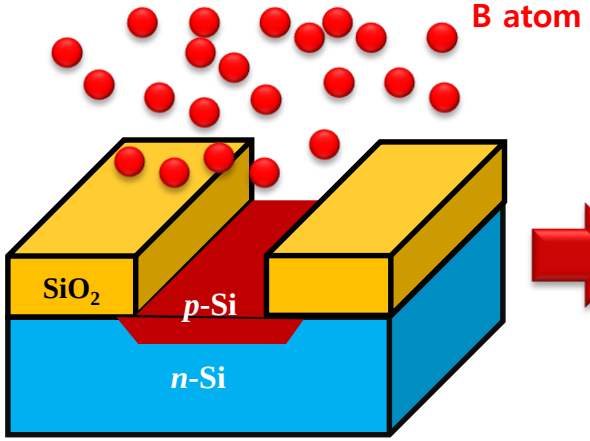
4) PR exposure



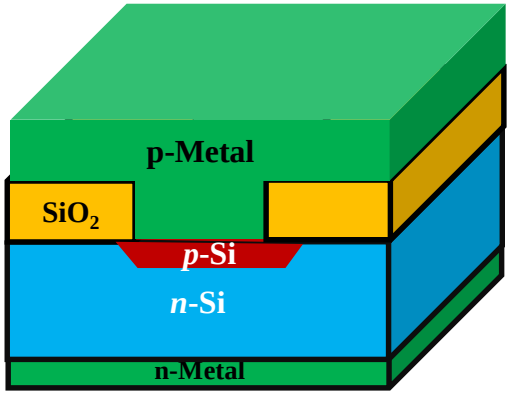
5) Development of PR
6) SiO_2 removal



7) Doping (Diffusion or ion implantation)



8) Metallization



Chapter 8. Properties of the metal-oxide-silicon system

The ideal MOS structure

Thermal-Equilibrium Energy-Band Diagram

The Fermi levels in the different materials are equalized by the transfer of negative charge from materials with higher Fermi levels (smaller work functions) across the interfaces to materials with lower Fermi levels (higher work functions).

*The vacuum level is a continuous function of position

When the materials are **separated**, the various energies are indicated on the Figure 8.1

Aluminum (work function = 4.1 V), silicon dioxide (electron affinity ~0.95 V), uniformly doped p-type silicon (electron affinity = 4.05 V) having a work function of 4.9 V are considered.
The vacuum level is designated E_o,

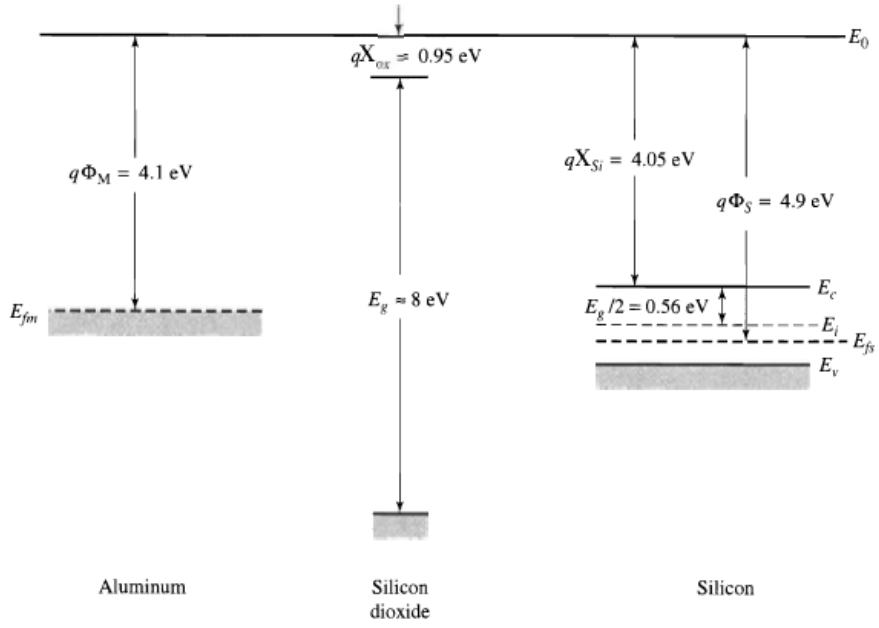


FIGURE 8.1 Energy levels in three separated materials that form an MOS system: aluminum, thermally grown silicon dioxide, and *p*-type silicon containing $N_a = 1.1 \times 10^{15}$ cm^{-3}. (Note that there is considerable variation in tabulated values for work functions and electron affinities. Commonly used values are indicated.)

The ideal MOS structure

Thermal-Equilibrium Energy-Band Diagram

As the materials are **brought together**,

Negative charge (electron) is transferred from the aluminum to the silicon to bring the system to equilibrium

because the work function of the metal is 0.8 eV less than the work function of the silicon

The insulator is incapable of transferring charge because it ideally possesses zero mobile charge, so a voltage drop appears across it because of the charge stored on either side.

There is a thin sheet of positive charge (a plane of charge in the ideal case of a perfect conductor) at the surface of the metal and negatively charged acceptors extending into the semiconductor from its

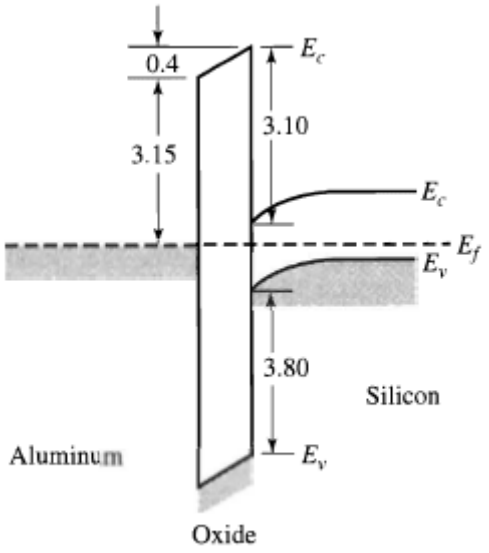


FIGURE 8.2 Energy-band diagram at thermal equilibrium for an ideal MOS system composed of the materials indicated in Figure 8.1. The oxide and Si–SiO_2 interface are assumed to be ideal and free of charges.

The ideal MOS structure

Thermal-Equilibrium Energy-Band Diagram

As the materials are **brought together**,

Negative charge (electron) is transferred from the aluminum to the silicon to bring the system to equilibrium

In fact, if the system being considered were fabricated without any path for charge flow between the metal and the silicon other than through an ideal oxide, the materials could exist in a condition of nonequilibrium (i.e., with unequal Fermi levels) for long periods

- However, nearly every MOS system of interest has some alternative path for the transfer of charge that is much more transmissive to charge flow than is the oxide; e.g., the aluminum gate electrode and the silicon substrate may be connected together, or an ohmic conducting path may exist between them.

- We assume that thermal equilibrium exists between the metal and the semiconductor. With these assumptions the band diagram for the MOS system formed with the materials

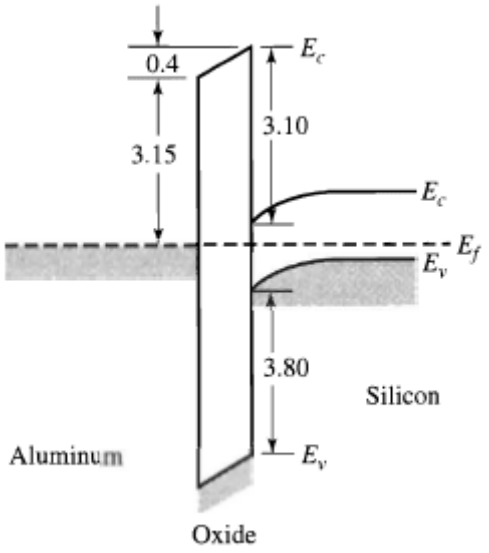


FIGURE 8.2 Energy-band diagram at thermal equilibrium for an ideal MOS system composed of the materials indicated in Figure 8.1. The oxide and Si–SiO_2 interface are assumed to be ideal and free of charges.

The ideal MOS structure

Polysilicon and Metals as Gate-electrode Materials

Because the surface condition of the silicon can be controlled by the metal electrode, the metal layer is usually called the *gate*, and the voltage on the metal is denoted by V_G.

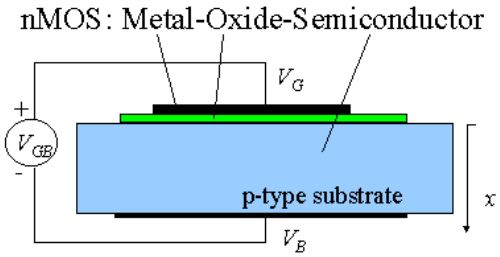
Because the silicon is deposited over amorphous silicon dioxide, it is a polycrystalline film typically consisting of sub-micrometer-size crystallites.
A very high concentration of either *n-type* or *p-type* dopant is subsequently introduced into the polysilicon to make it sufficiently conducting to behave electrically like a metal

- One major advantage of polysilicon is its ability to withstand high-temperature thermal treatments
- primary drawback is the high resistance of even heavily doped polysilicon compared to that of a metal

Attempts to find attractive metals to replace polysilicon as the gate electrode are continuing

The ideal MOS structure

The Flat-Band Voltage



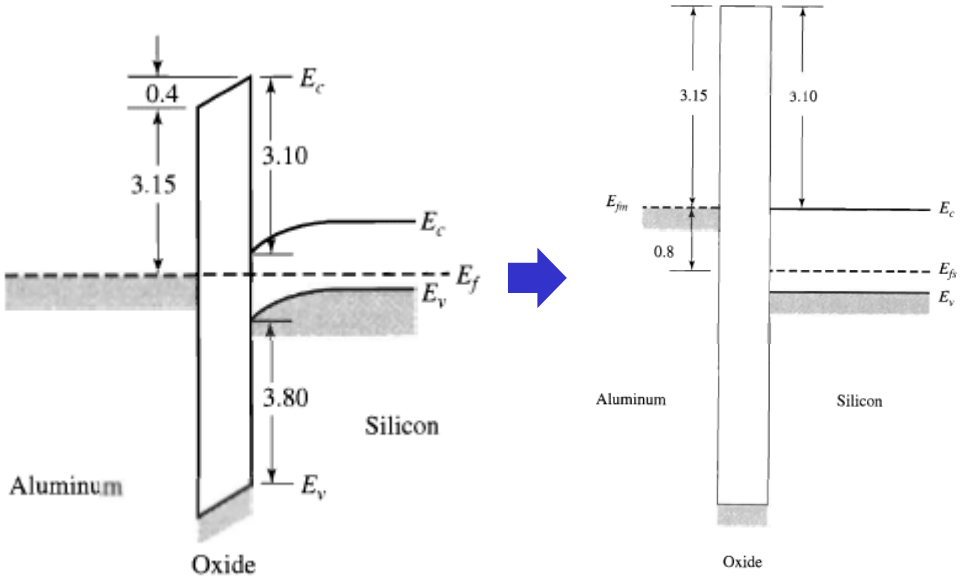
For the idealized MOS system at thermal equilibrium,
the metal and the semiconductor form two plates of a capacitor.

The capacitor is charged to a voltage corresponding to the difference between the metal and semiconductor work functions

- Applying a bias voltage between the metal and the silicon causes the system to depart from thermal equilibrium and changes the amount of charge stored on the capacitor.

Negative voltage applied to the metal with respect to the silicon opposes the built-in voltage on the capacitor and tends to reduce the charge stored on the capacitor plates below its equilibrium value.

- pulling positive holes toward the surface of the semiconductor to neutralize some of the negatively charged acceptors.



The ideal MOS structure

The Flat-Band Voltage

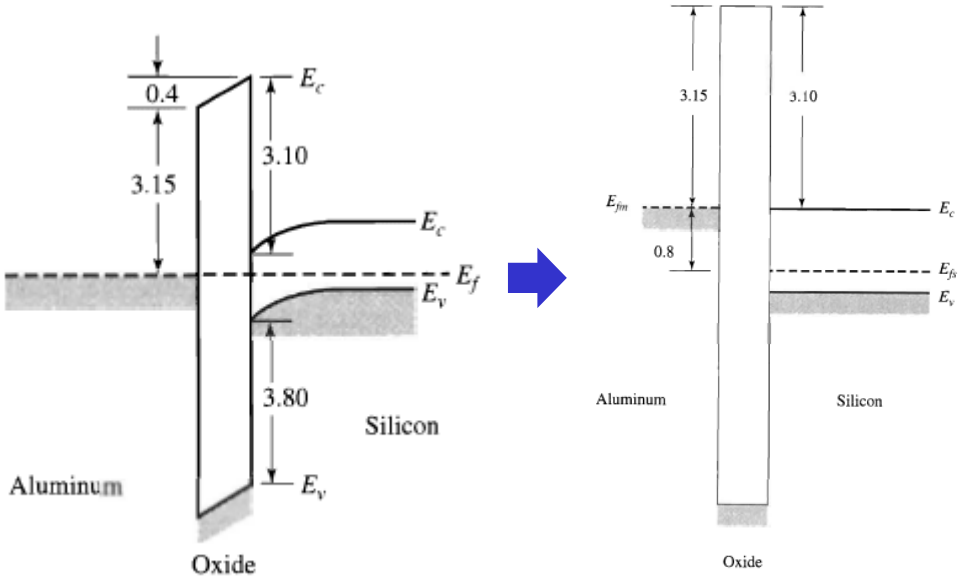
For the idealized MOS system at thermal equilibrium,
the metal and the semiconductor form two plates of a capacitor.

The capacitor is charged to a voltage corresponding to the difference between the metal and semiconductor work functions

- At one particular value, the applied voltage exactly compensates the difference in the work functions of the metal and the semiconductor.

The stored charge on the MOS capacitor is then reduced to zero, and the fields in the oxide and the semiconductor vanish

- The voltage that produces flat energy bands in the silicon is called the flat-band voltage and usually designated V_{FB}



The ideal MOS structure

The Flat-Band Voltage

For the idealized MOS system at thermal equilibrium,
the metal and the semiconductor form two plates of a capacitor.

The capacitor is charged to a voltage corresponding to the difference between the metal and semiconductor work functions

- The flat-band voltage varies with the dopant density in the silicon, as well as with the specific metal(work function) used for the MOS system

At the flat-band condition

→ MOS system is *not* at thermal equilibrium

The voltage applied to the ideal MOS system to bring it to the flat-band condition equals the difference in the work functions of the metal and the silicon.

$$V_{FB} = \Phi_M - \Phi_S = \Phi_{MS}$$

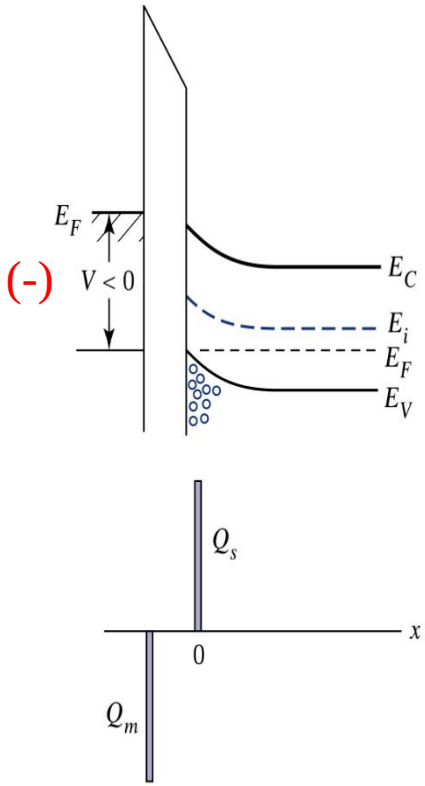
TABLE 8.1 Work Functions (Φ_M and Φ_S) and Flat-Band Voltages for Commonly Used Gate Materials and *p*-Type Silicon with $N_a = 1.1 \times 10^{15}$ cm^{-3}.

Gate material parameter	Aluminum	n^+ polysilicon	p^+ polysilicon	Tungsten
Φ_M (V)	4.1	4.05	5.17	4.61
Φ_S (V)	4.9	4.9	4.9	4.9
V_{FB} (V)	−0.8	−0.85	0.27	−0.29

Analysis of the ideal MOS structure

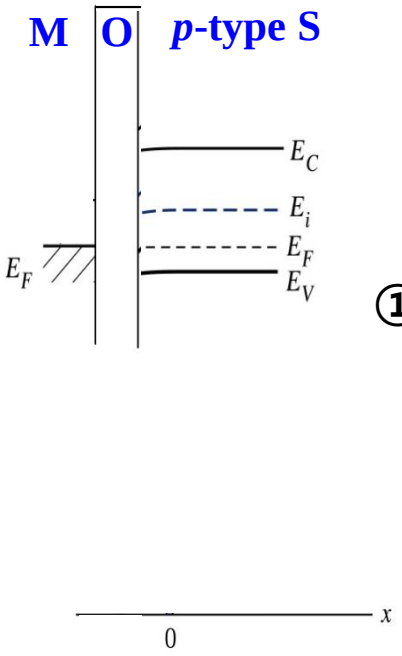
Qualitative Description (nMOS)

① Negative
(V_G - V_{FB} < 0)



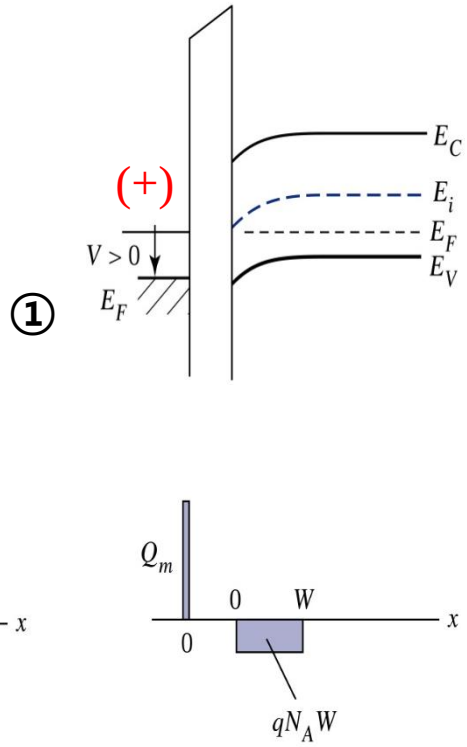
"Accumulation"

② No bias
(V_G - V_{FB} = 0)



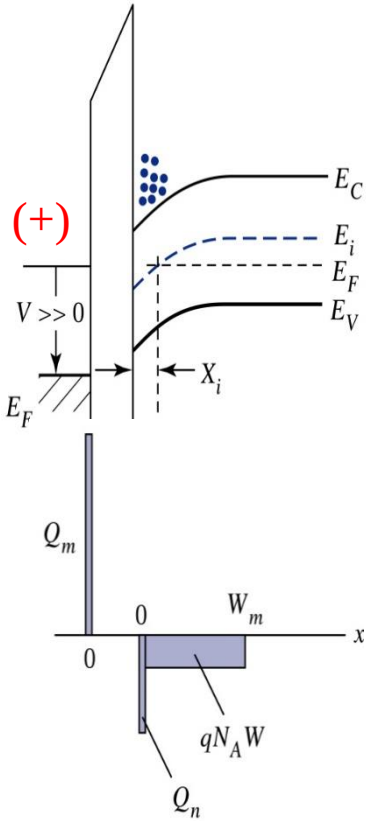
"Flat band"

③ Positive
(V_G - V_{FB} > 0)



"Depletion"

④ More Positive
(V_G - V_{FB} ≫ 0)



"Inversion"

Analysis of the ideal MOS structure

Qualitative Description (nMOS)

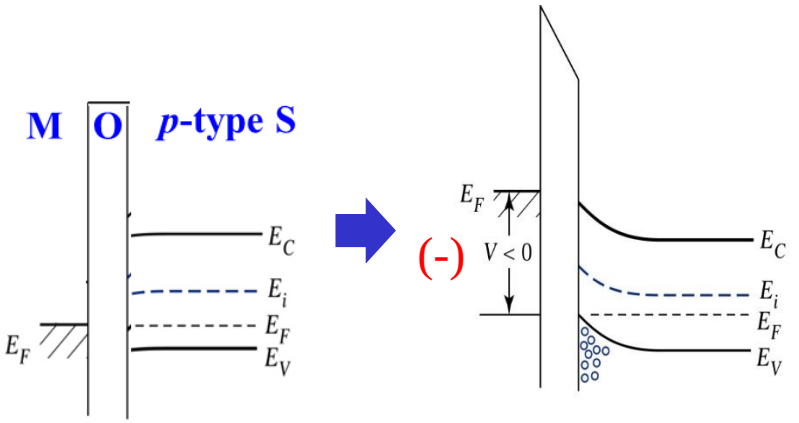
"Accumulation"

If the silicon is held at ground and the voltage applied to the metal is negative but increases in magnitude above V_{FB}

➡ Additional positively charged holes are attracted toward the silicon surface, and the MOS capacitor begins to store positive charge there.

This positive charge is made up of an increase in the hole population at the surface, so the surface has a greater density of holes than N_a the acceptor density

Flat band **① Negative (V_G - V_{FB} < 0)**



Negative voltage applied to the metal plate

⬇

Excess positive carriers (holes) induced at the interface

⬇

Energy bands bent upward

⬇

Increase of (E_i-E_F)

⬇

Enhanced hole concentration "Accumulation"

Analysis of the ideal MOS structure

Qualitative Description (nMOS)

"Depletion"

The applied voltage gives rise to negative charge in the semiconductor by repelling holes from the surface to create the depletion region

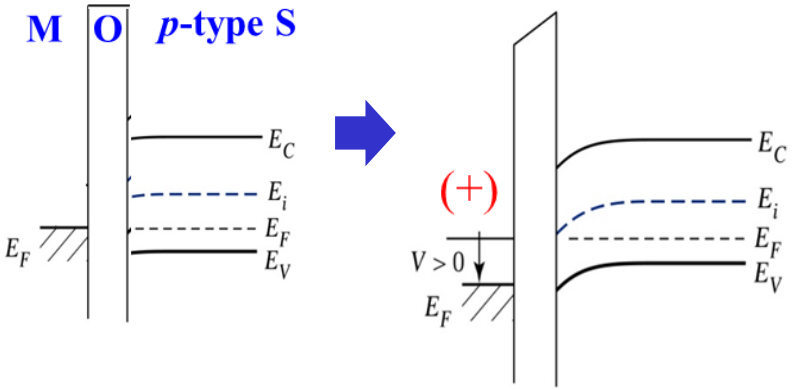
If this built-in voltage is aided by applying a positive gate voltage between the metal and the silicon

➡ The silicon becomes further depleted as more holes are repelled from its surface and more acceptors are exposed, the positive charge on the metal increases.

Because mobile silicon charge is withdrawn from the surface, this condition is called *surface depletion*

Flat band

③ Positive
(V_G - V_{FB} > 0)



Small positive voltage applied to the metal plate

⬇

Energy band near the interface bent downward

⬇

Decrease of (E_i-E_F)

⬇

The holes are depleted

⬇

"Depletion"

Analysis of the ideal MOS structure

Qualitative Description (nMOS)

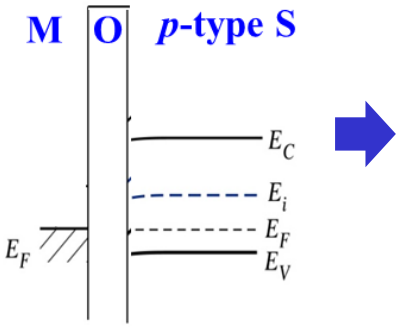
"Inversion"

The applied voltage gives rise to negative charge in the semiconductor by inducing electrons to form the inversion layer

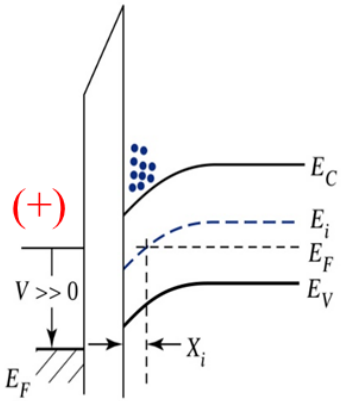
If the Fermi level remains constant in the silicon while the energy bands bend as the applied voltage changes, at sufficiently high voltages the intrinsic Fermi level E_i at the silicon surface crosses the Fermi level corresponding to the silicon bulk.

➡ the Fermi level is closer to the conduction- band edge than to the valence-band edge. In terms of carrier densities, this means that the applied voltage has created an *inversion layer*, so-called because the surface contains more electrons than holes, even though the silicon was doped with acceptor impurities.

Flat band



③ More Positive (V_G - V_{FB} >> 0)



Larger positive voltage applied to the metal plate

Energy band bent downward even more

$(E_i - E_F) < 0$

$$p_p = n_i e^{\frac{(E_i - E_F)}{kT}} < n_i$$

$$n_p = n_i e^{\frac{(E_F - E_i)}{kT}} > n_i$$

Minority carrier (n_p) is greater than majority carrier (p_p) at the interface (semiconductor surface)

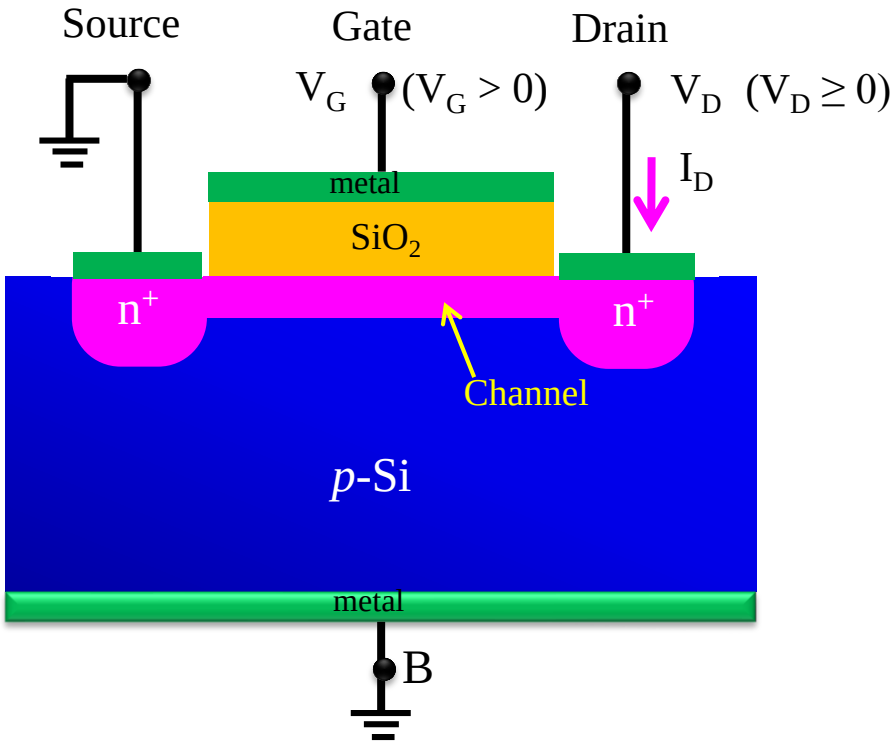
"Inversion"

Chapter 9. MOS Field-Effect Transistor

MOS Field-effect transistor

Operation of MOSFET (Gate voltage)

Flow of current (I_D) from "Source" to "Drain" is controlled by the "Gate" and "Drain" voltages.



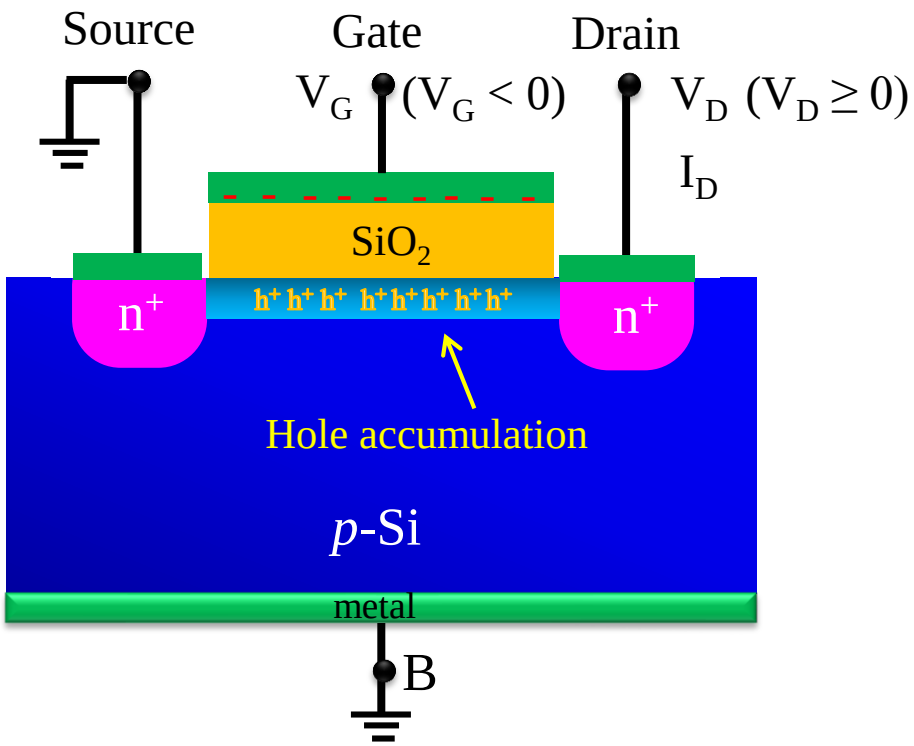
- Gate voltage modulate the conductivity of the semiconductor region just below the gate. → Channel
- Charge carrier in channel is electron ⇒ n-channel MOSFET (NMOS)
- Charge carrier in channel is hole ⇒ p-channel MOSFET (PMOS)

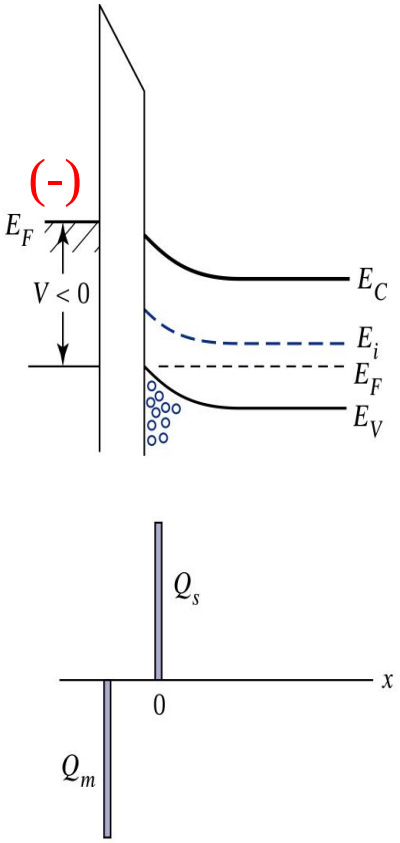
MOS Field-effect transistor

Operation of MOSFET (Gate voltage)

1) Accumulation

$V_G < 0$ and $< V_T$





Only holes are accumulated between the source and drain.

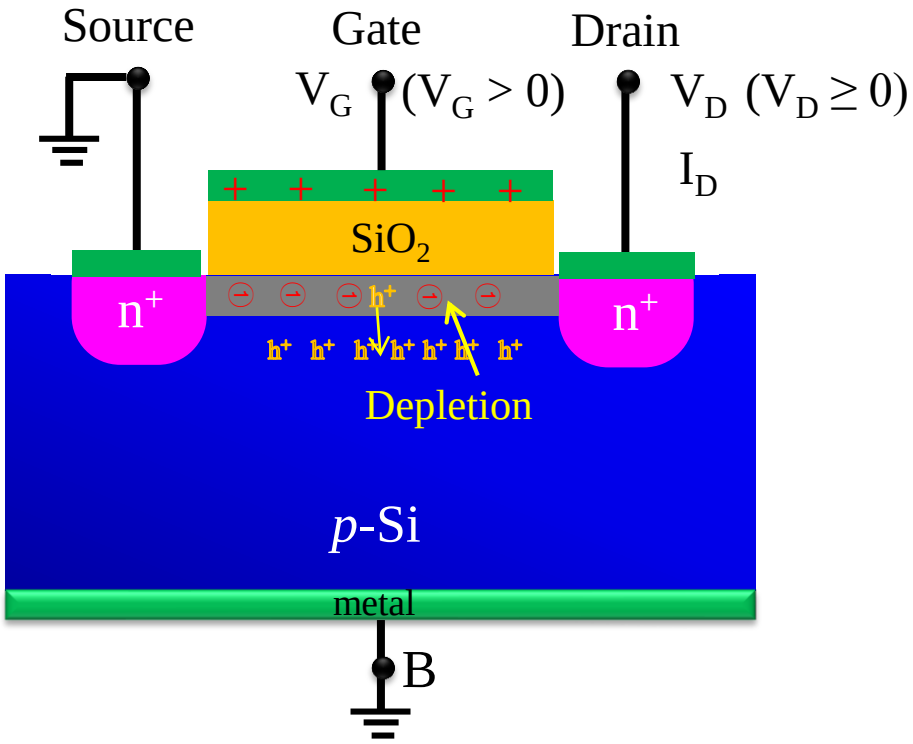
➔ No current between source and drain

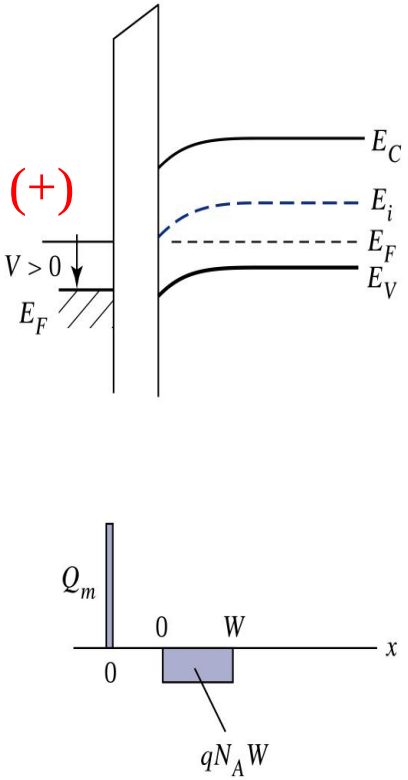
MOS Field-effect transistor

Operation of MOSFET (Gate voltage)

2) Depletion

$0 < V_G < V_T$





Holes are depleted between the source and drain.

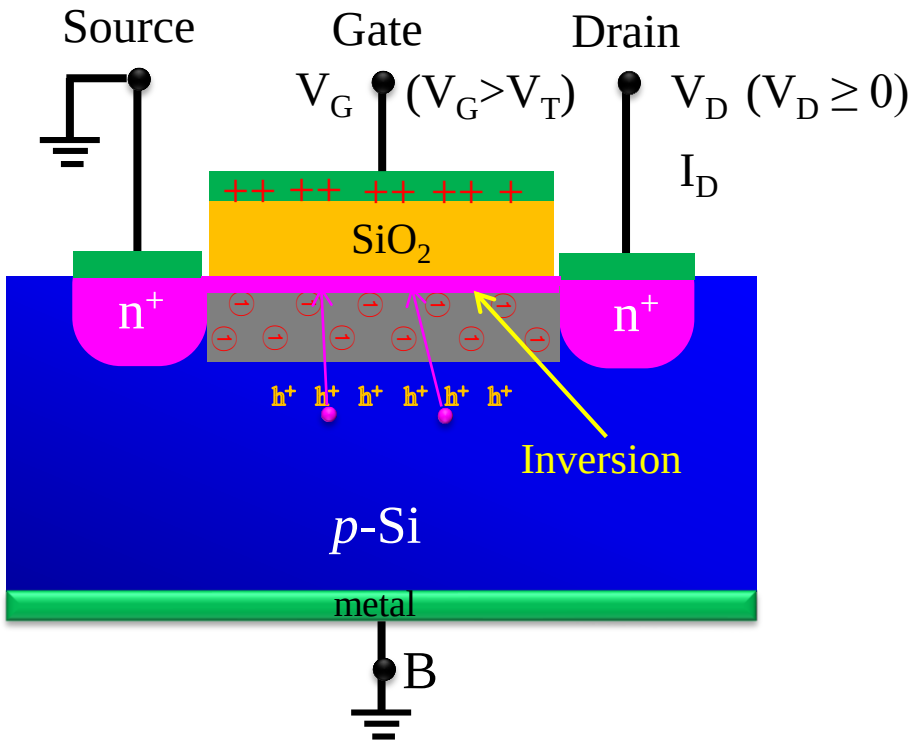
➔ No current between source and drain

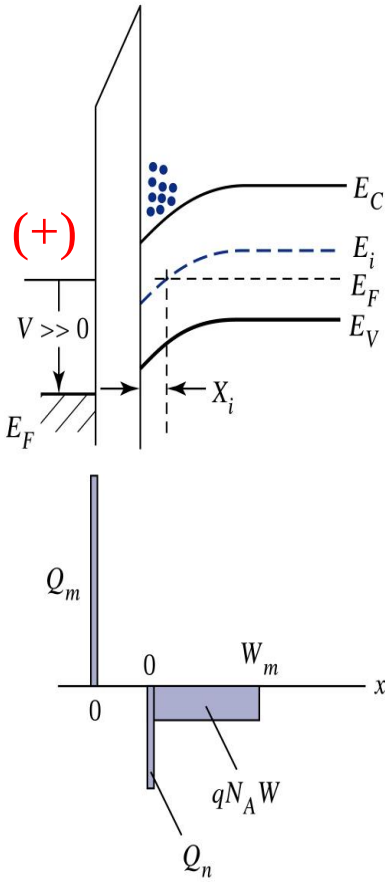
MOS Field-effect transistor

Operation of MOSFET (Gate voltage)

3) Inversion

$0 < V_T < V_G$





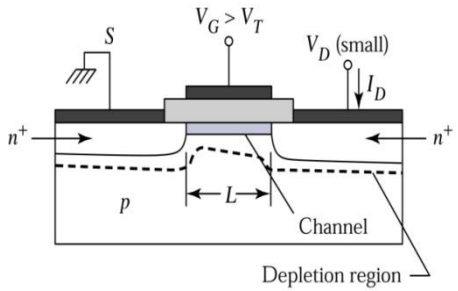
Inversion layer is formed between the source and drain.

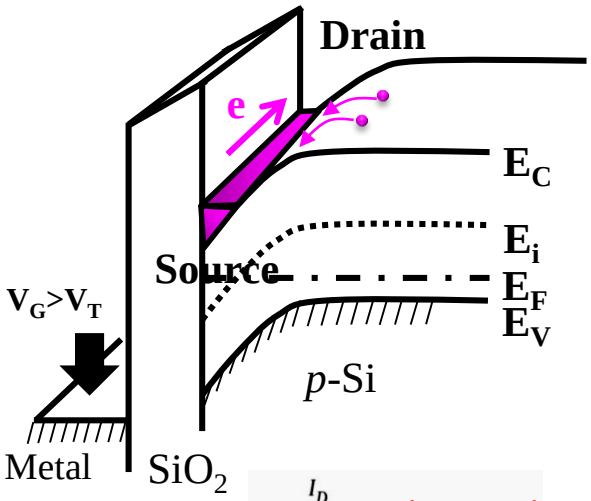
→ Channel ➔ Current flow between source and drain

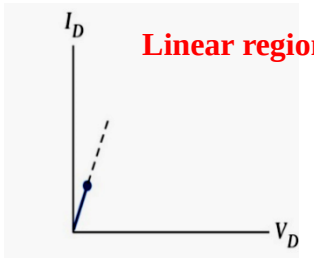
MOS Field-effect transistor

Operation of MOSFET (Drain voltage)

1) $V_D > 0$

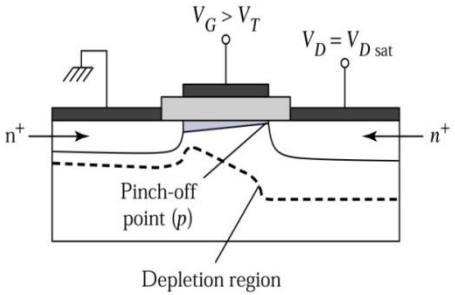


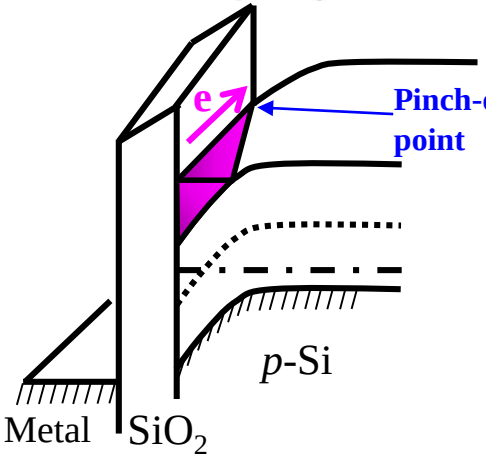


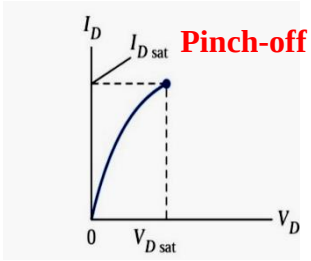


Linear region

2) $V_D \sim V_{D\,sat}$

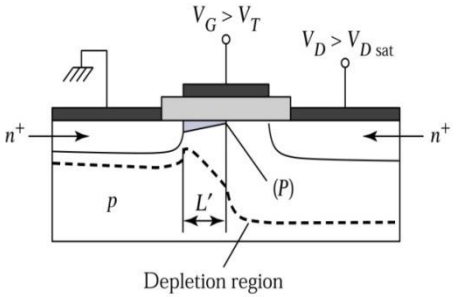


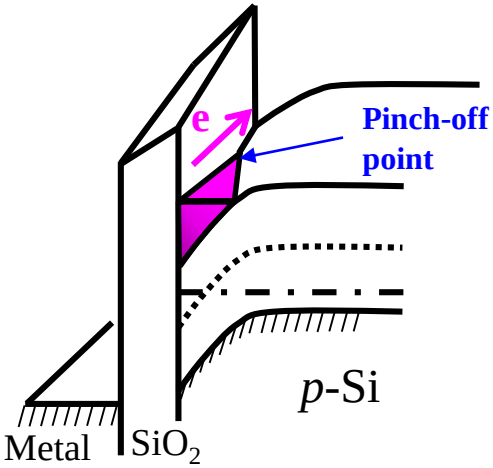


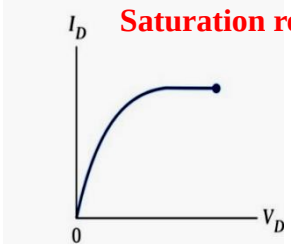


Pinch-off point

3) $V_D > V_{D\,sat}$







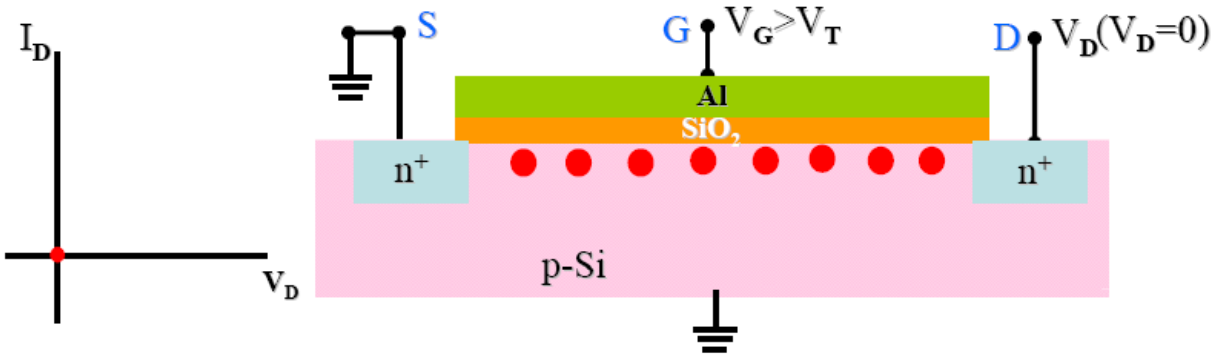
Saturation region

MOS Field-effect transistor

Operation of MOSFET (Drain voltage)

1) Zero drain voltage ($V_D = 0$)

$V_D = 0, V_G > V_T \longrightarrow I_D = 0$



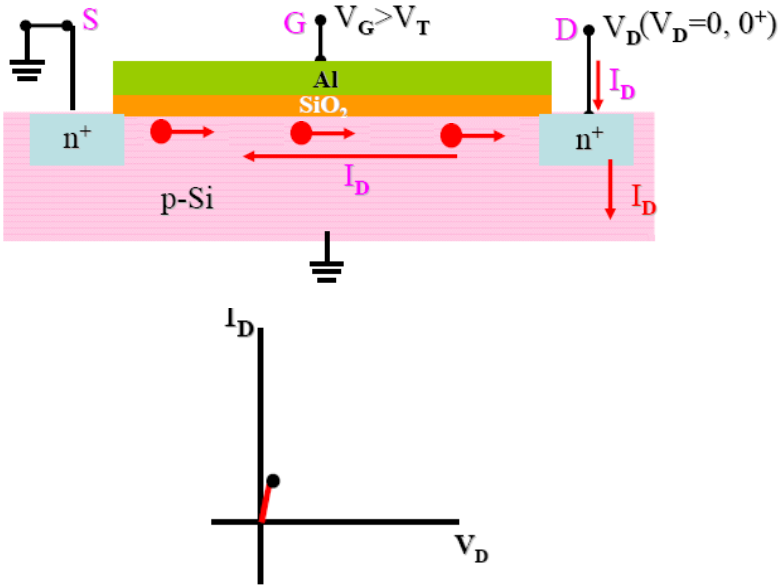
- Mobile electrons pile up at the interface between Si and SiO_2.
- Higher gate bias : more electrons pile up ⇒ increase channel conductance
- Still, no current (very small) flows because no potential gradient exist

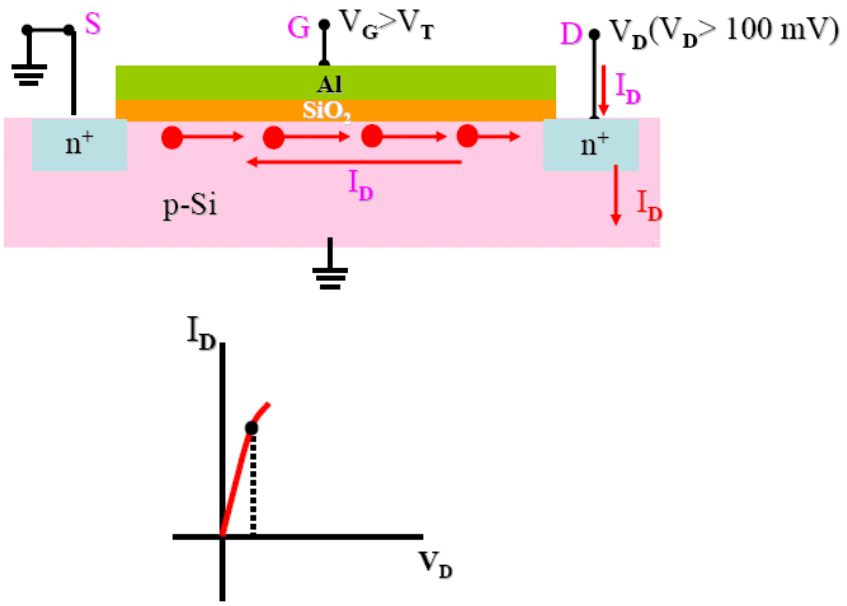
MOS Field-effect transistor

Operation of MOSFET (Drain voltage)

2) Linear region ($V_D > 0$)

$$V_D > 0,\ V_G > V_T \Longrightarrow I_D = V_D/R$$





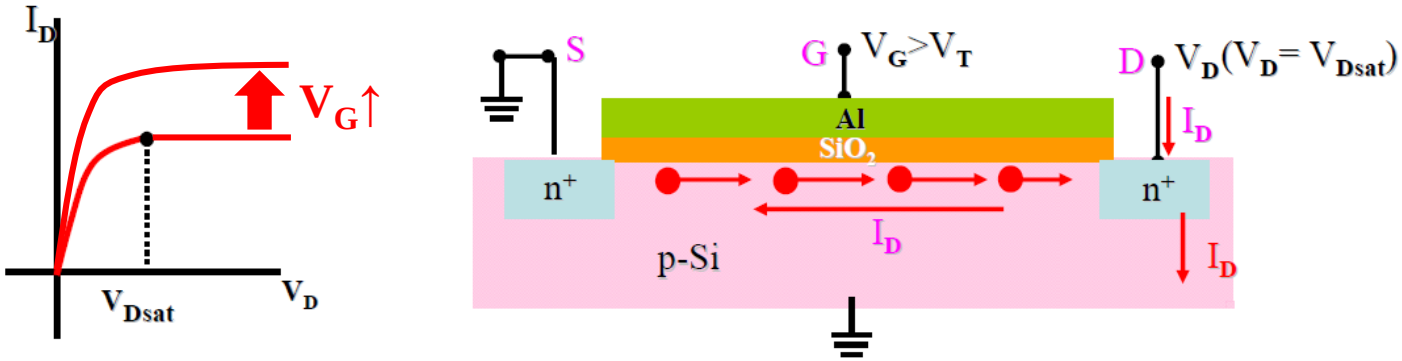
- Depletion width widen due to V_{DS} .
- Further increase of V_D ⇒ progressive reduction of the carrier concentration in the channel ⇒ decrease conductance of channel ⇒ slowly increase I_D
- Increase of V_G ⇒ increase conductance of channel ⇒ Increase I_D

MOS Field-effect transistor

Operation of MOSFET (Drain voltage)

3) Saturation region ($V_D > V_{D,sat}$)

$V_D \geq V_{D,sat}$, $V_G > V_T$ ⟶ I_D = saturation



- Depletion width is further widen due to V_{DS} .
- Slope of V_D-I_D is “zero”

- $V_D \geq V_{D,sat}$ ➔ “pinch off”

Chapter 10. Optoelectronic Devices

Optoelectronic (Photonic) devices

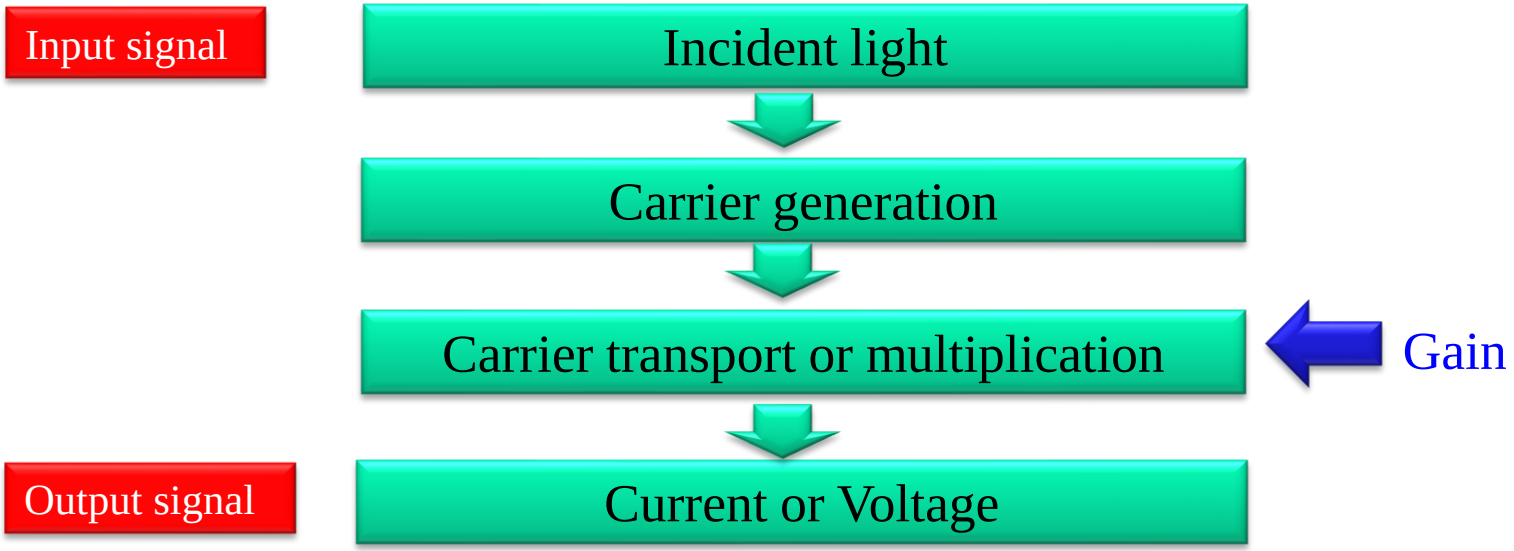
Light-Emitting Diode (LED)
Laser Diode (LD)

Photodetectors

Solar cells

Photodetector

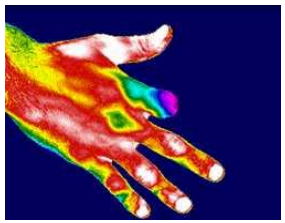
Principle of photodetector : photoconductor / photodiode



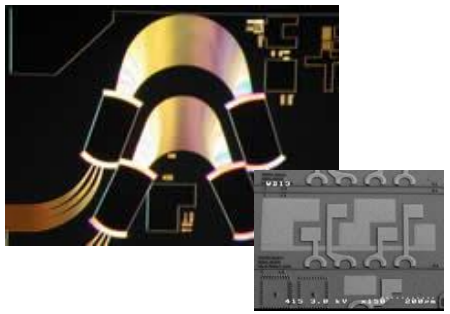
Optical receiver

Night vision

Thermal images



Photonic Integrated Circuits

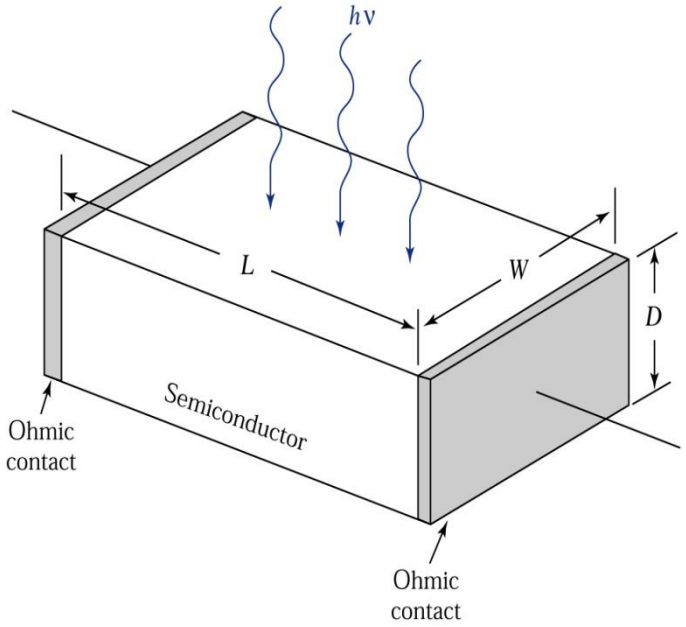


Photodetector

1) Photoconductor

Conductivity of semiconductors

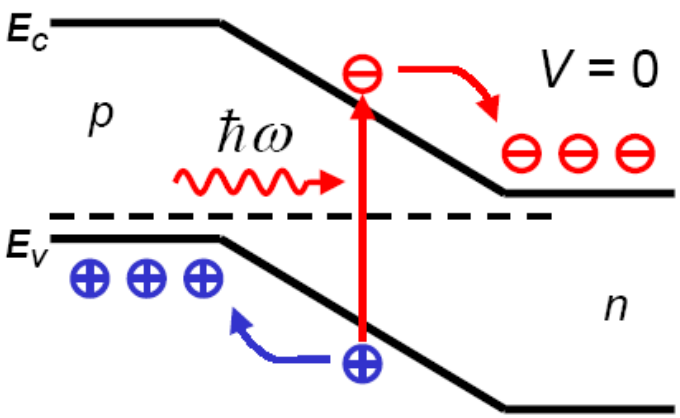
$$\sigma = q\left(\mu_n n + \mu_p p\right)$$ *Shining light* → *n* and *p* increase → σ increase

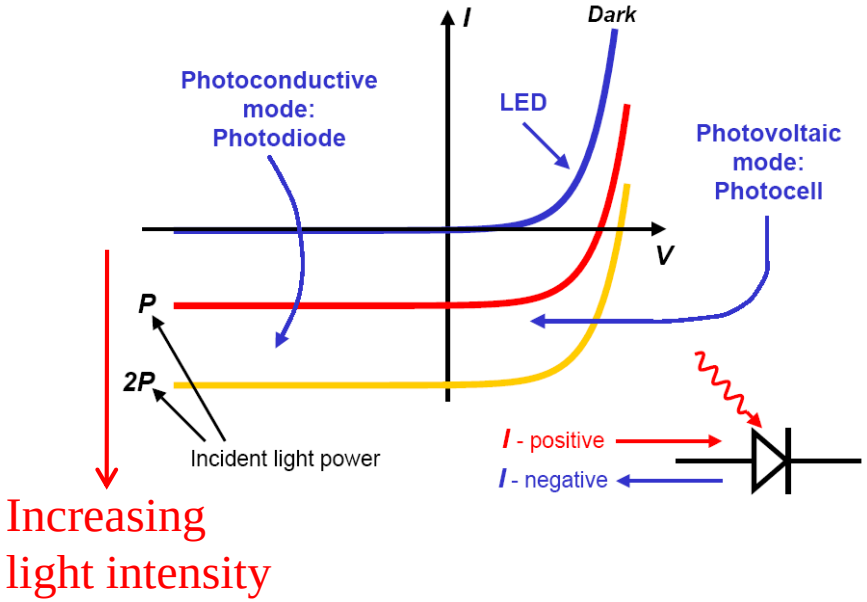


Photodetector

(2) Photodiode

Reverse biased *p*-*n* junction or metal-semiconductor junction





End of Slide