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NTE74163
Integrated Circuit
TTL – Synchronous 4–Bit Binary Counter

Description:

The NTE74S163 is a synchronous, presettable binary counter with direct clear in a 16–Lead DIP type package that feature an internal carry look–ahead for application in high–speed counting designs. Synchronous operation is provided by having all flip–flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count–enable inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with asynchronous (ripple clock) counters, however counting spikes may occur on the (RCO) ripple carry output. A buffered clock input triggers the four flip–flops on the rising edge of the clock input waveform.

This counter is fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. The clear function of the NTE74S163 is synchronous and a low level at the clear input sets all four flip–flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to 0000 (LLLL).

The carry look–ahead circuitry provides for cascading counters for n–bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count–enable inputs and a ripple carry output. Both count–enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high–level output pulse with a duration approximately equal to the high–level portion of the Q_A output. This high–level overflow ripple carry pulse can be used to enable successively cascaded stages. Transitions at the enable P or T inputs of the NTE74S163 is allowed regardless of the level of the clock input.

The NTE74S163 features a fully–independent clock circuit. Changes at control inputs (enable P or T, or load) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

Features:

- Internal Look–Ahead for Fast Counting
- Carry Output for n–Bit Cascading
- Synchronous Counting
- Synchronously Programmable
- Load Control Line
- Diode–Clamped Inputs

Absolute Maximum Ratings: (Note 1)

Supply Voltage, V_{CC} 7V
DC Input Voltage, V_{IN} 5.5V
Interemitter Voltage (Note 2) 5.5V
Power Dissipation, P_D 475mW
Operating Temperature Range, T_A . . . . . 0°C to +70°C
Storage Temperature Range, T_{stg} . . . . . −65°C to +150°C

Note 1. Unless otherwise specified, all voltages are referenced to GND.
Note 2. This is the voltage between two emitters of a multiple−emitter transistor. For these circuits, this rating applies between the count enable inputs P and T.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
High−Level Output Current	I_{OH}	–	–	−1	μA
Low−Level Output Current	I_{OL}	–	–	20	mA
Clock Frequency	f_{clock}	0	–	40	MHz
Width of Clock Pulse	$t_{w(clock)}$	10	–	–	ns
Width of Clear Pulse	$t_{w(clear)}$	10	–	–	ns
Setup Time Data Inputs A, B, C, D	t_{su}	4	–	–	ns
ENP or ENT		12	–	–	ns
$\overline{LOAD}$		14	–	–	ns
$\overline{LOAD}$ Inactive State		12	–	–	ns
$\overline{CLR}$		14	–	–	ns
$\overline{CLR}$ Inactive State		12	–	–	ns
Hold Time Data Inputs A, B, C, D	t_h	3	–	–	ns
$\overline{LOAD}$		0	–	–	ns
$\overline{CLR}$		0	–	–	ns
Operating Temperature Range	T_A	0	–	+70	°C

Electrical Characteristics: (Note 3, Note 4)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		2	–	–	V
Low Level Input Voltage	V_{IL}		–	–	0.8	V
Input Clamp Voltage	V_{IK}	V_{CC} = MIN, I_I = −18mA	–	–	−1.2	V
High Level Output Voltage	V_{OH}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = −1mA	2.7	3.4	–	V
Low Level Output Voltage	V_{OL}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 4mA	–	–	0.5	V
Input Current	I_I	V_{CC} = MAX, V_I = 5.5V	–	–	1	mA

Note 3. .For conditions shown as MIN or MAX, use the appropriate value specified under “Recommended Operation Conditions”.
Note 4. All typical values are at V_{CC} = 5V, T_A = +25°C.

Electrical Characteristics (Cont'd): (Note 3, Note 4)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
High Level Input Current CLK and Data Inputs	I_{IH}	V_{CC} = MAX, V_I = 2.7V	–	–	50	μA
All Other Inputs			–10	–	–200	μA
Low Level Input Current ENT	I_{IL}	V_{CC} = MAX, V_I = 0.5V	–	–	–4	mA
All Other Inputs			–	–	–2	mA
Short–Circuit Output Current	I_{OS}	V_{CC} = MAX, Note 5	–40	–	–100	mA
Supply Current	I_{CC}	V_{CC} = MAX	–	95	160	mA

Note 3. .For conditions shown as MIN or MAX, use the appropriate value specified under "Recommended Operation Conditions".

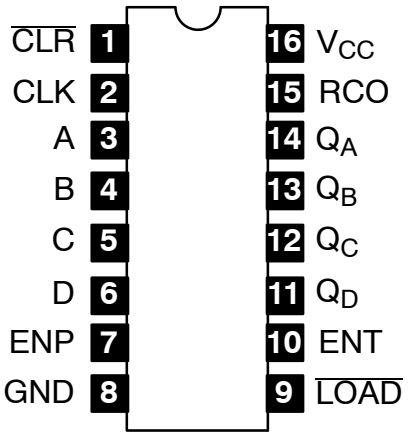
Note 4. All typical values are at V_{CC} = 5V, T_A = +25°C.

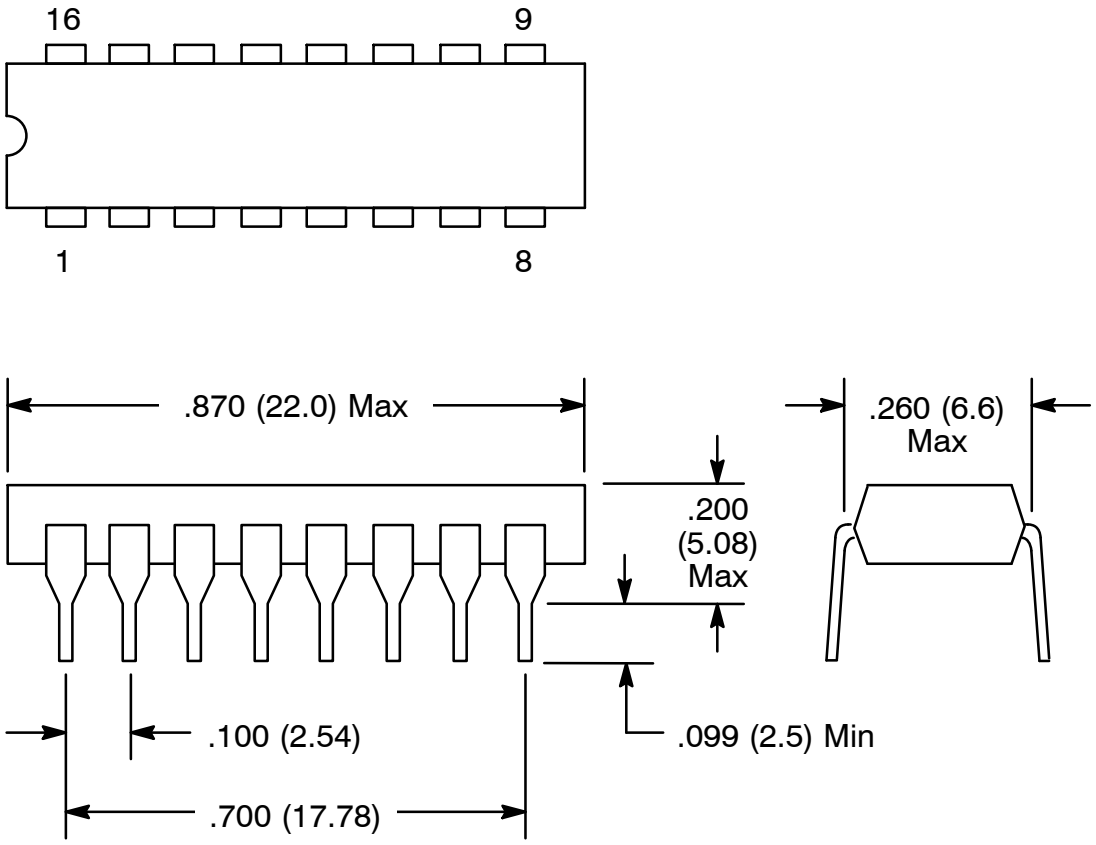
Note 5. Not more than one output should be shorted at a time and duration of short–circuit should not exceed one second.

Switching Characteristics: (V_{CC} = 5V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Maximum Clock Frequency	f_{max}	R_L = 280Ω, C_L = 15pF	40	70	–	MHz
Propagation Delay Time (From CLK Input to RCO Output)	t_{PLH}		–	14	25	ns
	t_{PHL}		–	17	25	ns
Propagation Delay Time (From CLK Input to Any Q Output)	t_{PLH}		–	8	15	ns
	t_{PHL}		–	10	15	ns
Propagation Delay Time (From ENT Input to RCO Output)	t_{PLH}		–	10	15	ns
	t_{PHL}		–	10	15	ns

Pin Connection Diagram




16
9
1
8
.870 (22.0) Max
.260 (6.6)
Max
.200
(5.08)
Max
.100 (2.54)
.099 (2.5) Min
.700 (17.78)