Name: _____.

- Exam 3: 12/6 8:00—9:15PM, 105 Forum
- Conflict exam 3: 12/6 12:05—1:20PM (class time), Westgate W375
- Complete the **Exam 3 availability survey**!!!

- No calculator needed
- Everything after Exam 2 can be on Exam 3 (including the latter part of cache)
- Review below questions, online quizzes, Kahoot.
- Additionally, be prepared for questions asking to “Explain” simple concepts or advantages/disadvantages, etc.

- No office hour this Wednesday
- No class this Thursday

Name: _____.

Q1. What will the following virtual address be translated into? Answer in hexadecimal. You should put 0x at the beginning of your answer (e.g., 0x12345678).

Here the virtual address is 32bit and the physical address is 28bit.

Assume the page is 4KB.

Virtual address: 0x00003abc

Page table (assume all the entries are valid)

0x1234
0x5678
0x9abc
0xdef2
0x426a

Q2. What will the following virtual address be translated into? Answer in hexadecimal. You should put 0x at the beginning of your answer (e.g., 0x12345678).

Here the virtual address is 32bit and the physical address is 28bit.

Assume the page is 1MB.

Virtual address: 0x00003abc

Page table (assume all the entries are valid)

0x12
0x56
0x9a
0xde
0x42

Name: _____.

Q3. What will the following virtual address be translated into? Answer in hexadecimal. You should put 0x at the beginning of your answer (e.g., 0x12345678).

If you result in a TLB miss, write "TLB miss" in the answer.

Here the virtual address is 32bit and the physical address is 28bit.

Assume the page is 4KB.

Virtual address: 0x00003abc

TLB (fully associative, assume all the entries are valid)

Tag (VPN)	PPN
0x00003	0x1234
0x0003a	0x5678
0x00000	0x90ab
0x03abc	0xcdef

Q4. Can you overlap cache access with the TLB access in the following case?

Page size: 4KB

words in a cache block: 4

blocks in a direct-mapped cache: 256

Q5. What is the possible maximum number of words in a cache block to allow cache / TLB access overlap?

Page size: 16KB

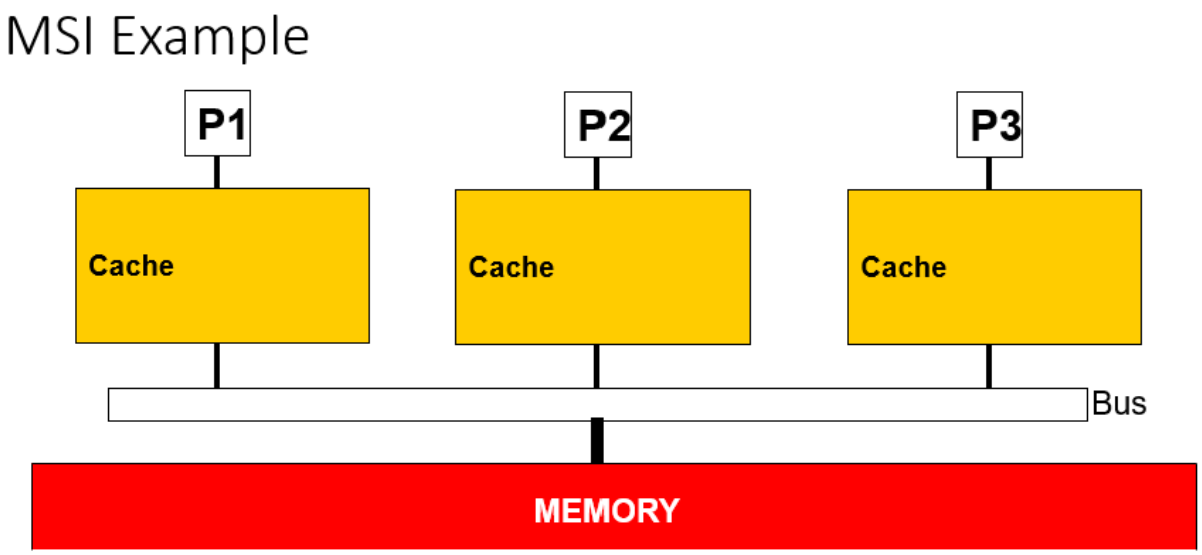
words in a cache block: ??

blocks in a direct-mapped cache: 512

Name: _____.

Q6. Draw a state diagram for MSI writeback invalidation protocol.

Q7. Fill the below table. Assume initially all state are I.



Processor Action	State in P1	State in P2	State in P3	Bus Transaction	Data Supplier
P1 reads X					
P3 reads X					
P3 writes X					
P1 reads X					
P2 reads X					

Name: _____.

Q8. Write a function that acquires a lock using atomic exchange.

Q9. Write a function that acquires a lock using ll (load-linked) and sc (store-conditional).