Quiz 4: OoO

Due Oct 17 at 11:59pm **Points** 10 **Questions** 10 **Available** after Oct 13 at 1:20pm **Time Limit** None **Allowed Attempts** 3

Take the Quiz Again

Attempt History

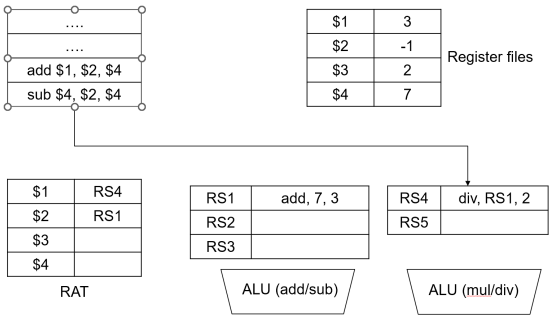
	Attempt	Time	Score
LATEST	Attempt 1	7 minutes	6.83 out of 10

Answers will be shown after your last attempt

Score for this attempt: **6.83** out of 10
Submitted Oct 18 at 6:37am
This attempt took 7 minutes.

Question 1

1 / 1 pts



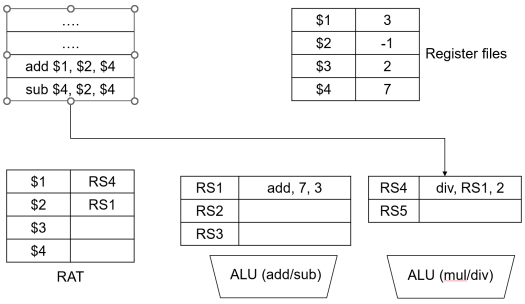
From the above diagram, when the sub instruction is issued, what will the two source address $2 and $4 be renamed into?

$2 RS1

$4 7

Question 2

1 / 1 pts



From the above diagram, when the add instruction is issued, what will be the two source addresses $2 and $4 be renamed into?

(add is issued after the sub, and assume that sub is placed at RS2 after being issued)

$2 RS1

$4 RS2

Question 3

1 / 1 pts

RS1	add, 7, 3
RS2	sub, RS3, RS1
RS3	add, RS1, 2

ALU (add/sub)

RS4	div, RS1, RS2
RS5	

ALU (mul/div)

From the above reservation station, order instructions in each RS in the order they will be executed.

Place the instruction that will be executed first next to 1.

1 RS1

2 RS3

3 RS2

4 RS4

Question 4

1 / 1 pts

What is NOT true about the broadcast stage of the original Tomasulo's algorithm (w/o ROB)?

- (•) Register file is not updated
- ( ) RAT is released
- ( ) source registers in the reservation station is updated
- ( ) Instructions in the reservation station that were not ready can become ready

Partial

Question 5

0.33 / 1 pts

[MULTIPLE ANSWERS] Which of the following can still slow down the execution even after register renaming?

- [x] RAW dependencies between registers
- [ ] WAW dependencies between registers
- [ ] WAR dependencies between registers
- [ ] WAR dependencies between load/store
- [ ] WAW dependencies between load/store

Partial

Question 6

0.5 / 1 pts

[MULTIPLE ANSWERS] What is NOT true about the broadcast stage of an OoO processor WITH ROB?

- [x] Register file is updated
- [ ] RAT is released
- [ ] Source registers in the reservation station is updated
- [ ] ROB is updated

Question 7

1 / 1 pts

What is NOT true about commit stage?

- (•) Commit can happen out-of-order
- ( ) ROB entry is released

- Register file is updated
- RAT is released

Question 8

1 / 1 pts

Let's say the LSQ was initially empty. Assume a sequence of load and store.

sw $1, 0($2)

sw $3, 0($2)

lw $4, 0($2)

What will be the value of $4, and from where the value is being read from?

- (•) The value of $3, LSQ
- ( ) The value of $3, cache or memory
- ( ) The value of $1, LSQ
- ( ) The value of $1, cache or memory

Incorrect

Question 9

0 / 1 pts

Consider the below code.

Inst 1: sw $1, 0($2)

Inst 2: lw $3, 0($4)

Inst 3: lw $5, 0($6)

Which of the following statement is correct for a conservative load-store reordering?

- ( ) Inst 2 and 3 can be reordered, but Inst 1 must be executed first
- ( ) Inst 1 and 2 can be reordered
- ( ) Inst 1, 2, 3 can all be reordered
- (•) No instructions can be reordered

Incorrect

Question 10

0 / 1 pts

Consider the below code.

Inst 1: sw $1, 0($2)

Inst 2: lw $3, 0($4)

Inst 3: lw $5, 0($6)

Let's say the machine did aggressive reordering, and executed in the order of Inst 2 > Inst 1 > Inst 3

What should be done when Inst 1 (sw) was executed?

- ( ) It must check the memory addr Inst 2 accessed using LSQ
- ( ) It must check the memory addr Inst 3 accessed using LSQ
- ( ) It does not need to do any check
- (•) It must both check the memory addr Inst 2, 3 accessed using LSQ

Quiz Score: **6.83** out of 10