Computer Science and Engineering 431

First Midterm Exam

Spring 2022

2/17/2022

Name_____

1	25	
2	25	
3	25	
4	25	
Total	100	

NOTE:

You have 1 hour and 15 minutes to complete the exam.

This exam is closed notes and book.

Please write down solution steps and partial credits are considered.

The total points of this exam are 100 points. The maximum points for each question are indicated.

1. (25pts) Performance Evaluation

A. (2 pts) Give the performance equation (ignoring memory system effects) discussed in the class, and explain its components.

Cycle per instruction · clock cycle time · Instruction count.

$$ET = CPI \times CCT \times IC$$

B. (2 pts) The following measurements have been made using a simulator for a design that is projected to have a clock rate of 1GHz. What is the design's CPI?

Instruction class	CPI	Frequency
R-type (ALU)	1	45%
Load	5	25%
Branch	2	15%
Jump	2	5%
Store	3	10%

$$0.45 + 0.25\times5 + 0.15\times2 + 0.05\times2 + 0.1\times3 = \boxed{2.4}$$

C. (2 pts) How does this compare to using branch prediction to shave one cycle off the branch time?

$$2.4 - 0.15 = \boxed{2.25}$$

D. (4 pts) Assume that an optimized version of the design has been implemented which doubles the projected clock rate to 2 GHz but also doubles the CPI of each instruction class except stores. Which design is faster, the 1GHz version or the 2 GHz version, and by how much (the 1 GHz version is the one in question B, not the one in C)?

2GHz version

new CPI $= 4.8 - 0.3 = 4.5$

$$\frac{ET_{old}}{ET_{new}} = \frac{1\times2.4}{0.5\times4.5} = \frac{4.8}{4.5} \simeq 1.07\times$$

E. (5 pts) Why are pipeline state registers required in a pipeline datapath? Explain what each of the pipeline registers stores when executing r-type and store instructions.

To hold necessary values/control signals.

R-type, store → can be found in the slides (I will skip)

F. (5 pts) Consider the following loop instruction sequence:

```
Loop:  add $3, $3, $2     ... → 4 cycles
       lw $4, -100($3)    ... → 5 cycles
       beq $3, $4, Loop   ... → 3 cycles
```

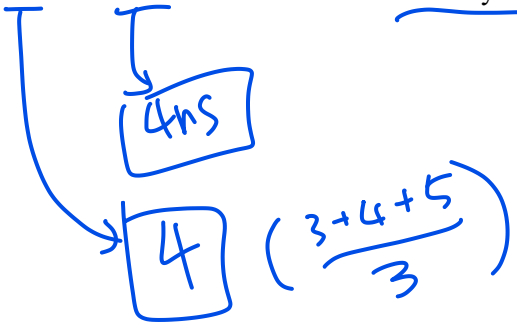
Suppose this loop executes exactly 3 times (iterations). Further assume that we have 5 execution stages, Instruction fetch, reading resource from register file, performance and ALU computation, reading or writing memory, storing data back to the register file and that the clock times for these stages are 4ns, 1ns, 2ns, 4ns, 1ns, in that order. What is the CPI and CCT of the 3-iteration loop in a single-cycle machine?

CCT: 12ns

IC: 9

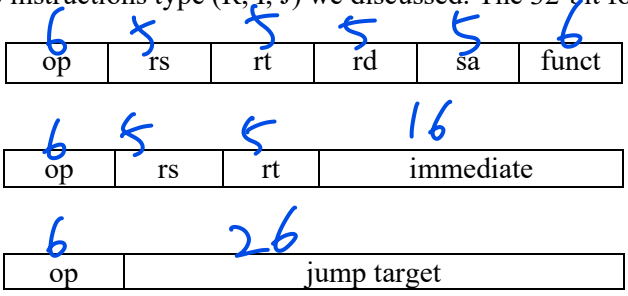
CPI = 1

G. (5 pts) In G, what is the CPI and CCT in 3 iterations in a multi-cycle machine?



2 (25 pts) MIPS Instructions

A. (6 pts) Recall the MIPS instructions type (R, I, J) we discussed. The 32-bit formats are shown here:



Indicate the bits for each part and explain the functionalities of op, funct, and immediate fields.

See the slides.

B. (2 pts) The IBM PowerPC supports an addressing mode called indexed addressing which adds the values stored in two registers (whose register file addresses are contained in the instruction) together to form the memory address of operand. If this were an addressing mode supported by MIPS machine, what instructions format (R, I or J) would it be?

R. Because only R can use 3 regs (2 for mem addr, 1 for data load/store)

C. (4 pts) The individual stages of a pipelined datapath have the latencies and the instruction percentage has the mix as shown in the tables below.

IF	ID	EX	MEM	WB
300ps	300ps	400ps	500ps	200ps

ALU	BEQ	LW	ST
45%	20%	25%	10%

1700ps

500ps

What is the fastest possible clock time (in ps) for a non-pipelined, single-cycle MIPS datapath and for a 5-stage pipelined MIPS datapath, respectively?

D. (2 pts) How are memory structural hazards avoided in our 5-stage MIPS pipelined datapath?

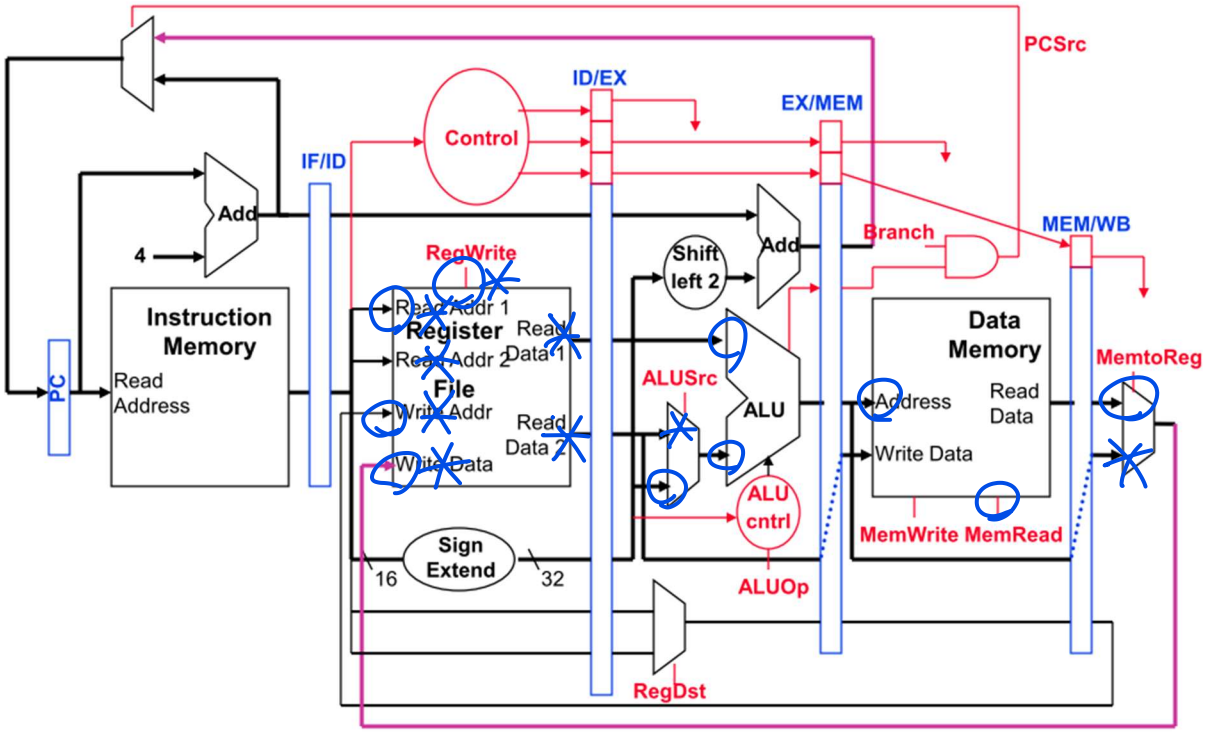
Separate IM/DM

E. (6 pts) Consider the following instruction sequence executed on a 5-stage pipeline in-order machine.

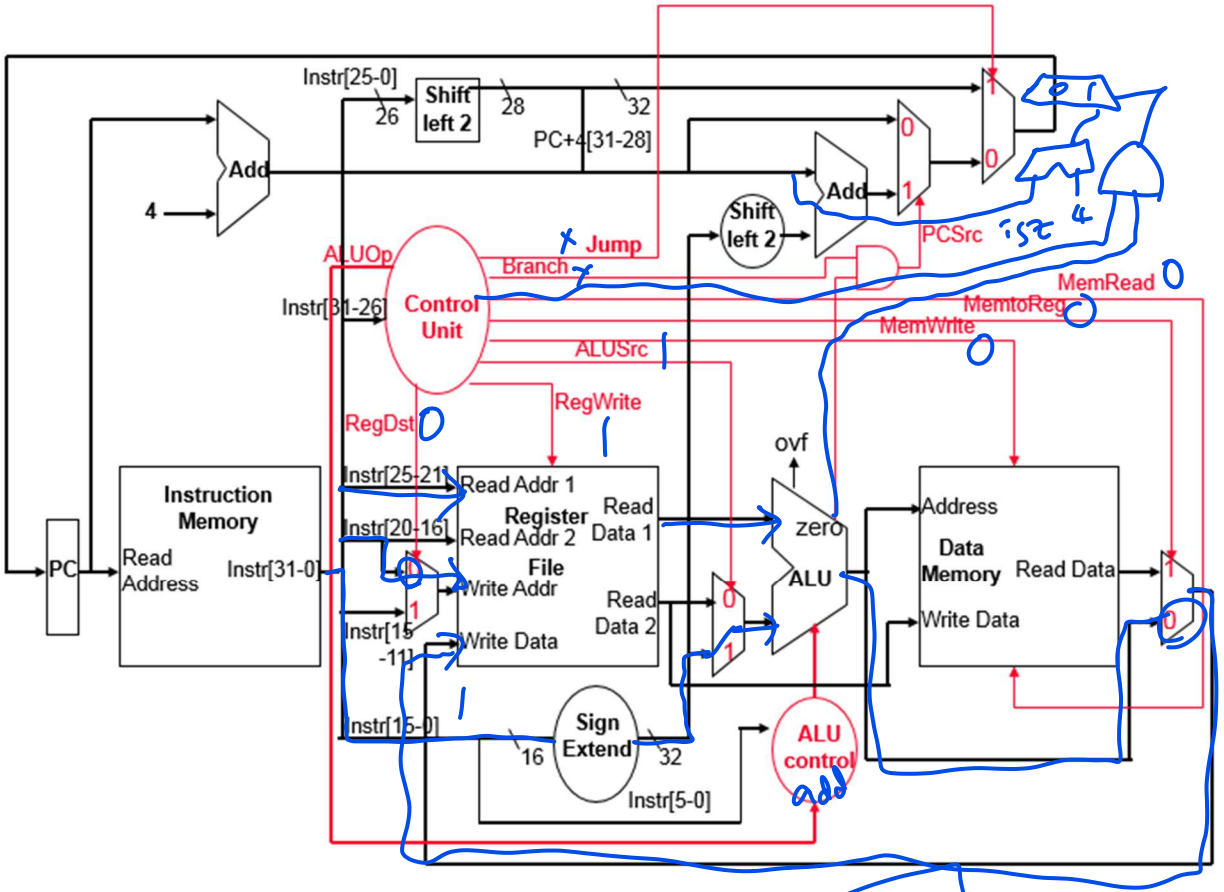
sw $2 100($3)

sub $5, $2, $4

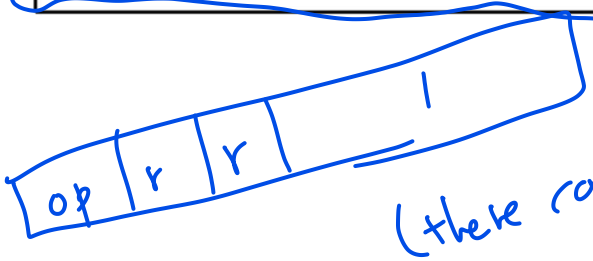
Indicate, on the figure below, the components that will be activated to execute lw and add instructions above, using *circle* (o) and *star* (*) to denote lw and add, respectively.



F. (5 pts) Modify the MIPS single cycle datapath shown below to accommodate a new instruction, isz (increment and skip on zero), which increments (by 1) the contents of a register, stores the incremented value back in the register, and skips the next instruction if the result of the incrementing is zero. All other instructions remain unchanged. What new or expanded (in terms of number of bits) control signals need to be added, if any? Be sure to indicate what instruction format you are using and how the instruction fields are used.



I-type

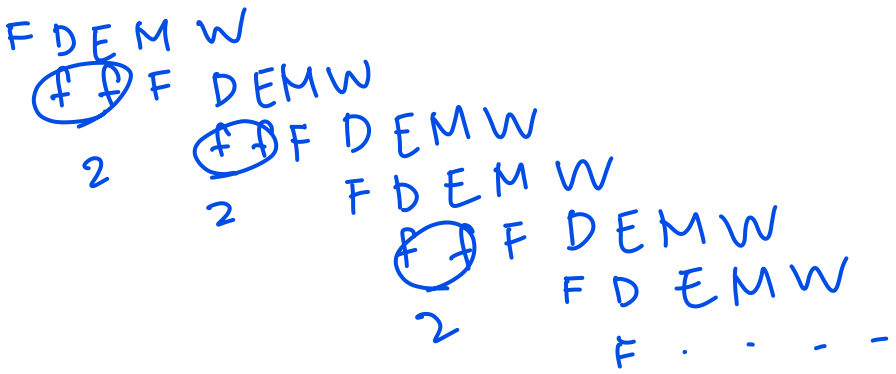


(there can be different solutions)

3. (25 pts) Data Hazards

A. (8 pts) Consider the following execution sequence:

1. add $4, $2, $2
2. lw $1, 0($4)
3. and $5, $3, $1
4. and $6, $6, $2
5. or $6 $3, $6
6. sw $1, 4($4)
7. lw $2, 4($4)



Find the all the data hazards and fill the following table (you may leave some entries blank or add more rows to accommodate your answer).

Instruction #1	Instruction #2	Register	Hazard Type

skip

B. (5 pts) Suppose the code sequence in A is executed in a 5-stage pipelined in-order execution machine. How many *nops* do we need to insert into the pipeline without a forwarding unit?

6.

C. (5 pts) How many *nops* do we need to insert to the pipeline with a forwarding unit?

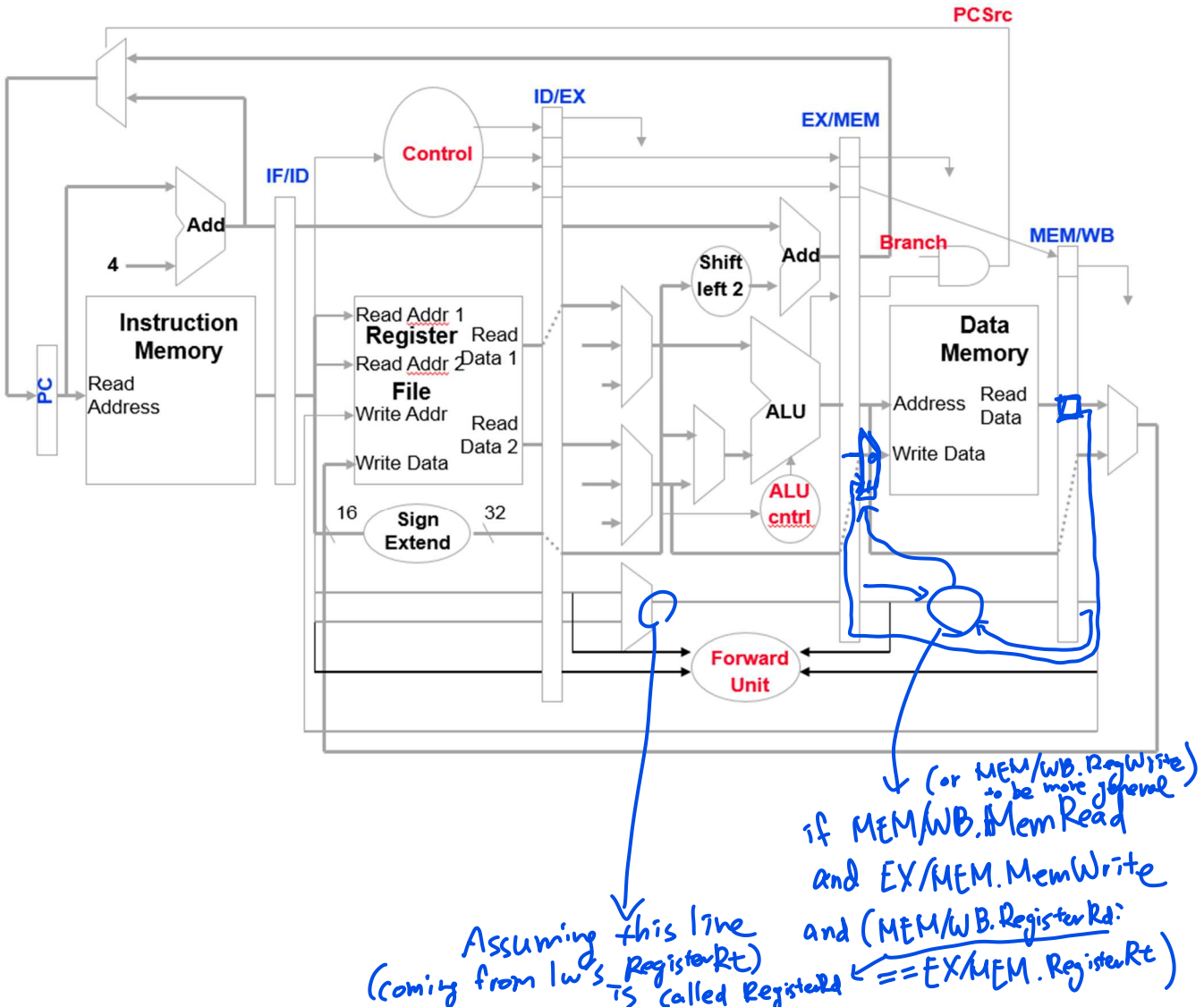
1

(between #2 and #3)

D (7 pts) Add to the diagram below the connections that can enable data forwarding in the pipeline, to prevent stalls in the following instruction sequence (do not include any connections that is not necessary for this sequence).

lw $1, 100($3)

sw $1, 100($2)



4. (25 pts) Branches

A. (4 pts) Explain two strategies to handle control hazards.

Decide Early

Predict

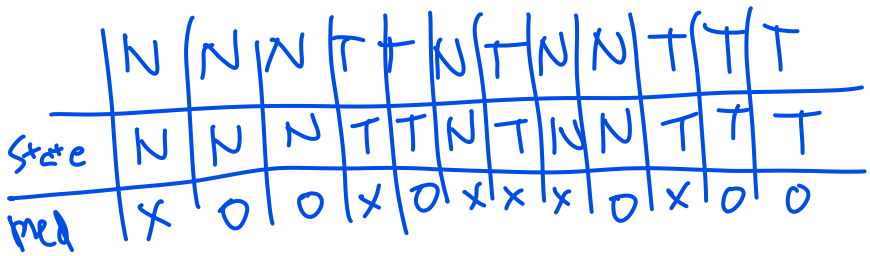
B. (7 pts) Consider a branch that has the following outcome pattern (T for taken, N for not taken).

N N N T T N T N N T T T

How many branches are predicted correctly with a static (0-bit) always-taken branch predictor for this branch outcome pattern.

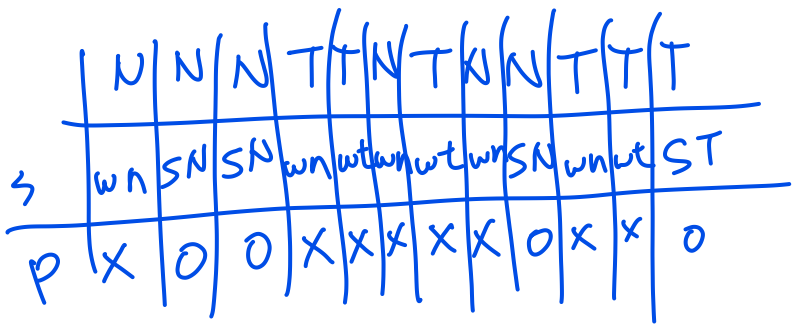
6

C. (7 pts) Using the same sequence from B. How many branches are predicted correctly with a dynamic 1-bit predictor where the initial state is Taken (T) for this branch outcome pattern?



6

D. (7 pts) How many branches are predicted correctly with a dynamic, saturating counter 2-bit predictor for the branch outcome pattern in B? Suppose the four states are strong not taken (SN), weak not taken (wn), weak taken (wt) and strong taken (ST). Assume that the initial prediction state is wt (weak taken).



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