Unnamed Quiz

Due Nov 14 at 11:59pm **Points** 7 **Questions** 7 **Available** after Nov 10 at 12am **Time Limit** None **Allowed Attempts** 3

Take the Quiz Again

Attempt History

	Attempt	Time	Score
LATEST	Attempt 1	3 minutes	2 out of 7

Answers will be shown after your last attempt

Score for this attempt: **2** out of 7
Submitted Nov 10 at 9:05am
This attempt took 3 minutes.

Unanswered **Question 1** 0 / 1 pts

Assume a MSI writeback invalidation protocol.

Write the state transition and a corresponding bus activity that must be done for each scenario:

For STATE, write either M, S, or I

For ACTION, write either None, BusRd, BusRdX, Flush

Cur State	Event	Next State	Action
I	Processor read		
I	Processor write		
S	Processor read		
S	Processor write		
S	Snoop BusRd		
S	Snoop BusRdX		
M	Processor read		
M	Processor write		
M	Snoop BusRd		
M	Snoop BusRdX		

Answer 1:

(You left this blank)

Answer 2:

(You left this blank)

Answer 3:

(You left this blank)

Answer 4:

(You left this blank)

Answer 5:

(You left this blank)

Answer 6:

(You left this blank)

Answer 7:

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Answer 8:

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Answer 9:

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Answer 10:

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Answer 11:

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Answer 12:

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Answer 13:

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Answer 14:

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Answer 15:

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Answer 16:

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Answer 17:

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Answer 18:

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Answer 19:

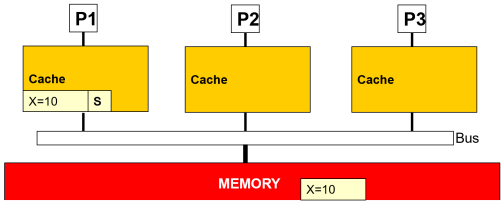
(You left this blank)

Answer 20:

(You left this blank)

Question 2

1 / 1 pts

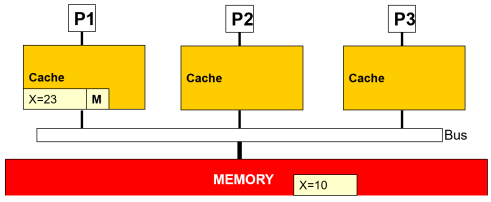


In this scenario, what is NOT true if P2 tries to read X, in an MSI protocol?

- (●) It gets the block from P1
- ( ) The block becomes S state
- ( ) P1's state does not change
- ( ) P2 sends BusRd through the bus

Question 3

1 / 1 pts



In this scenario, what is TRUE if P2 tries to read X, in an MSI protocol?

- (●) It gets the block from P1
- ( ) P1's block becomes I state
- ( ) P2's block becomes M state
- ( ) P2 sends a BusRdX signal

Unanswered **Question 4** 0 / 1 pts

Assume you implement a directory-based coherence protocol where you use 1 bit for processors to mark the presence.

If you have only 16 blocks (which is unrealistically small) and 256 processors, how many bits do you need to implement the directory?

Unanswered **Question 5** 0 / 1 pts

Assume you implement a directory-based coherence protocol where you limit the number of processors that can share the block into 4.

If you have only 16 blocks (which is unrealistically small) and 256 processors, how many bits do you need to implement the directory?

Unanswered **Question 6** 0 / 1 pts

In sequential consistency, what is NOT a possible outcome from the following code?
Initially, a = 0; b = 0;

Thread 1	Thread 2
a = 7; b = 3;	print(b); print(a);

- a=0, b=3
- a=0, b=0
- a=7, b=0
- a=7, b=3

Unanswered **Question 7** 0 / 1 pts

In processor consistency, can a = 0, b = 3 be possibly printed?

Thread 1	Thread 2
a = 7; b = 3;	print(b); print(a);

- True
- False

Quiz Score: **2** out of 7