

Quiz 5: TLB and virtual memory

Due Nov 7 at 11:59pm

Points 5

Questions 5

Available after Nov 3 at 12am

Time Limit None

Allowed Attempts 3

Attempt History

	Attempt	Time	Score
KEPT	Attempt 3	2 minutes	4 out of 5
LATEST	Attempt 3	2 minutes	4 out of 5
	Attempt 2	2 minutes	1 out of 5
	Attempt 1	33 minutes	2 out of 5

Score for this attempt: 4 out of 5

Submitted Nov 7 at 11:57am

This attempt took 2 minutes.

Question 1

1 / 1 pts

What will the following virtual address be translated into? Answer in hexadecimal. You should put 0x at the beginning of your answer (e.g., 0x12345678).

Here the virtual address is 32bit and the physical address is 28bit.

Assume the page is 4KB.

Virtual address: 0x00003abc

Page table (assume all the entries are valid)

0x1234
0x5678
0x9abc
0xdef2
0x426a

Correct!

0xdef2abc

Correct Answers

0xdef2abc

Question 2

0 / 1 pts

What will the following virtual address be translated into? Answer in hexadecimal. You should put 0x at the beginning of your answer (e.g., 0x12345678).

Here the virtual address is 32bit and the physical address is 28bit.

Assume the page is 1MB.

Virtual address: 0x00003abc

Page table (assume all the entries are valid)

0x12
0x56
0x9a
0xde
0x42

You Answered

0x123abc

Correct Answers

0x1203abc

Question 3

1 / 1 pts

What will the following virtual address be translated into? Answer in hexadecimal. You should put 0x at the beginning of your answer (e.g., 0x12345678).

If you result in a TLB miss, write "TLB miss" in the answer.

Here the virtual address is 32bit and the physical address is 28bit.

Assume the page is 4KB.

Virtual address: 0x00003abc

TLB (fully associative, assume all the entries are valid)

Tag (VPN)	PPN
0x00003	0x1234
0x0003a	0x5678
0x00000	0x90ab
0x03abc	0xcdef

Correct!

0x1234abc

Correct Answers

0x1234abc

Question 4

1 / 1 pts

Can you overlap cache access with the TLB access in the following case?

Page size: 4KB

words in a cache block: 4

blocks in a direct-mapped cache: 256

Correct!

☒ True

☐ False

Question 5

1 / 1 pts

What is the possible maximum number of words in a cache block to allow cache / TLB access overlap?

Page size: 16KB

words in a cache block: ??

blocks in a direct-mapped cache: 512

Correct!

8

Correct Answers

8 (with margin: 0)

0 (with margin: 0)

Quiz Score: 4 out of 5