## Quiz 2: Pipelined processors and hazards

Due Sep 13 at 1:59am Points 7 Questions 7 Available after Sep 8 at 1:20pm Time Limit None Allowed Attempts 3

Attempt History

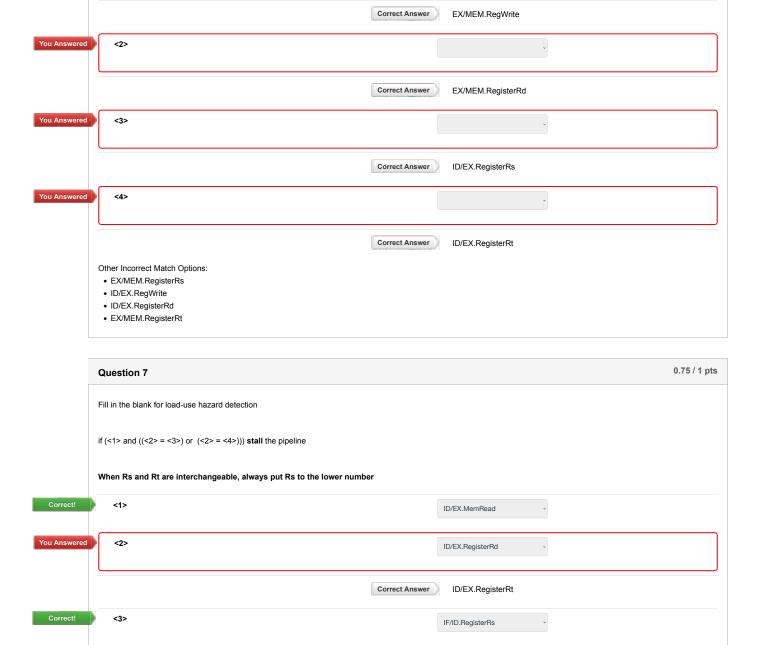
	Attempt	Time	Score
KEPT	Attempt 2	81 minutes	4.17 out of 7
LATEST	Attempt 3	1,096 minutes	2.42 out of 7
	Attempt 2	81 minutes	4.17 out of 7
	Attempt 1	95 minutes	3.92 out of 7

Score for this attempt: **2.42** out of 7 Submitted Sep 12 at 1:49pm This attempt took 1,096 minutes.

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	Question 1	0.67 / 1 pts
	[MULTI-SELECT] Select all that needs to be saved in the MEM/WB pipeline state register.	
	☐ Men/Write control signali	
Correct!	RegWrite control signal	
Correct Answer	☐ MemToReg control signal	
	RegCat control signal	
Correct!	☑ Destination register address	
	Source register address	
Unanswered	Question 2	0 / 1 pts
	What hazard can these cause?	
You Answered	Multiplier requiring multiple cycles to execute	
	Correct Answer structural hazard	
You Answered	load \$1, 0(\$2) followed by add \$3, \$1, \$1	
	Correct Answer data hazard	
You Answered	branch	
	Correct Answer control hazard	
Unanswered	Question 3	0 / 1 pts
	Assume full forwarding support.	
	In what cycle this program fully finish?	

In what cycle this prog	ram fully finish?	•							
Only type in the number	er								
	0	1	2	3	4	5	6	7	
lw \$1, 0(\$2)	IF	ID	EX	MEM	WB				
add \$2, \$1, \$1		IF							
sw \$2, 0(\$3)									
lw \$4, 0(\$3)									
add \$1, \$4, \$1									

You Answered											
Correct Answers	0 (with margin: 0) 10 (with margin: 0)										
	0 (with margin: 0) 0 (with margin: 0)										
	Question 4										0 / 1 pts
	Assume NO forwarding support this processor detects a hazard and then stall necessary cycles to resolve the stalls.										
	In what cycle this program fully finish?  Only type in the number										
	Only type in the number	0	1	2	3	4	5	6	7		
	lw \$1, 0(\$2)	IF	ID	EX	MEM	WB	3		,		
	add \$2, \$1, \$1		IF								
	sw \$2, 0(\$3)										
	lw \$4, 0(\$3)										
	add \$1, \$4, \$1										
You Answered	16										
Correct Answers	0 (with margin: 0)										
50110017111011011	0 (with margin: 0)										
	14 (with margin: 0) 0 (with margin: 0)										
	Question 5										1 / 1 pts
	Question 5 1/1 pts										
	Assume full forwarding support.										
	In what cycle this program full	y finish?									
	Only type in the number		1				1	-			
		0	1	2	3	4	5	6	7		
	lw \$1, 0(\$2)	IF	ID	EX	MEM	WB					
	lw \$2, 0(\$1)		IF								
	add \$3, \$2, \$4										
Correct!	8										
Correct Answers	0 (with margin: 0)										
	0 (with margin: 0)										
	8 (with margin: 0) 0 (with margin: 0)										
Unanswered											0 / 1 pts
Onanswered	Question 6										071 pts
	Fill in the blank for the EX/ME	M forward	unit pseu	do code							
	if (<1> and (<2>!= 0) and (<2> = <3>)) ForwardA = 10										
	if (<1> and (<2>!= 0) and (<2> = <4>)) ForwardB = 10										
	When Rs and Rt are intercha	angeable,	always p	ut Rs to	the lower ni	umber					
You Answered	<1>										



IF/ID.RegisterRt

<4>

Other Incorrect Match Options:

ID/EX.RegWrite

IF/ID.RegWrite

IF/ID.RegisterRd

ID/EX.RegisterRd

IF/ID.MemRead

ID/EX.RegisterRs