Quiz 1: MIPS ISA and single-cycle processor

Due Sep 6 at 11:59pm **Points** 8 **Questions** 8 **Available** after Sep 1 at 1:20pm **Time Limit** None **Allowed Attempts** 3

Take the Quiz Again

Attempt History

	Attempt	Time	Score
LATEST	Attempt 1	61 minutes	6 out of 8

Score for this attempt: **6** out of 8
Submitted Sep 5 at 11:51am
This attempt took 61 minutes.

Question 1

0 / 1 pts

Below is the structure of the R-type instruction.

op (6 bits)	Rs (5 bits)	Rt (5 bits)	Rd (5 bits)	shamt (5 bits)	funct (6 bits)

What is the binary representation of: sub $t0, $s1, $s2

(op for sub is 0, funct for sub is 0x22, $t0 is register 8, $s0 is register 17, $s1 is register 18)

You Answered

- [x] 000000 01000 10010 10001 00000 100010
- [ ] [illegible]
- [ ] [illegible]

Correct Answer

- [ ] 000000 10001 10010 01000 00000 100010

Question 2

0 / 1 pts

What is the MIPS assembly equivalent of the following?
int A[10];

int b = A[3];

Assume that b is register $t0, and &A[0] is stored in $s0.

You Answered

- [x] lw $t0, 3($s0)
- [ ] [illegible]
- [ ] [illegible]

Correct Answer

- [ ] lw $t0, 12($s0)

Question 3

1 / 1 pts

What is the MIPS assembly equivalent of the following?
char A[10];

char b;

A[3] = b;

Assume that b is register $t0, and &A[0] is stored in $s0.

- [ ] [illegible]

Correct!

- [x] sb $t0, 3($s0)
- [ ] [illegible]
- [ ] [illegible]

Question 4

1 / 1 pts

What will the bne instruction's offset field hold?

bne $s0, $s1, L1

add $t0, $s1, $s2

addi $s1, $s1, 4

L1: ...

0x05 (6 bits)	16 (5 bits)	17 (5 bits)	**??????? (16 bits)**

Correct!

- 8
- 2
- 3
- 12

Question 5

1 / 1 pts

What will the bne instruction's offset field hold?

L1: lw $s2, 4($s1)

add $t0, $s1, $s2

addi $s1, $s1, 4

bne $s0, $s1, L1

...

0x05 (6 bits)	16 (5 bits)	17 (5 bits)	**??????? (16 bits)**

Correct!

- -16
- -4
- -3
- -12

Question 6

1 / 1 pts

What C code is equivalent to the following?

slt $t0, $s0, $s1

beq $t0, $zero, L1

add $s0, $s0, $s1

L1: ...

Assume that variable name is the same with the register name ($s0 corresponds to s0 in C).

- if (s0 <= s1) s0 += s1
- if (s0 >= s1) s0 += s1

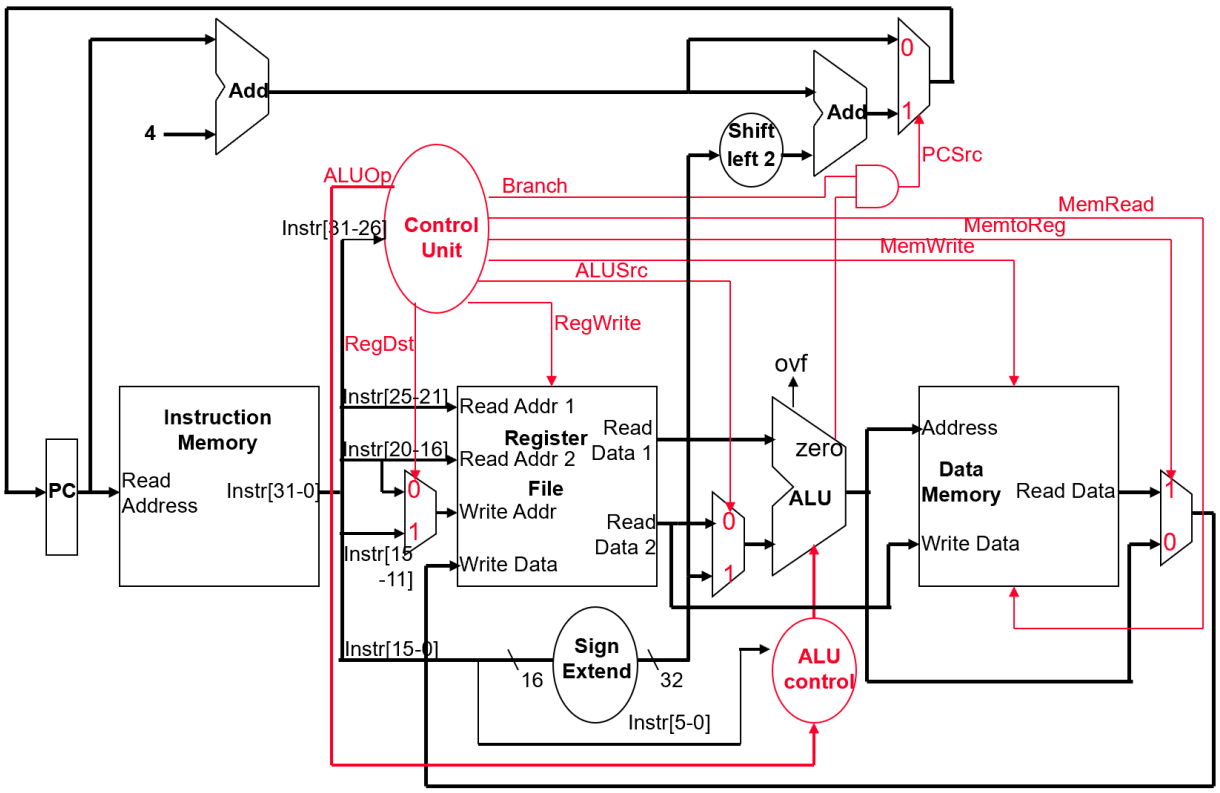
Correct!

- if (s0 < s1) s0 += s1
- if (s0 > s1) s0 += s1

Question 7

1 / 1 pts

Single Cycle Datapath with Control Unit



When running an R-type instruction, the control signals would be:

RegDst = 1

RegWrite = 1

ALUSrc = 0

MemWrite = 0

MemToReg = 0

Branch = 0

Answer 1:

Correct! 1

Answer 2:

Correct! 1

Answer 3:

Correct! 0

Answer 4:

Correct! 0

Answer 5:

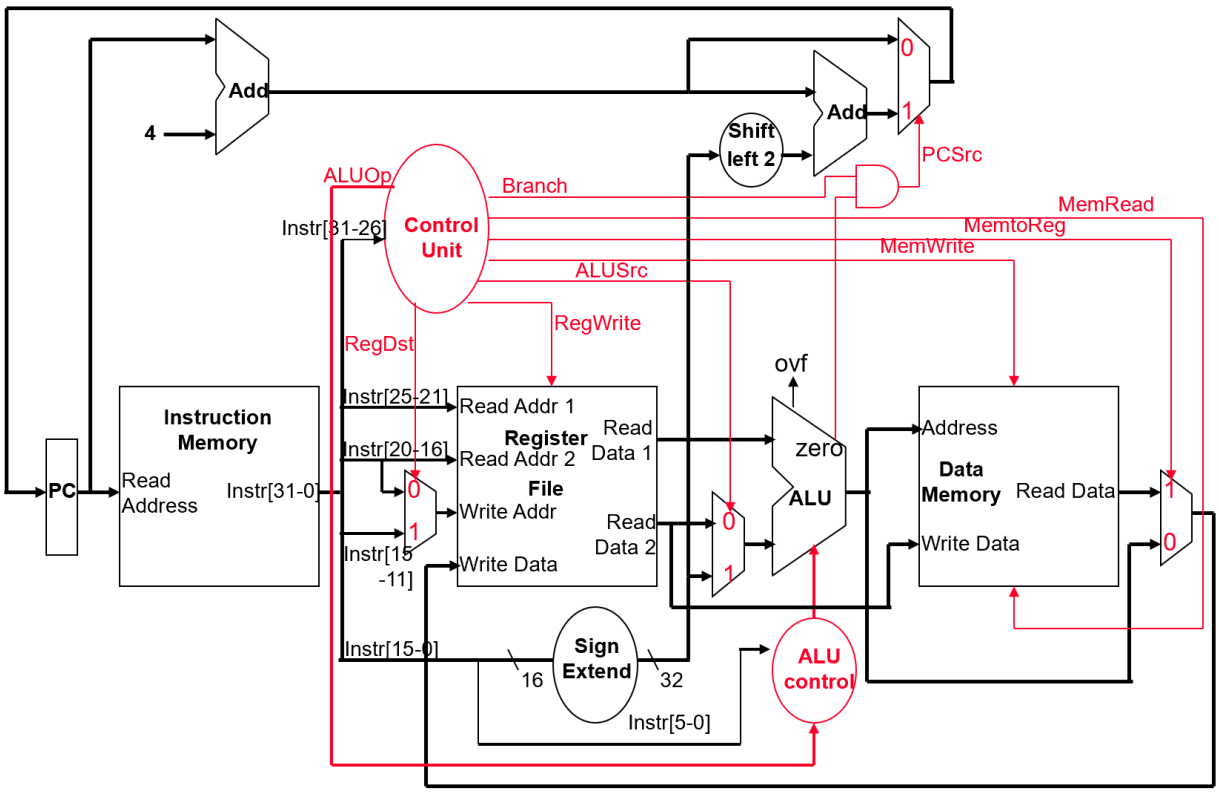
Correct! 0

Answer 6:

Correct! 0

Question 8 1 / 1 pts

Single Cycle Datapath with Control Unit



When running a LOAD instruction, the control signals would be:

RegDst = 0

RegWrite = 1

ALUSrc = 1

MemWrite = 0

MemToReg = 1

Branch = 0

Answer 1:

Correct! 0

Answer 2:

Correct! 1

Answer 3:

Correct! 1

Answer 4:

Correct! 0

Answer 5:

Correct! 1

Answer 6:

Correct! 0

Quiz Score: **6** out of 8