These are questions you can solve to prepare for the exam. Note that these are not in the exact same form of what will be given during the exam (in the exam, there will be visuals and it would give you a cleaner picture on what you need to do). However, you should be able to answer these questions, and if so, it will help the exam greatly. Also, you should also know other concepts taught in class as well, as concepts not covered in this practice exam can, and will, be in the exam.

Q1. Assume you have the following MIPS instructions.

L: lw $2, 0($1)

add $2, $2, $3

sw $2, 0($1)

addi $1, $1, -4

bne $1, $0, L

Q1-1. Unroll the loop by 2. Assume that the loop can be perfectly unrolled.

L: lw $2, 0($1)

lw $4, -4($1)

add $2, $2, $3

add $4, $4, $3

sw $2, 0($1)

sw $4, -4($1)

addi $1, $1, -8

bne $1, $0, L

Q1-2. Try scheduling it into a 2-issue VLIW. Assume the first instruction should be ALU/branch instruction and the second should be load/store.

L: nop	lw $2, 0($1)
addi $1, $1, -8	lw $4, -4($1)
add $2, $2, $3	nop
add $4, $4, $3	sw $2, 8($1)
bne $1, $0, L	sw $4, 4($1)

Q2. Assume you have the following MIPS instructions.

add $1, $2, $3

add $4, $1, $2

mul $4, $2, $5

sub $1, $1, $4

Q2-1. Assume a Tomasulo's machine without ROB, that has 3 reservation station slots, RS1, RS2, and RS3 for add/sub, and RS4, RS5, RS6 for mul/div. Initially, assume the register files hold $1=1, $2=2, $3=3, $4=4, $5=5. If you issue all the four instructions without dispatching/executing any, what will be the state of the RAT and the reservation station?

Reservation station

RS1	add, 2, 3
RS2	add, RS1, 2
RS3	sub, RS1, RS4
RS4	mul, 2, 5
RS5	
RS6	

RAT

$1	RS3
$2	
$3	
$4	RS4

Q2-2. Describe step-by-step how the RAT, register files, and the reservation station will change when each instruction is dispatched. When you have to choose which instruction to dispatch among multiple instructions, choose the one with the lowest RS number.

1. RS1, RS4 dispatched
    a. RAT: $4 gets released
    b. Register files: $4 is updated to 2*5=10

c. RS1, RS4 released

d. RS2 updated to add, 6, 2

e. RS3 updated to sub, 6, 10

2. RS2 dispatched

a. RAT: no update

b. Register files: no update

c. Reservation station: RS2 released

3. RS3 dispatched

a. RAT: $1 released

b. Register files: $1 updated to -4

c. Reservation station: RS3 released

Q2-3. Do Q2-1 again, but this time, assume you have an ROB.

ROB:

$1		
$4		
$4		
$1		

Reservation station

ROB1	add, 2, 3
ROB2	add, ROB1, 2
ROB4	sub, ROB1, ROB3
ROB3	mul, 2, 5

RAT

$1	ROB4
$2	

$3	
$4	ROB3

Q2-4. Do Q2-2 again, but this time, assume you have an ROB.

1. RS1, RS4 dispatched (still using RS1—4 to indicate which slot I am talking about)
    a. ROB: first entry gets 6 and marked done. Third entry gets 10 and marked done
    b. RS1, RS4 released
    c. RS2 updated to add, 6, 2
    d. RS3 updated to sub, 6, 10
2. RS2 dispatched
    a. ROB: second entry gets 8 and marked done.
    b. Reservation station: RS2 released
3. RS3 dispatched
    a. ROB: fourth entry gets -4 and marked done.
    b. Reservation station: RS3 released

Q2-5. Describe step-by-step how the RAT, register files, and the ROB will change when each instruction is committed, from Q2-4.

1. ROB1 committed
    a. ROB1 released
    b. Register file $1 becomes 6
2. ROB2 committed
    a. ROB2 released
    b. Register file $4 becomes 8
3. ROB3 committed
    a. ROB3 released
    b. Register file $4 becomes 10
4. ROB4 committed
    a. ROB4 released
    b. Register file $1 becomes -4

Q3. If a 64KB direct-mapped cache has 8 words per block, explain how many bits should be for each field (tag, index, block offset, and byte offset). Also, how many bits do we need to implement the cache?

Byte offset: 2

Block offset: 3

Index: 11

Tag: 16

2048*(1 + 16 + 32*8) = 546Kb needed to implement the cache

Q4. Assume a direct-mapped cache with 4 blocks, with 2 words per block. Simulate what will happen if we access Mem(0), Mem(1), Mem(4), Mem(16), Mem(5). Only the lower two bits of the tag needs to be shown.

1. Miss

Valid?	Tag	Word 1	Word 0
1	00	Mem(1)	Mem(0)

2. Hit
3. Miss

Valid?	Tag	Word 1	Word 0
1	00	Mem(1)	Mem(0)
1	00	Mem(5)	Mem(4)

4. Miss

Valid?	Tag	Word 1	Word 0
1	10	Mem(17)	Mem(16)
1	00	Mem(5)	Mem(4)

5. Hit

Q5. Assume a 2-way set-associative with 4 sets, with one word per block. Simulate what will happen if we access Mem(0), Mem(1), Mem(4), Mem(0), Mem(8), Mem(5). Only the lower two bits of the tag needs to be shown.

1. Miss

Way 0				Way 1		
Valid?	Tag	Word		Valid?	Tag	Word
1	00	Mem(0)				

2. Miss

Way 0				Way 1		
Valid?	Tag	Word		Valid?	Tag	Word
1	00	Mem(0)				
1	00	Mem(1)				

3. Miss

Way 0				Way 1		
Valid?	Tag	Word		Valid?	Tag	Word
1	00	Mem(0)		1	01	Mem(4)
1	00	Mem(1)				

4. Hit

5. Miss

Way 0				Way 1		
Valid?	Tag	Word		Valid?	Tag	Word
1	00	Mem(0)		1	10	Mem(8)
1	00	Mem(1)				

6. Miss

Way 0				Way 1		
Valid?	Tag	Word		Valid?	Tag	Word
1	00	Mem(0)		1	10	Mem(8)
1	00	Mem(1)		1	01	Mem(5)