Analysis and Design of Tuning-less mm-Wave Injection-Locked Frequency Dividers with Wide Locking Range Using 8th-Order Transformer-Based Resonator in 40 nm CMOS

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***Abstract*—Three tuning-less ultra-wide locking range (LR) transformer-based millimeter-wave (mm-wave) injection-locked frequency dividers (ILFDs) are presented. An 8th-order transformer-based resonator is proposed to improve the LR without an extra tuning mechanism or chip area. The operation principle of high-order transformer-based resonator in ILFDs based on the impedance diagram is analyzed. By comparing different high-order transformer-based resonators, the proposed resonator is the best option for the ultra-wide LR ILFD design. Also, the design considerations and trade-offs of the implemented resonator are discussed. Furthermore, an inductive gain peaking technique is adopted to ensure start-up conditions and achieve low power consumption. Three ILFDs are designed and fabricated in 40 nm CMOS technology. The first chip exhibits a best-in-class LR of 104.5% from 28.8 to 91.9 GHz while consuming 5.8 mW with a 0.9 V power supply. The second chip achieves the best figure of merit (FoM) up to 26.6 GHz/mW and 79.6% from 31 to 72 GHz LR with a 0.5 V power supply. The third chip obtains an LR of 108.9% from 20 to 67.8 GHz while consuming 4.9 mW with a 0.9 V power supply. Furthermore, 6 dB phase noise differences of the three chips are achieved, which is close to the theoretical value.**

***Index Terms*—Frequency divider, high-order transformer-based resonator, injection-locked, injection-locked frequency divider (ILFD), locking range (LR), millimeter-wave, phase response, transformer.**

I. Introduction

In recent years, the surges in demand for mm-wave communications, such as multi-band fifth-generation (5G) mobile communications systems and 77 GHz automotive radar, have attracted significant attention [1], [2]. The spectrum of 5G is divided into multiple bands, and different countries have different licensed spectrum bands. For example, the Federal Communications Commission (FCC) of the United States has deployed multiple bands above 24 GHz for 5G mobile communications, including the 24 GHz (24.25–24.45/24.75–25.25 GHz), 37 GHz (37.6–38.6 GHz), 39 GHz (38.6–40 GHz), and 47 GHz (47.2–48.2 GHz) bands. In addition to the licensed bands, further unlicensed bands need to be developed [3]–[5]. Therefore, for mm-wave 5G communications, an ultra-wideband system is essential to support the multiple licensed and unlicensed bands simultaneously. To build wide-band mm-wave transceivers for 5G applications, the frequency synthesizers are the most critical blocks. However, the first-stage frequency divider in frequency synthesizers creates a bottleneck since it must operate in the mm-wave frequency bands and cover the multi-band VCOs.

For mm-wave wideband frequency dividers, current-mode-logic (CML) static dividers [6], [7], miller dividers [8], [9], and ILFDs [10]–[20] are the widely used solutions. CML dividers have the widest LR with a small chip area since no inductors are used. However, their operating frequency is typically below mm-wave frequency and suffers from high power consumption. On the other hand, miller dividers can operate at higher frequencies with lower power consumption but narrower LR than CML dividers. Whereas ILFDs are more suitable for mm-wave applications than the other two types due to their highest operation frequency and lowest power consumption. However, the conventional ILFDs suffer from a narrow LR because of the narrowband of the LC resonator, which is usually smaller than 20%.

Distributed *LC*-tanks have been reported to increase the LR of ILFDs by minimizing the parasitic capacitance [10], [11], but more inductors are required, which means a larger chip area is inevitable. Other ways to improve the LR are frequency tracking [12]–[14] and transformer distribution [15], [16], but the results are still less than 40%. More successfully, the inductive peaking and forward-body-bias techniques have been applied to enhance the LR, with results reaching up to 90.9% [17]. Further, a 4th-order transformer-based resonator has achieved an LR of 62.7% with only 1.2 mW power consumption [18]. And a 6th-order transformer-based resonator

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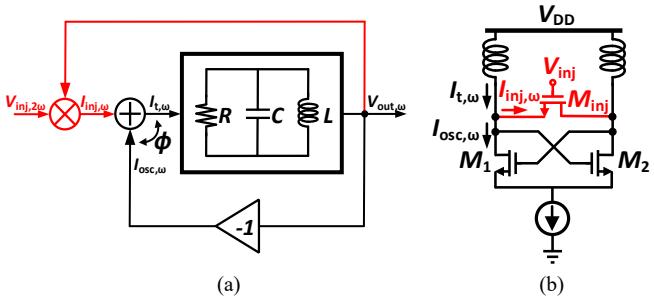
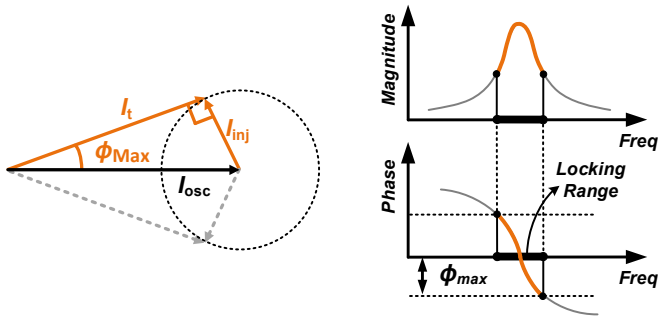


(a) (b)

Fig. 1. Conventional ILFD. (a) behavior model. (b) Circuit with LC-tank.



(a) (b)

Fig. 2. Conventional ILFD. (a) Phasor diagram. (b) Phase response of the resonator.

demonstrates a LR of 29.3 GHz from 19 GHz to 48.3 GHz, satisfying most applications for different nations' 5G standards [19]. Although extraordinary performance has been achieved, the LR in these solutions does not cover the licensed and unlicensed bands for 5G applications simultaneously. Additionally, there is still room to enlarge the LR, making it suitable for both multi-band 5G and 77 GHz automotive radar applications while using less power and a compact chip area.

In this paper, three tuning-less ILFDs using the proposed 8th-order transformer-based resonator achieve an ultra-wide LR with low power consumption and compact chip area. This paper expands the description in [20] to present a theoretical analysis of the high-order transformer-based resonator used in ILFDs. In addition, the design methods and considerations of the proposed 8th-order transformer-based resonator are explained in detail. Also, more measurement results are included. The inductive peaking and class-C type structure techniques are utilized to decrease power consumption. Another new chip is fabricated to demonstrate the performance of the class-C type structure used in mm-wave ILFD. From these approaches, the three ILFDs are successfully achieving an LR of 28.8 to 91.9 GHz, 31 to 72 GHz, and 20 to 67.8 GHz, respectively.

This paper is organized as follows. Section II discusses the limitation of a high-order transformer-based resonator. The proposed 8th-order transformer-based resonator and design details are also presented. Section III describes the circuit implementation of the proposed ILFDs, the power consumption reduction technique, and the robustness verification. Measurement results and conclusions are provided in Section IV and Section V, respectively.

II. Analysis of High-Order Transformer-Based Resonator in ILFDs

A. Locking Range Limitations

Fig. 1(a) and (b) show the behavior model and circuit of a conventional ILFD based on a simple *LC*-tank, respectively. The conventional *LC*-tank ILFD can be simply treated as an *LC*-oscillator with an injection device. The injection device M_{inj} acts as a mixer with an adder that mixes the injection signal V_{inj} and the output signal V_{out}, which generates I_{inj}. Then I_{inj} adds I_{osc}, which is generated from the cross-coupled pair, to get the total current I_t into the *LC*-tank. According to [21], the LR can be calculated as follow:

$$\omega_L \approx \frac{\omega_0}{2Q}\frac{I_{inj}}{I_{osc}}. \quad (1)$$

where ω_L represents the LR, ω_0 is the center operating frequency of the ILFD, and Q is the quality factor of the *LC*-tank. Usually, the operation frequency ω_0 is determined by the specification. Therefore, conventionally, we can increase I_{inj} or decrease Q and I_{osc} to improve the LR based on the equation. However, a large I_{inj} requires a large transistor size of M_{inj}, which increases both the input / output loadings and limits the maximum operating frequency. Also, a smaller I_{osc} or Q would face a lower output power and incur a risk of oscillation failure.

In addition to these traditional LR improvement methods based on (1), the phase response of the ILFD should be taken into consideration. The complete phasor diagram can be drawn by adding the current phasors I_{inj}, I_{osc}, and I_t, as shown in Fig. 2(a), giving an intuitive LR analysis and improvement method. According to the Barkhausen theorem, the phase shift of the circuit should be $2\pi n$ ($n \geq 1$), which means the phase difference between I_{osc} and I_t equals to the phase shift produced by the load resonator. The maximum phase shift Φ_{max} is achieved when I_T is tangent to the locus of I_{inj}, which can be expressed as [21]:

$$\Phi_{max} \approx \arcsin\frac{I_{inj}}{I_{osc}}. \quad (2)$$

Once the phase shift of the load resonator exceeds Φ_{max}, the Barkhausen theorem cannot be satisfied, and the ILFD will fail to oscillate. Therefore, the LR can be defined by the frequency range corresponding to the phase response curve of the resonator between the Φ_{max} and $-\Phi_{max}$, as shown in Fig. 3(b).

According to (2), Φ_{max} is fixed when the I_{inj} and I_{osc} of the circuit are determined. Therefore, based on the phase response characteristic, making the phase response of the resonator sufficiently flat and having ripples within Φ_{max} over a wide frequency range can significantly enlarge the LR. Thus, we can use a high-order transformer-based resonator rather than an *LC*-type resonator to improve the LR.

B. Locking Range Improvement of High-Order Resonator

Compared with the conventional *LC*-type resonator, high-order transformer-based resonators are already used for LR improvement in ILFDs, injection-locked frequency multipliers (ILFMs), and injection-locked oscillators [18]–[20], [22]–[26]. In [18] and [22], 4th-order transformer-based resonators were used to show a phase ripple around the 0° and achieve a good LR. In [19] and [20], the 6th-order transformer-based resonator and 8th-order transformer-based resonator were proposed to further flatten the phase response and show more phase ripples

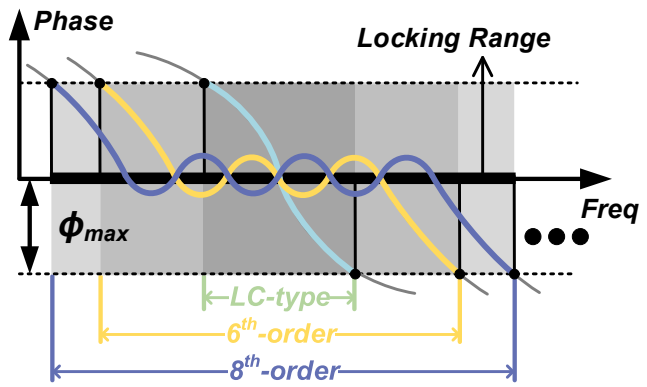


Fig. 3. Phase response of the *LC*-type resonator, the 6th-order transformer-based resonator, and the 8th-order transformer-based resonator.

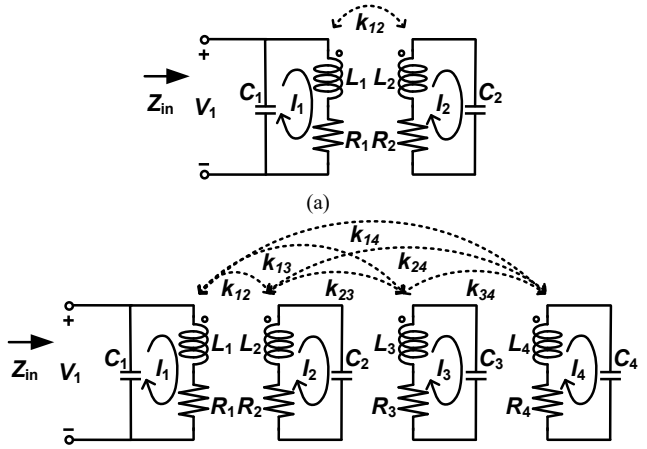


Fig. 4. Simplified equivalent model. (a) The 4th-order transformer-based resonator. (b) The 8th-order transformer-based resonator.

within Φ_{max} over a wide frequency range, which demonstrated an excellent LR performance.

Ideally, higher-order transformer-based resonator results in more phase ripples around 0°, corresponding to wider LR, as shown in Fig. 3. The phase ripple of the 8th-order resonator significantly improves the LR compared with the *LC*-tank and 6th-order resonator, which indicates that potentially it is a better solution for ILFDs. However, can we increase the order of the resonator to an even higher-order to achieve an even wider LR? Is there a limitation here? Which order is the best option for ILFD LR improvement design?

It is better to use a 4th-order transformer-based resonator to understand the trade-offs in the ILFD design. Fig. 4(a) shows the simplified equivalent model of the 4th-order transformer-based resonator. Because the phase noise of the ILFD is followed by the phase noise of the injection signal when working in the locking state [21], we only add the resistive components in series with the inductors to account for the loss of the network. The Q of the inductors can be $Q_{L1} = \omega L_1 / R_1$, and $Q_{L2} = \omega L_2 / R_2$. Since the tank-$Q$ will not affect the oscillation frequency, to simplify this analysis, the input tank impedance Z_{in} (also called Z_{11}) can be estimated by assuming R_1=R_2=0, which is expressed as [27]:

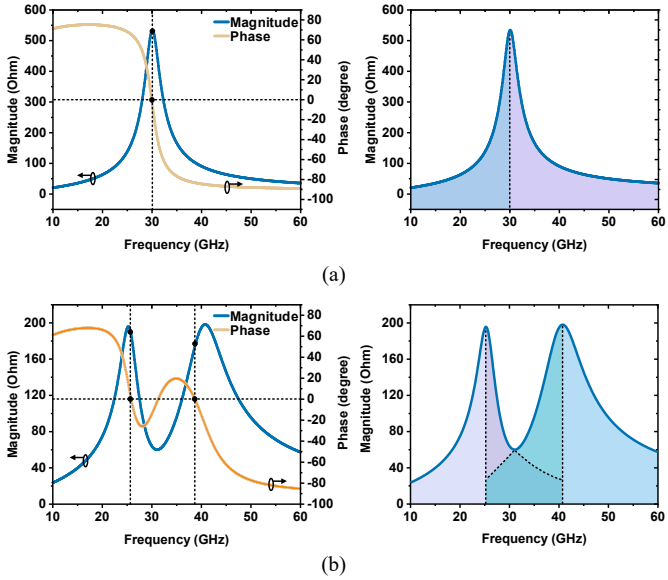


Fig. 5. The effect of reactance in magnitude and phase response. (a) The *LC*-type resonator. (b)The 4th-order transformer-based resonator.

$$Z_{11} \approx \frac{j\omega\omega_1^2 L_1[(1-k^2)\omega^2 - \omega_2^2]}{-\omega_1^2\omega_2^2 + \omega^2(\omega_1^2+\omega_2^2) - \omega^4(1-k^2)}. \quad (3)$$

where the self-oscillation frequencies $\omega_1^2 = 1/L_1C_1$, and $\omega_2^2 = 1/L_2C_2$. And the two resonant frequencies of the transformer are:

$$\omega_{H/L}^2 = \frac{\omega_1^2 + \omega_2^2 \pm \sqrt{\left(\omega_1^2 - \omega_2^2\right)^2 + 4k^2\omega_1^2\omega_2^2}}{2(1-k^2)}. \quad (4)$$

For an *LC*-tank, as shown in Fig. 5(a), at the peak resonant frequency, the inductive reactance of the inductor is equal to the capacitive reactance of the capacitor, which means $X_L = \omega L = X_C = 1 / \omega C$. At the peak resonant frequency, the magnitude of Z_{11} becomes maximum, and the phase of Z_{11} becomes 0°. However, for a 4th-order transformer-based resonator, the simulation result shows that the frequencies that correspond to the peak magnitude and the 0°phase are not the same, as shown in Fig. 5(b).

Intuitively, for a 4th-order transformer-based resonator, at the peak resonant frequencies, $X_{L1} \neq X_{C1}$ and $X_{L2} \neq X_{C2}$. The inductive reactance X_{L2} of L_2 has to compensate for two capacitive reactances: part of X_{C1} and the whole X_{C2} of C_1 and C_2, respectively. Therefore, at the first peak resonant frequency, $X_{L1} > X_{C1}$, and at the last peak resonant frequency, $X_{L2} < X_{C2}$, as shown in Fig. 5(b).

Theoretically, from (3), the real part and the imaginary part of the tank impedance can be derived as:

$$Real = 0. \quad (5)$$

$$Imag \approx \frac{(1-k^2)\omega^3 + \omega_2^2\omega}{(k^2-1)\omega^4 C_1 + (\omega_1^2 + \omega_2^2 - \omega_1^2\omega_2^2)\omega^2}. \quad (6)$$

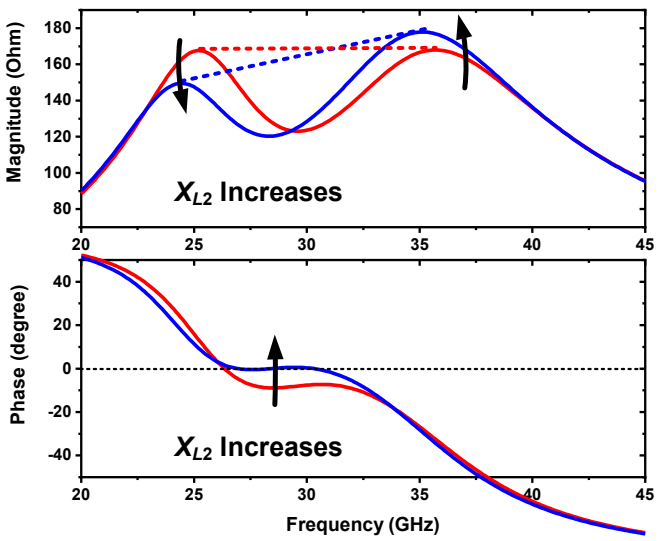


Fig. 6. Simulation results on the impedance of the resonator with different inductive reactance X_{L2}.

assuming the imaginary part of the tank impedance is equal to zero, the frequencies of $X_{L1} = X_{C1}$ and $X_{L2} = X_{C2}$ can be calculated as:

$$\omega_{1/2}^2 = \pm\frac{2\omega_2^2}{(k^2-1)}. \quad (7)$$

which is not equal to the two resonant frequencies $\omega_{H/L}$ of the transformer.

For the wide LR ILFD design, there are five design considerations.

1) Gain condition. According to the Barkhausen theorem, the loop gain of the ILFD must be above one to make the circuit oscillate normally. Therefore, the magnitude of the resonator must be large enough to sustain oscillation.
2) Balanced loading. To achieve the same loading for the circuit, the in-band magnitudes of the resonator should be almost the same.
3) Low-Q tank. The Q of each inductor in the resonator and the whole tank is designed to be a low value. The reason is that a high Q would introduce a large ripple for the phase response, which would be out of the upper and lower bounds of Φ_{max}, thus causes the in-band loss-of-lock phenomenon. Also, the magnitude difference between the peak and notch is large, which brings unbalanced loading [18]–[20].
4) Moderate k. Large k would bring a large ripple of the phase response and magnitude response, which would cause in-band loss-of-lock phenomenon and unbalanced loading. However, the LR is narrow with a small k. Therefore, a moderate k should be carefully chosen [18].
5) Phase ripples around 0°. To achieve a large LR, more phase ripples around 0° are better.

Based on the first four design considerations, the magnitude and phase response of a 4th-order transformer-based resonator can be obtained, as plotted by the red curves in Fig. 6. However, the phase ripples are below 0°, which results in a narrow LR. As discussed before, the inductive reactance X_{L2} of L_2 has to compensate for part of X_{C1} and the whole X_{C2}. If the inductive reactance X_{L2} is not large enough, the X_{C1} and X_{C2} could not be compensated, and the phase response would not be pulled back up to zero. If we increase the inductance of L_2 so as to increase X_{L2}, the phase response (the fifth design consideration) can be satisfied, as plotted by the blue curve in Fig. 6. However, the unbalanced magnitudes cause the unbalanced loading of the circuit, which cannot meet the second design consideration.

This theory can be expanded to the 8th-order transformer-based resonator. Fig. 4(b) shows the simplified equivalent model of the 8th-order transformer-based resonator. The input tank impedance Z_{11} can be estimated by solving the following matrix:

$$\begin{bmatrix} Z_1 & -j\omega M_{12} & -j\omega M_{13} & -j\omega M_{14} \\ -j\omega M_{12} & Z_2 & -j\omega M_{23} & -j\omega M_{24} \\ -j\omega M_{13} & -j\omega M_{23} & Z_3 & -j\omega M_{34} \\ -j\omega M_{14} & -j\omega M_{24} & -j\omega M_{34} & Z_4 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix} = \begin{bmatrix} V_1 \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (8)$$

where $M_{12} = k_{12}\sqrt{L_1L_2}$, $M_{13} = k_{13}\sqrt{L_1L_3}$, $M_{14} = k_{14}\sqrt{L_1L_4}$, $M_{23} = k_{23}\sqrt{L_2L_3}$, $M_{24} = k_{12}\sqrt{L_2L_4}$, and $M_{34} = k_{34}\sqrt{L_3L_4}$ are mutual inductances. k_{12}, k_{13}, k_{14}, k_{23}, k_{24} and k_{34} are the coupling factors between each inductor. For simplicity consideration, we assume $R_1 = R_2 = R_3 = R_4 = 0$ since the tank-Q will not affect the oscillation frequency. Also, the mutual inductances and capacitances will not destroy the oscillation characteristic, so that $M_{12} = M_{13} = M_{14} = M_{23} = M_{24} = M_{34} = M$ and $C_1 = C_2 = C_3 = C_4 = C$.Thus, the four inductor's own peak impedances are simplified as $Z_1 = j\omega L_1 + 1/(j\omega C)$, $Z_2 = j\omega L_2 + 1/(j\omega C)$, $Z_3 = j\omega L_3 + 1/(j\omega C)$, $Z_4 = j\omega L_4 + 1/(j\omega C)$. Additionally, letting $L_{1-4} = L_1L_2 +$

$$Z_{11} \approx \frac{j\omega C[1-\omega^2 C\sum_{i=2}^4 L_i + 3\,\omega^4C^2(M^2+L_2L_3+L_2L_4+L_3L_4) + \omega^6C^3(2M^3+M^2\sum_{i=2}^4 L_i+\sum_{i=2}^4 L_i)]}{\omega^2 C\sum_{i=2}^4 L_i - \omega^4C^2(6M^2+L_{1-4}) + \omega^6C^3(8M^3-3M^2\sum_{i=2}^4 L_i+L_{1-4}) + \omega^8C^4(3M^4-2M^3\sum_{i=2}^4 L_i+M^2L_{1-4}) - 1}. \quad (9)$$

$$\omega^8C^4(3M^4-2M^3\sum_{i=2}^4 L_i+M^2L_{1-4}) + \omega^6C^3(8M^3-3M^2\sum_{i=2}^4 L_i+L_{1-4}) - \omega^4C^2(6M^2+L_{1-4}) + \omega^2C\sum_{i=2}^4 L_i - 1 = 0. \quad (10)$$

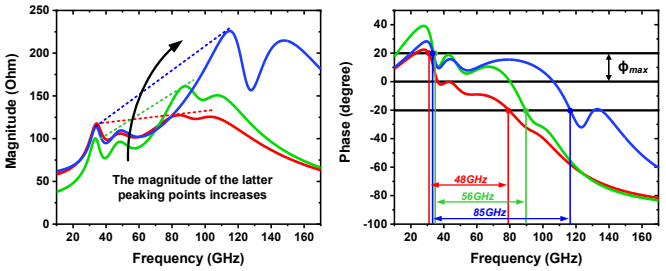
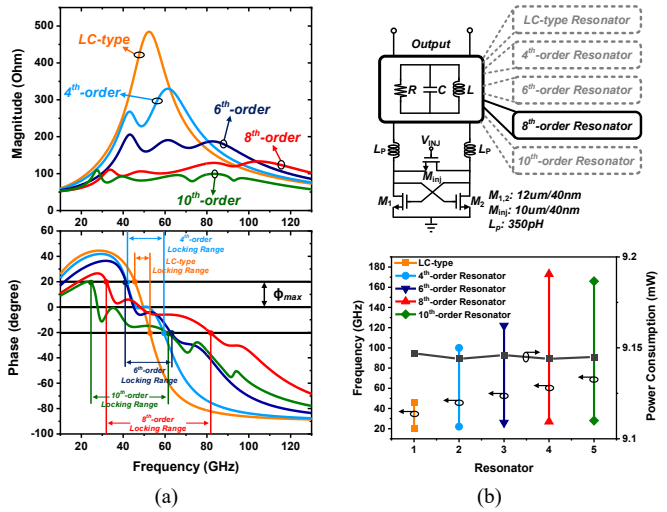


Fig. 7. The simulated phase response comparison of different magnitude slopes of the 8th-order resonator.



(a) (b)

Fig. 8. (a) The simulated impedance of the same total tank Q of five different resonators. (b) The schematic of the test circuit and the simulated locking range and power consumption comparison of the five resonators.

$L_1L_3 + L_1L_4 + L_2L_3 + L_2L_4 + L_3L_4$ to simplify the expression of the formula. Therefore, the input tank impedance Z_{11} of the 8th-order transformer-based resonator can be derived as given by (9), shown at the bottom of the page.

According to (9), the peak resonant frequencies appear when Z_{11} reaches the maximum value, that is, when the denominator reaches zero. By solving (10), eight roots can be obtained. However, for the physical system, ω has to be larger than zero. Therefore, the equation has four roots, implying four peak resonant frequencies in the 8th-order transformer-based resonator.

Ideally, four peak resonant frequencies correspond to seven zero-crossing points in the 8th-order resonator's phase response, as shown in Fig. 3. However, considering the gain condition, balanced loading, low-Q tank and moderate k value, the phase response of the 8th-order resonator declines rapidly, as plotted by the red curve in Fig. 7(a). Here we use the "peak points" to represent the resonant frequencies of the resonator. As discussed above, the inductive reactance of the latter peak points not only needs to compensate for their own capacitive reactance, but also needs to compensate for part of other peak points' capacitive reactance. Therefore, large inductances of the latter peak points are indispensable to compensate for the capacitances of the former peaks that can pull the phase response back up to zero. In other words, the magnitude of the four peaks should have a significant positive slope, as plotted by the green and blue curves in Fig. 7. This phenomenon brings a critical trade-off between the balanced loading and the flatten phase response around 0°. For an ILFD design, the balanced loading is essential to ensure a constant power consumption across the whole LR and generates balanced output power [25]. Although the LR of the blue curve is 1.8 times larger than that of the red curve, it introduces an extensively unbalanced loading for the circuit.

To find out the LR improvement limitation of the high-order transformer-based resonator, the simulated LR comparison diagram of five different resonators under the same total tank Q is illustrated in Fig. 8(a). The LC-type, 4th-order and 6th-order resonators has narrower LR compared to the proposed 8th-order resonator. For the same balanced loading considerations as for the 8th-order resonator, the phase response of the 10th-order resonator decreases faster since it is more difficult to compensate for the capacitive reactance. Therefore, the 8th-order resonator has the widest LR among all of them. Furthermore, as depicted in Fig. 8(b), a test circuit is designed to compare the LR of these five resonators with the same total tank Q under the same power consumption. Just by changing the resonator from the LC-type to 10th-order, the LR of the 8th-order resonator is 5.6 times, 1.9 times, 1.5 times and 1.1 times larger than the LC-type, 4th-order, 6th-order and 10th-order resonator, respectively, as plotted in Fig. 8(b). These simulation results further illustrate that the 8th-order resonator is the best option for the wide LR ILFD design.

C. *Proposed 8th-Order Transformer-Based Resonator*

The design of the 8th-order transformer-based resonator should take into account both LR performance and layout feasibility. Fig. 4(b) illustrates the simplified equivalent model of the transformer whose tank impedance Z_{11} is described by (9). Here, L_1, L_2, L_3 and L_4 are the inductances of each coil, C_1, C_2, C_3 and C_4 are the tuning capacitors of the transformer, R_1, R_2, R_3 and R_4 are the equivalent series resistors that represent the loss of the transformer, and k_{12}, k_{13}, k_{14}, k_{23}, k_{24} and k_{34} are the magnetic coupling coefficients between each coil, respectively. The target is to find the optimum eighteen values of L_1, L_2, L_3, L_4, C_1, C_2, C_3, C_4, R_1, R_2, R_3, R_4, k_{12}, k_{13}, k_{14}, k_{23}, k_{24} and k_{34}, then get the transformer's layout implementation. However, it is hard to design the transformer directly with eighteen variable parameters and complex tank impedance formula. Fortunately, the simplified equivalent model has sufficient accuracy to speed up the optimization and iteration.

First, the initial magnitude and phase response as the cornerstone of optimization should be set to roughly cover a large frequency range. It can be done by defining four different self-resonant frequencies of each coil with variable magnetic coupling coefficients and losses.

Next, these variables can be adjusted in the simulator through the controlled variable method to optimize the amplitude and phase response. Since the self-resonant frequency is defined by $\omega = 1/\sqrt{LC}$, when the inductance changes, the capacitance can be adjusted accordingly to maintain a fixed self-resonant frequency. Thus, the effect of capacitance can be out of consideration.

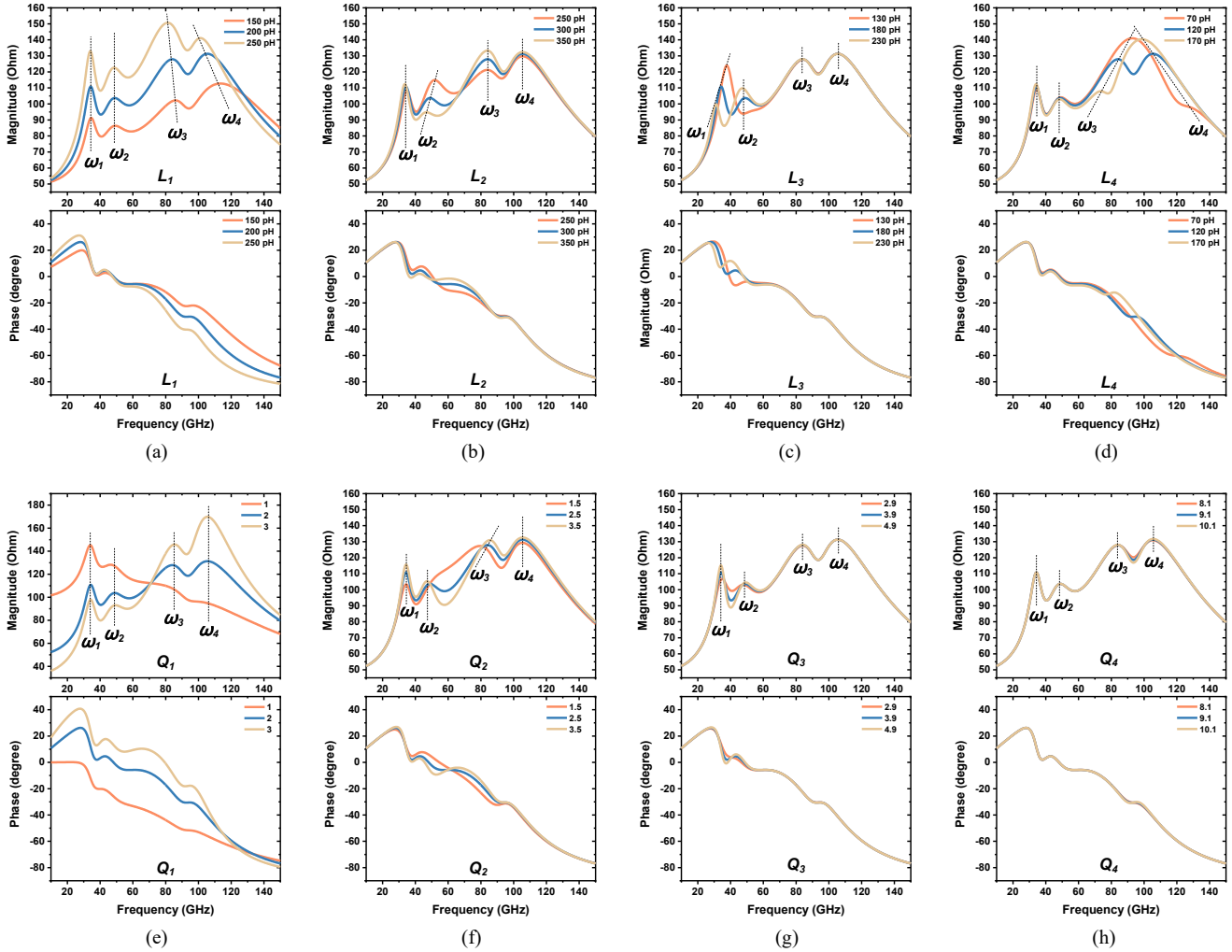


Fig. 9. Magnitude and phase response with different values of (a)L_1, (b)L_2, (c)L_3, (d)L_4, (e)Q_1, (f)Q_2, (g)Q_3, and (h)Q_4.

Fig. 9(a)(b)(c)(d) depict the effect of L_1, L_2, L_3 and L_4. By increasing L_1, the whole magnitudes of the resonator are enhanced, which can satisfy the gain condition easier. However, the peak frequencies ω_3 and ω_4 are reduced, making the phase response drop faster, which is not suitable for wide LR design. As shown in Fig. 9(b), L_2 only affects ω_2 and ω_3. Small L_2 has a more balanced magnitude but a fast phase response drop. However, large L_2 has a more flatten phase response, but extensive unbalanced magnitude. As shown in Fig. 9(c), L_3 only affects ω_1 and ω_2, and the effect on magnitude and phase response is opposite to L_2. As for the L_4, the positions of ω_1 and ω_2 keep unchanged. However, both small and large L_4 will bring a tremendous unbalanced magnitude in ω_3 and ω_4.

Fig. 9(e)(f)(g)(h) show the influence e of Q_1, Q_2, Q_3 and Q_4. As shown in Fig. 9(e), the peak frequencies of ω_1, ω_2, ω_3 and ω_4 are unchanged. With a small Q_1, the magnitudes of ω_1 and ω_2 are reduced, but the magnitudes of ω_3 and ω_4 are increased, which can pull the phase response back upon zero and achieve a more flatten phase response, by sacrificing extensive unbalanced loading. However, the influence of a large Q_1 is opposite to a small Q_1. The magnitudes of the peak frequencies are smaller and smaller from ω_3 to ω_4, and the phase response will decline rapidly so that narrow LR is induced. As shown in Fig. 9(f), Q_2 mainly affects the notch frequency between ω_2 and ω_3. Higher Q_2 corresponds to the lower magnitude of the notch frequency. Although a more rippled phase response can be obtained, the gain condition may not be satisfied due to a low magnitude of the notch frequency. As shown in Fig.9(g), Q_3 mainly affects the notch frequency between ω_1 and ω_2. The same effect as Q_2, higher Q_3 corresponds to the lower magnitude of the notch frequency, but the change rate is not as fast as Q_2. Also, it has the same problem with Q_2. As for Q_4, only the notch frequency between ω_3 and ω_4 are influenced with the same trend as Q_2 and Q_3, but the change rate is negligible, as shown in Fig. 9(h). Therefore, the value of Q_4 hardly destroys the characteristics of the resonator and can be selected according to the most favorable situation for the layout.

Fig. 10 illustrates the impacts of k_{12}, k_{13}, k_{14}, k_{23}, k_{24} and k_{34}. As depicted in Fig. 10(a)(b)(c), the effect and changing trends of k_{12}, k_{13}, and k_{14} are nearly the same, which is the smaller mutual inductance corresponds to the higher magnitude and the lower peak frequency. Therefore, the trade-off between balanced loading and flatten phase response around 0° appears again. The difference is that k_{12} mainly affects ω_3 and ω_4, k_{13} mainly affects ω_2 and ω_3, and k_{12} mainly affects ω_4, respectively. As shown in Fig. 10(d), when k_{23} increases, the

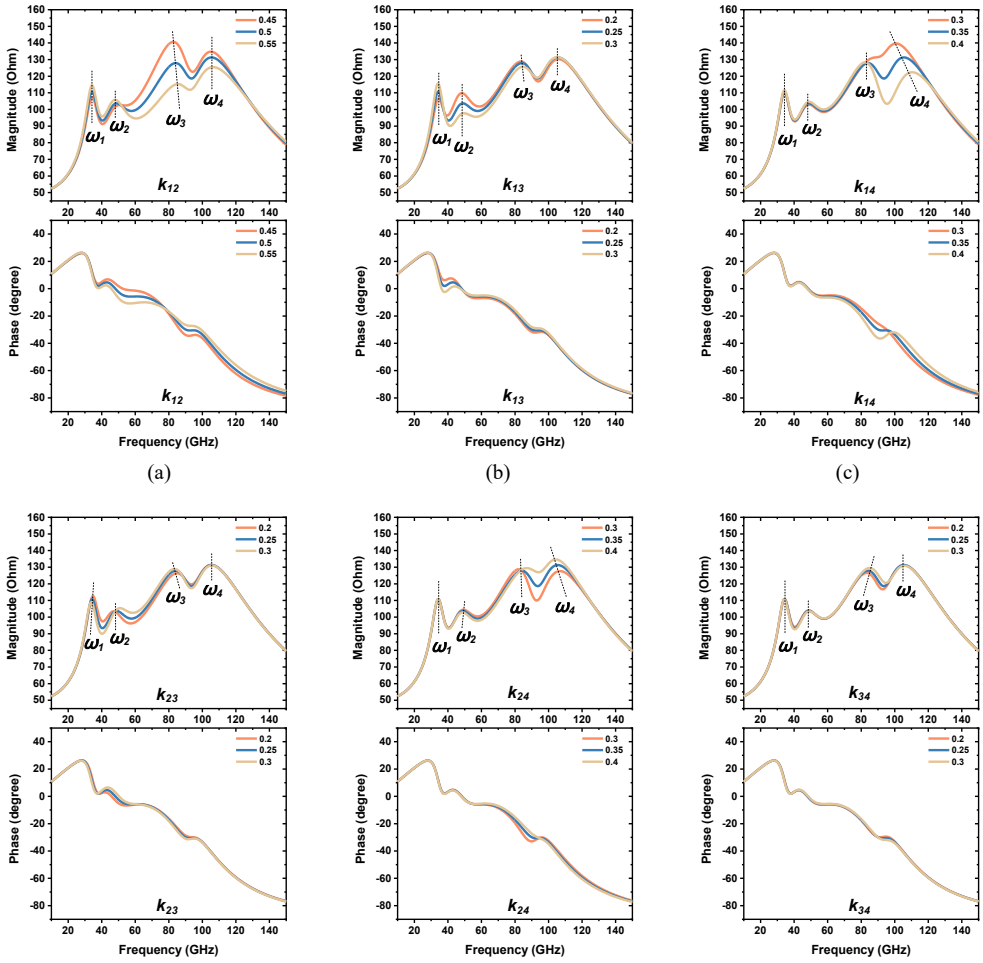


Fig. 10. Magnitude and phase response with different values of (a)k_{12}, (b)k_{13}, (c)k_{14}, (d)k_{23}, (e)k_{24}, and (f)k_{34}.

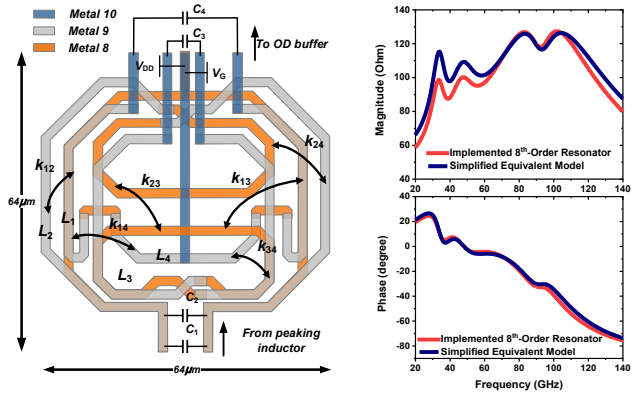


Fig. 11. (a) The implemented 8th-order transformer-based resonator. (b) The impedance simulation results of the model and the implemented resonator.

peak frequencies of ω_1, ω_2 and ω_3 are reduced, increased and reduced, respectively. Also, the magnitude of ω_1, ω_2 and ω_3 are reduced, increased and increased, respectively. Therefore, large k_{12} will bring a flatten phase response, but with high unbalanced loading and risk of start-up issue, since the magnitude of the notch frequency between ω_1 and ω_2 is low. As shown in Fig. 10(e), k_{24} has the same effect and changing trends with k_{23}, but with a faster change rate. As for k_{34}, larger k_{34} corresponds to higher magnitude and peak frequency of ω_3. However, the change rate is negligible, as shown in Fig. 10(f). Therefore, k_{34} can be selected according to the most favorable situation for the layout.

Finally, we can use the optimized eighteen parameters to guide the transformer layout implementation. Fig. 11(a) depicts the proposed 8th-order transformer-based resonator. In this work, lower metal layers, metal 9 and metal 8 with a narrow width and spacing, are used to design the resonator, which brings a very compact area for the resonator of only 64 μm × 64 μm. Using the design method shown above, we design the transformer with L_1 = 204 pH, L_2 = 300 pH, L_3 = 187 pH, L_4 = 122 pH, C_1 = 20fF, C_2 = 40fF, C_3 = 100fF, and C_4 = 30fF, k_{12} = 0.5, k_{13} = 0.25, k_{14} = 0.35, k_{23} = 0.25, k_{24} = 0.35, and k_{34} = 0.25. By optimizing the transformer, the Q of the four inductors are Q_1 = 2.0, Q_2 = 2.5, Q_3 = 3.9, and Q_4 = 9.1. The simulated resonator's magnitude and phase response comparison between the simplified equivalent model and the electromagnetic (EM) simulator is shown in Fig. 11(b). The few mismatches in the magnitude response between these two curves are because the layout cannot fully match all the parameters set into the simulator in pre-simulation. However, these few mismatches

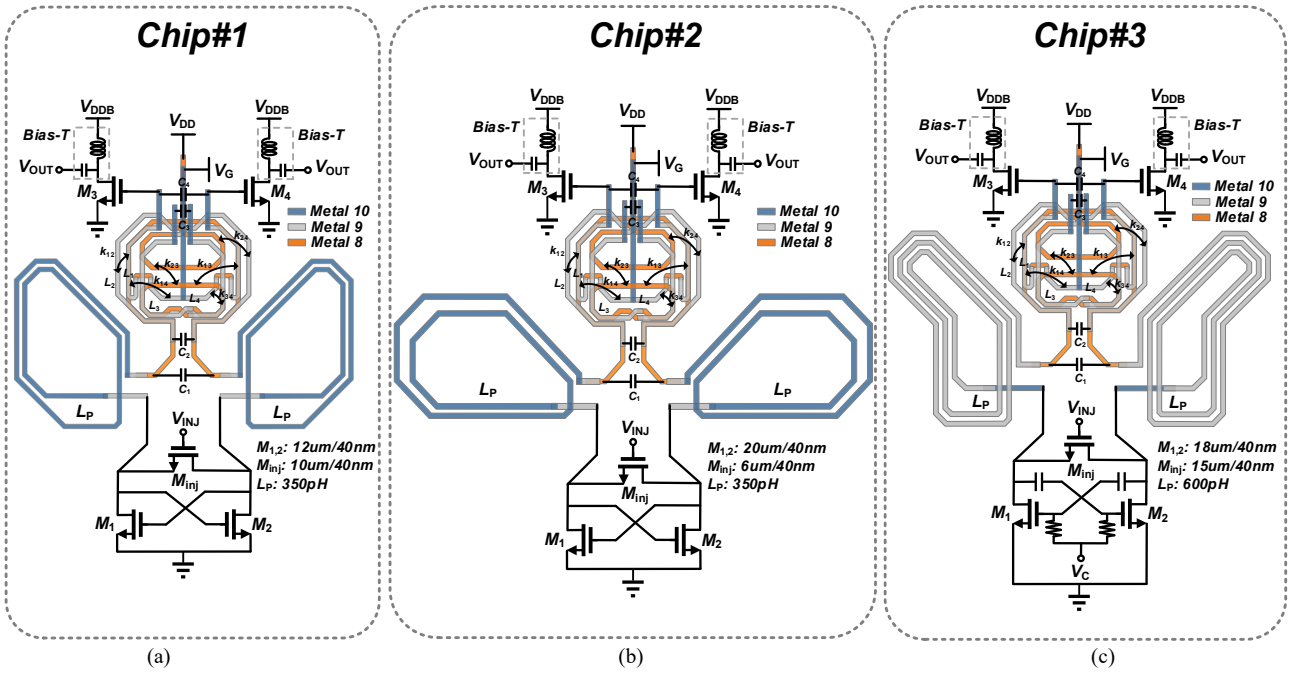


Fig. 12. Circuit implementations. (a) Chip#1, (b) Chip#2, (c) Chip#3.

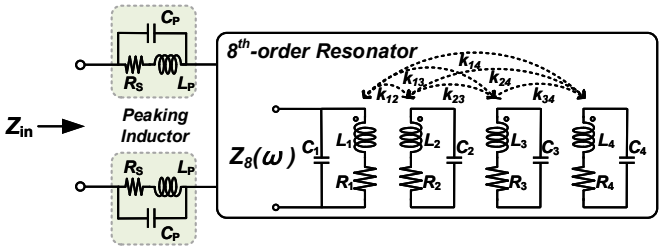


Fig. 13. Simplified equivalent model of the proposed resonator with peaking inductor.

can be accepted since no phase response degradation, which means the simplified equivalent model is accurate enough to guide the layout.

III. Circuit Implementations

A. Complete ILFD Topology

The schematics of three wide LR ILFDs are depicted in Fig. 12. Chip #1 is focused on an ultra-wide LR while consuming more power. Chip #2 aims at low power consumption, which achieves a high figure of merit (FoM), by sacrificing a little of the LR. Chip #3 introduces the class-C type structure to reduce power consumption further.

The 8th-order transformer-based resonator is proposed to enlarge the LR significantly. However, due to the low-Q characteristic of the 8th-order transformer-based resonator, the impedance magnitude is too low to satisfy the gain condition. In other words, a high bias current is needed to ensure start-up, which will bring high power consumption. This problem can be solved by inserting a peaking inductor (L_P) in series with the resonator [18], as shown in Fig. 13. The input impedance can be obtained as:

$$Z_{\text{in}} = \frac{L_P}{C_P R_S} \frac{1 - j\frac{R_S}{\omega_P L_P}}{1 + j\left(\frac{\omega_P L_P}{R_S} - \frac{1}{\omega_P C_P R_S}\right)} + Z_8(\omega). \tag{11}$$

where ω_P is the resonant frequency of the peaking inductor, which can be derived as:

$$\omega_P = \sqrt{\frac{1}{L_P C_P} - \frac{R_S^2}{L_P^2}}. \tag{12}$$

Treating the resonator and the peaking inductor as a whole block, the impedance magnitude of the resonator will be peaked, so that the gain condition and low power consumption can be achieved simultaneously. According to (11), the total input impedance Z_{in} is the combination of the resonator and the peaking inductor. Now that the impedance of the resonator is settled, then how the magnitude and phase responses of the total input impedance Z_{in} are affected by the peaking inductor? It is well known that the impedance magnitude will be peaked significantly at the resonant frequency when using a high-Q inductor rather than a low-Q inductor. Therefore, by using a high-Q peaking inductor whose resonant frequency ω_P is within the operation frequency band (in-band) of the ILFD, the magnitude at the resonant frequency is increased by around 3 times, as shown in Fig. 14(a). However, only the magnitude corresponding to a narrow frequency band around ω_P has been enhanced, also the phase response will drop rapidly after ω_P, which is not suitable for the wide-band application. When the ω_P is put far away from the operating frequency band of the ILFD (out-of-band), the phase response beyond 100 GHz can be pulled up upon zero due to the high magnitude caused by the peaking inductor, as shown in Fig. 14(b). However, a large

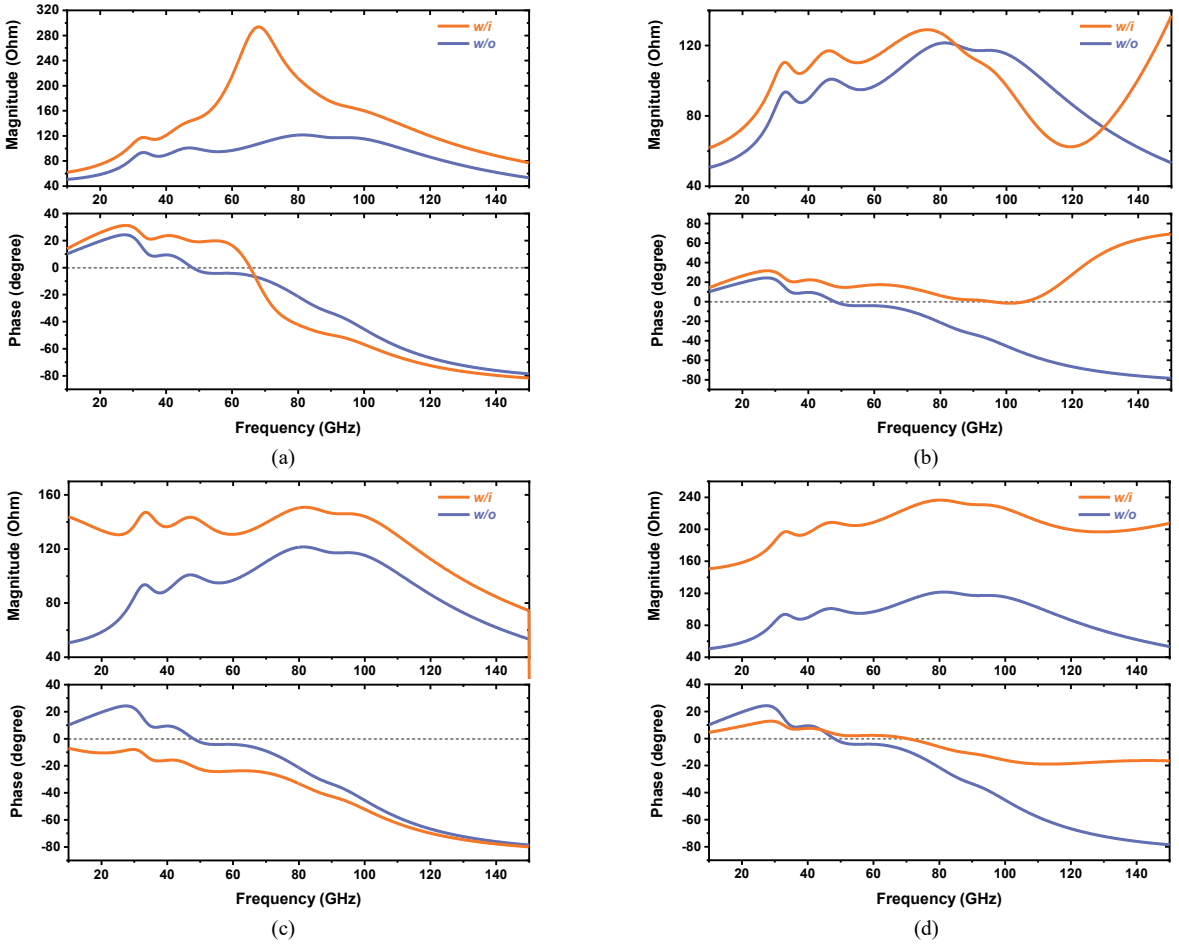


Fig. 14. The effect of the peaking inductor on the magnitude and phase response of the total input impedance. (a) High-Q, in-band, (b) High-Q, out-of-band, (c) Low-Q, in-band, (d) Low-Q, out-of-band.

magnitude loss and unbalanced loading at high frequency occurred, so that the balanced loading can not be satisfied.

Although the high-Q peaking inductor will enhance the magnitude tremendously, the narrow band characteristic is not a good option for the wide-band design. Therefore, a low-Q peaking inductor is adopted, as illustrated in Fig. 14(c)(d). When ω_P is put out-of-band, the whole in-band magnitude is enhanced by around 1.25 times. However, the phase response with the peaking inductor is lower than the one without the peaking inductor, which will cause an in-band loss-of-lock phenomenon. By setting ω_P out-of-band, as shown in Fig. 14(d), the whole in-band magnitude is improved by around 2 times. Also, the phase response at high frequency can be pulled up due to the large inductance of the peaking inductor as the last peak point to compensate the former peak point's capacitance. Therefore, by using the low-Q peaking inductor which ω_P is put out-of-band, not only the magnitude of the resonator is improved to satisfy the gain condition, but also the trade-off between the phase response and balanced loading which discussed in Section II can be solved.

To further reduce the power consumption, tail current sources of the three chips are removed to save power [18]. Since the phase noise of the ILFD mainly is decided by the injection signal and LR [28], the tail current source can be removed to release the voltage headroom of the circuit. Therefore, the voltage supply can be lower to reduce power consumption.

Also, wide LR and low power consumption can be achieved simultaneously by using a class-C oscillator [29]. For a class-C structure ILFD, the DC bias voltage V_C at the gate of the cross-coupled transistors is smaller than the threshold voltage, as shown in Fig. 12(c). Compared with the conventional direct cross-coupled class-B oscillator, the class-C oscillator has better power conversion efficiency [30]–[33]. However, the gain condition may be hard to achieve due to the low bias voltage of the cross-coupled pair. This can be solved by using a large transistor size to obtain a large g_m. Nevertheless, the transistor size cannot be too large to limit the highest operation frequency. Therefore, the transistor size of the cross-coupled pair should be optimized considering both gain condition and operation frequency. In addition to the parasitic capacitance from the transistor, the maximum output frequency is also limited by the large parasitic capacitance which contributed by the large biasing resistors (R_1, R_2) and DC blocking capacitors (C_5, C_6) at the gate of the cross-coupled pair, as shown in Fig. 12(c). Therefore, this structure may not be a good option for mm-wave applications.

Chip#1, chip#2 and chip#3 all use the implemented 8th-order transformer-based resonator, but with different values of

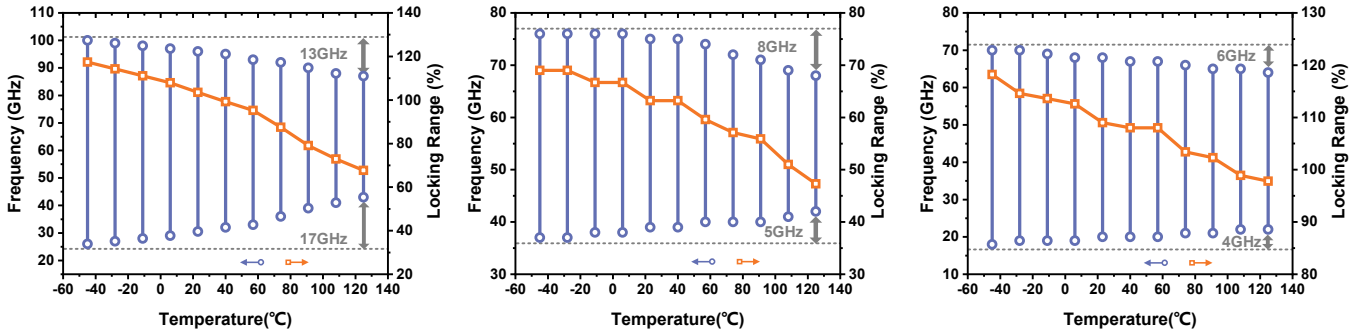


Fig. 15. Simulated ILFDs' LR over different temperatures at "TT" process corner under 0 dBm input power. (a) Chip#1 under 0.9 V power supply, (b) Chip#2 under 0.5 V power supply, (c) Chip#3 under 0.9 V power supply.

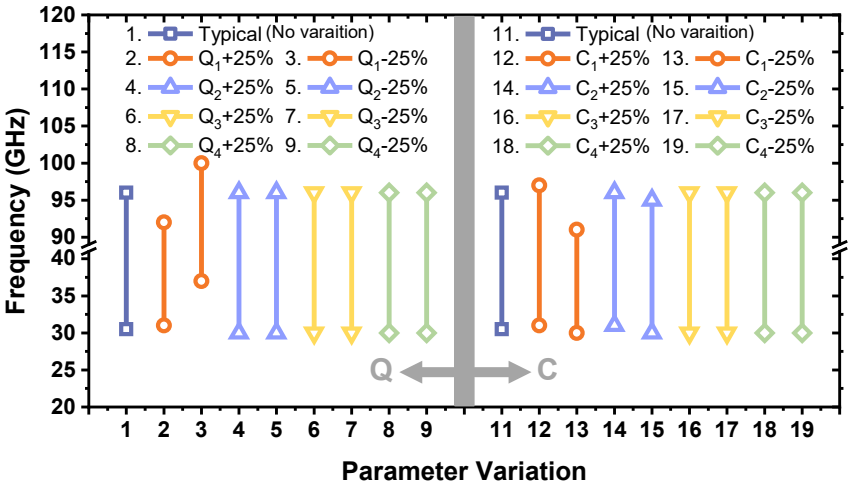


Fig. 16. Simulated Chip#1's LR variation caused by the capacitance and Q one-by-one at "TT" process corner and 27℃ under 0 dBm input power and 0.9 V power supply.

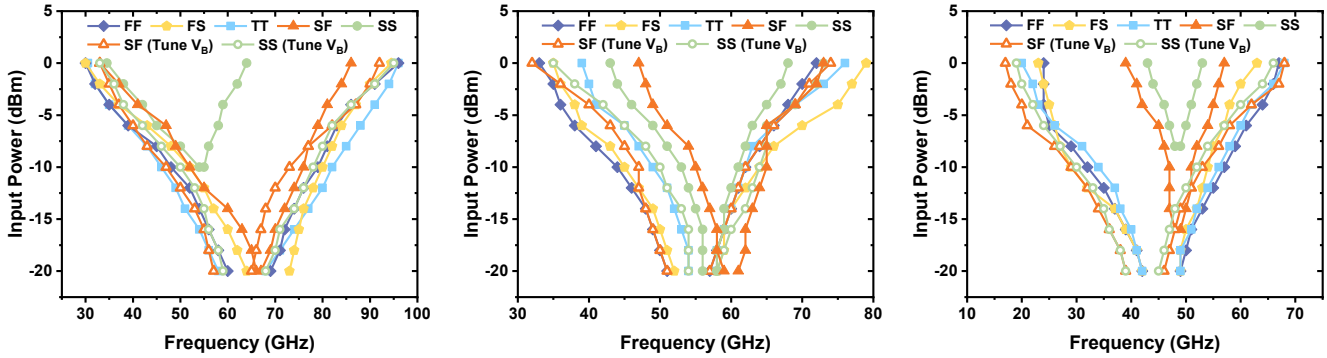
L_p and transistor sizes. Normally, the injection transistor M_{inj} can be biased in the subthreshold region and a large W/L transistor in the subthreshold region can increase the sensitivity without compromising g_m. However, the transistor size cannot be too large to limit the highest operation frequency. Therefore, considering the trade-off between the locking range and the highest operation frequency, the optimized transistor sizes are shown in Fig .12. Then the maximum phase shift Φ_{max} can be approximately estimated by simulating I_{inj} and I_{osc} in (2). In this design, the calculated Φ_{max} of chip#1, chip#2, and chip#3 are 25.3°, 22.3°, and 24.2°, respectively. Moreover, two open-drain output buffer transistors are connected to the fourth coil of the resonator and used to drive the 50 Ω loading of the instruments.

B. Robustness Verification

To verify the robustness of the proposed ILFDs, we perform circuit simulations over process and temperature variations. Fig. 15 illustrates the simulated ILFDs' LR over different temperatures (from −45℃ to 125℃) at "TT" (Typical-Typical) process corner under 0 dBm input power. The LR of the three ILFDs at −45℃ is wider than that at room temperature, and the LR decreases when the temperature moves high. Although at 125℃, the LR of Chip#1, Chip#2 and Chip#3 will drop 34.6%, 25.2%, and 10.3% compared to that at room temperature, it is still more than 44 GHz, 26 GHz and 42 GHz, respectively. This suggests the class-C structure is insensitive to temperature variation.

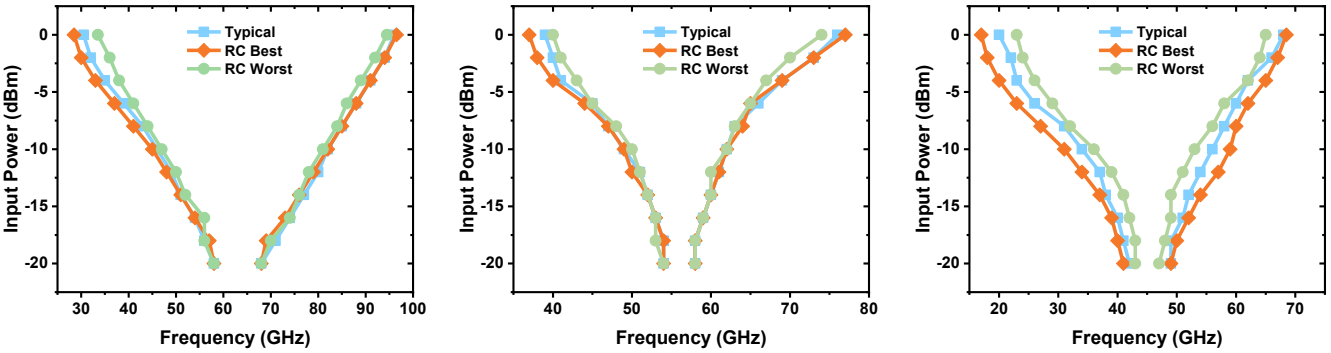
The 8th-order transformer-based resonator consists of 18 parameters. In the real chip, the capacitance and Q may have a 25% variation. So that we simulate the LR variation caused by the capacitance and Q one-by-one of Chip#1 at "TT" process corner and 27℃ under 0 dBm input power and 0.9V power supply, since the three chips use the same resonator, as shown in Fig. 16. It can be found that the variation of $Q_{2\text{-}4}$ and $C_{2\text{-}4}$ have nearly no impact on the LR. The largest LR variation occurred at Q_1 + 25%, however, the LR only drop 7.5% compared to the typical condition.

To evaluate the ILFDs robustness under different process corners, we simulate the three ILFDs at 27℃ against different process corners, as presented in Fig. 17. The LR of "SS" and "SF" process corners drop greatly, which is an abnormal performance. However, by tuning the bias voltage V_B of the injection transistor M_{inj}, both "SF" and "SC" process corners can be adjusted to close to the "TT" process corner and normal operation is recovered. The recovered widest and narrowest LR variations of chip#1, chip#2 and chip#3 are 10.6%, 15.9% and 21.6%, respectively. The chip#3 is the most sensitive to the



(a) (b) (c)

Fig. 17. Simulated ILFDs' LR over different process corners. (a) Chip#1 under 0.9 V power supply, (b) Chip#2 under 0.5 V power supply, (c) Chip#3 under 0.9 V power supply. Note that Fast-Fast (FF), Slow-Slow (SS), Typical-Typical (TT), Fast-NMOS-Slow-PMOS (FS) and Slow-NMOS-Fast-PMOS (SF).



(a) (b) (c)

Fig. 18. Simulated ILFDs' LR over different RC corners at "TT" process corner and 27℃ room temperature. (a) Chip#1 under 0.9 V power supply, (b) Chip#2 under 0.5 V power supply, (c) Chip#3 under 0.9 V power supply.

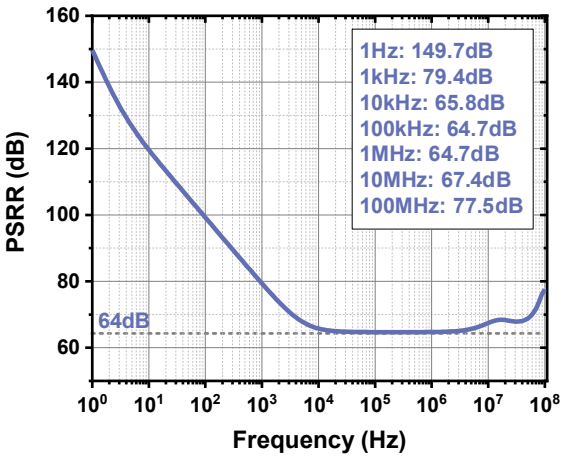


Fig. 19. Simulated PSRR of Chip#2 under 0.4 V power supply.

process corners, since the class-C structure of chip#3 uses two more DC blocking capacitors than chip#1 and chip#2. The worst LR of Chip#3 appears at FS corner, however, it still has 40 GHz LR.

In addition to the transistor's corner variation, there's a layout routing variation. Fig. 18 plots the simulated ILFDs' LR over RC best and RC worst corner at "TT" process corner and 27℃ room temperature. The LR variations between RC best and RC worst corners of chip#1, chip#2 and chip#3 are 11.0%, 15.0% and 18.4%, respectively.

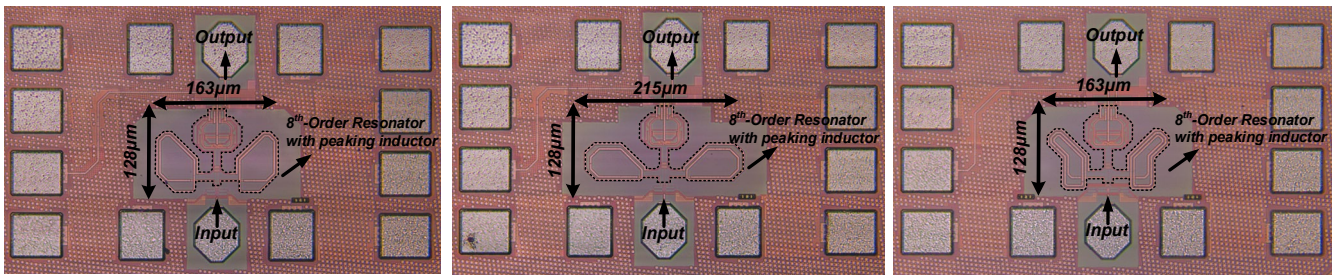
Moreover, the chip#2 is designed for low power supply applications which can be lowered to 0.4 V. Thus, the simulated PSRR of the chip#2 under 0.4 V power supply is estimated as plotted in Fig. 19. It achieves better than 64 dB PSRR up to 100 MHz at 0.4 V supply voltage, which is feasible in a real system.

IV. Measurement Results

A. Measurement Setups

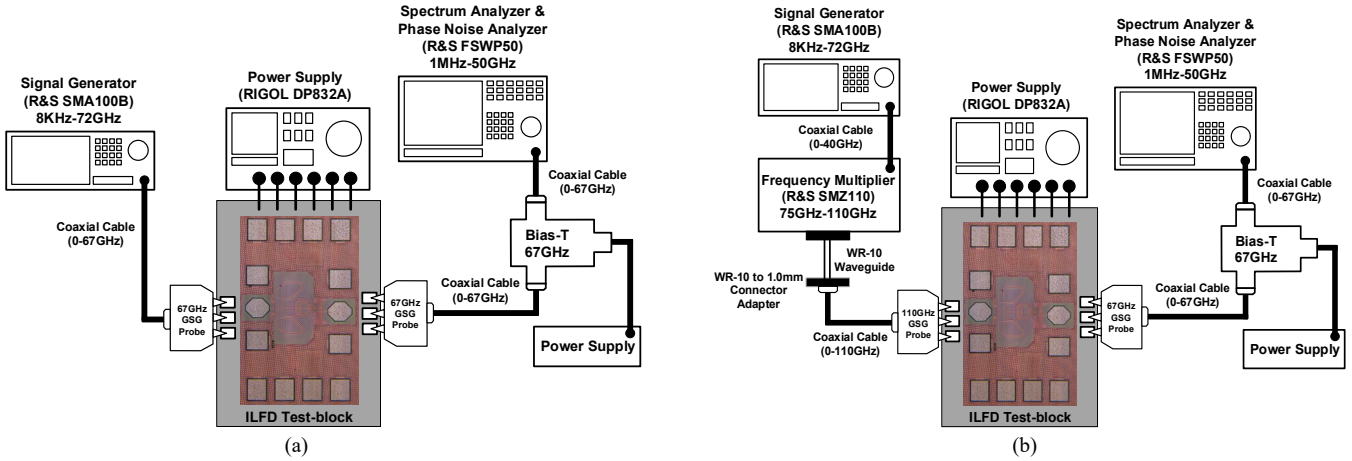
The three tuning-less transformer-based ILFDs are fabricated in 40 nm CMOS technology and tested on a probe station. Fig. 20 shows the chip microphotographs. The core area of each chip is 0.02mm^2, 0.027mm^2 and 0.02mm^2, respectively.

Fig. 21 shows the measurement setups of the three ILFDs. Due to the limited bandwidth of the testing equipment, two different setups are used to cover the whole frequency range. As shown in Fig. 21(a), the input signal below 72 GHz is generated from an SMA100B R&S signal generator, and a GSG probe is used for signal injection. The insertion loss of the coaxial cable and the GSG probe is around 10 dB, and it has been de-embedded. As shown in Fig. 21(b), the input signal



(a) (b) (c)

Fig. 20. Chip microphotographs: (a) Chip#1, (b) Chip#2, (c) Chip#3.



(a) (b)

Fig. 21. Measurement setups. (a) For input frequencies below 72 GHz. (b) For input frequencies from 75 GHz to 110 GHz.

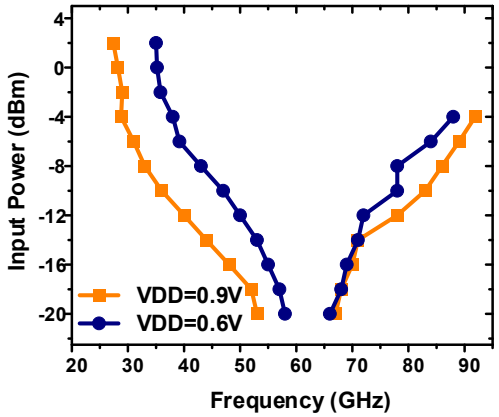


Fig. 22. Measured input sensitivity curves of chip#1 under both 0.9 V and 0.6-V power supplies.

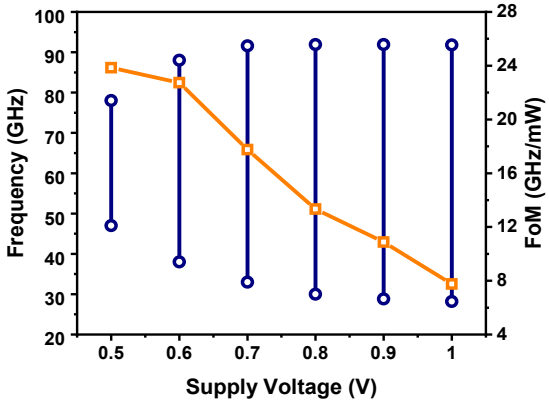
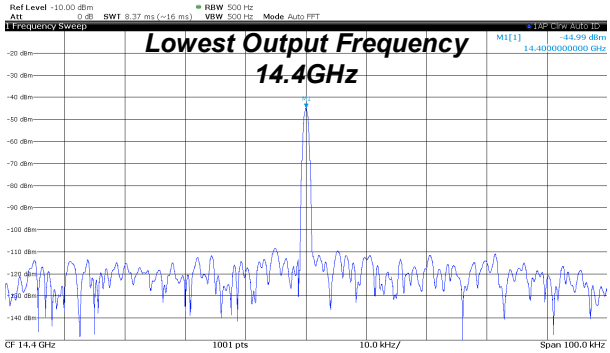


Fig. 23. Measured LR and FoM of chip#1 under different power supplies.

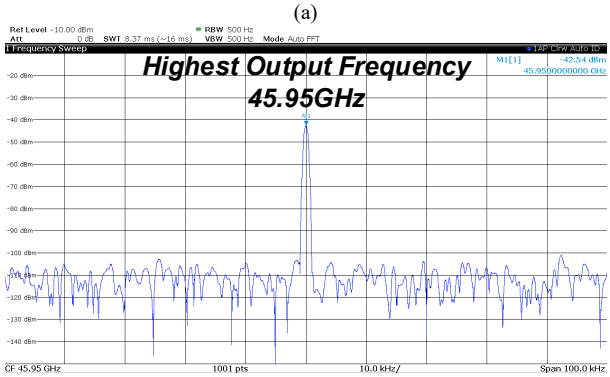
above 72 GHz is generated from the SMA100B R&S signal generator and an SMZ110 frequency multiplier. The total insertion loss of the coaxial cable, the WR-10 to 1.0 mm connector adapter and the GSG probe is around 8 dB. However, the output power of the frequency multiplier is insufficient, and the insertion loss cannot be fully calibrated. Therefore, the maximum output power is −4 dBm above 75 GHz. The output is captured with a GSG probe and FSWP50 R&S Spectrum Analyzer. A bias-T is also adopted to provide a DC-bias for the open-drain output buffer.

B. Chip#1

Fig. 22 shows the measured input sensitivity curves under both 0.9 V and 0.6 V power supply. With −4 dBm input power, 0.9 V power supply, and 5.8 mW power consumption, the LR can reach up to 63.1 GHz (from 28.8 GHz to 91.9 GHz, 104.6% of the center frequency), which corresponds to a FoM of 10.88 GHz/mW. For low power considerations, when the power supply decreases to 0.6 V, the LR remains 50 GHz (from 38 GHz to 88 GHz, 79.4% of the center frequency), with 2.2 mW power consumption, which corresponds to a FoM of 22.73 GHz/mW. The measured LR and FoM under different power supplies are shown in Fig. 23. The ILFD can work under 0.5 V power supply to achieve a higher FoM of 23.85 GHz/mW, but with only 31 GHz LR (from 47 GHz to 83 GHz, 47.7% of the center frequency). The output spectra when the ILFD is locked at the lowest and highest frequencies under −4 dBm input power and 0.9 V power supply are shown in Fig. 24. To make



(a)



(b)

Fig. 24. Measured output spectra when chip#1 is locked under 0.9 V power supply at (a) the lowest frequency and (b) the highest frequency.

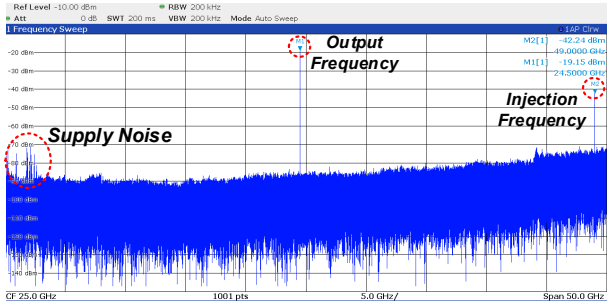


Fig. 25. Measured full span output spectra when chip#1 is locked under 0.9 V power supply at 49.5 GHz.

sure there's no either harmonic locking or serious tone, the measured full span output spectra with 200 kHz RBW at 49.5 GHz input frequency is plotted in Fig. 25. The spurs at low frequencies are from supply noise. This is because the probe test need a vacuum pump to ensure that the chip is firmly adsorbed on the probe station. When the pump turned on, the noise generated from the pump coupled to the power supply cable, and the spurs appeared. This problem could be solved by implementing better supply decoupling or using a better vacuum pump. Also, the frequencies and power of the spurs are less than 4 GHz and −70 dBm, which will not affect the desired signal.

Fig. 26 shows the measured phase noise with 84 GHz input frequency, −4 dBm injection signal and 0.9 V power supply. Once the ILFD is locked, the phase noise difference is about 6 dB from 1 kHz to 10 MHz offset, which is in good agreement with the theoretical value. However, when the offset frequency goes above 1 MHz, the noise floor of the spectrum analyzer becomes dominant, and the noise floor will be touched

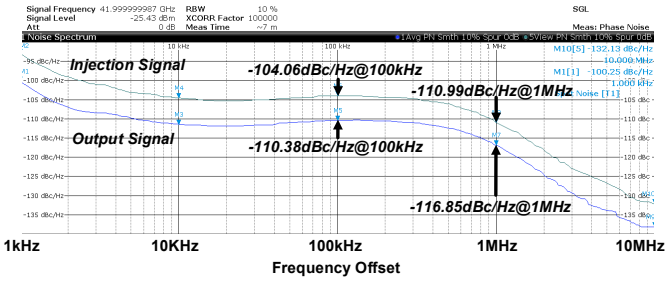


Fig. 26. Measured phase noise of chip#1 with 84 GHz input frequency, −4 dBm injection signal and 0.9 V power supply.

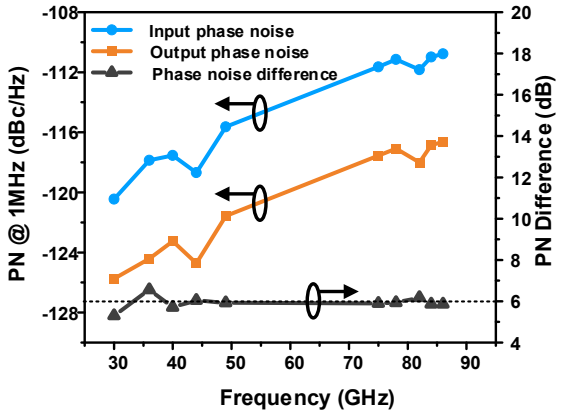


Fig. 27. Measured phase noise difference between input and output of chip#1 at different frequencies.

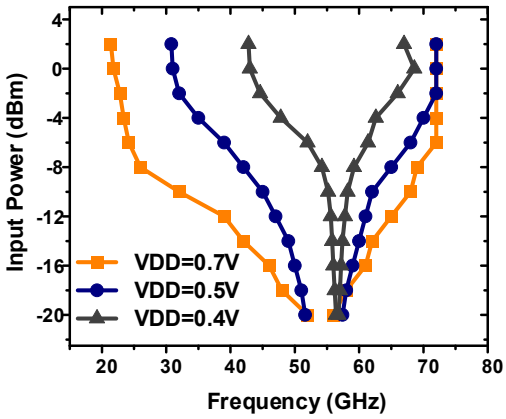


Fig. 28. Measured input sensitivity curves of chip#2 under 0.7 V, 0.5 V and 0.4 V power supplies.

inevitably when the input power of the spectrum analyzer is not strong enough. Therefore, when the injection frequency is above 84 GHz, the output power is too weak to be detected accurately by the spectrum analyzer at 10 MHz offset.

Fig. 27 shows the input and output phase noise at 1 MHz offset with different injection frequencies. The phase noise measurement results from 50 to 75 GHz are missing because of the lack of a harmonic mixer for this frequency band to down-convert the injection signal. Since this frequency band is in the middle of the LR, the phase noise difference is not affected. Moreover, the phase noise differences represent less than 1 dB degradation at the edge of the LR. Therefore, based on our experience, we believe the phase noise difference are consistent with the theoretical value all over the whole frequency band.

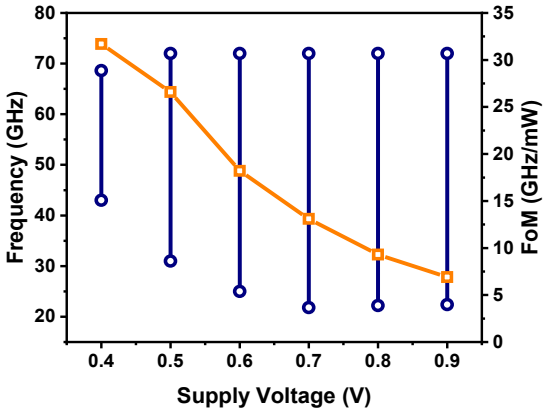
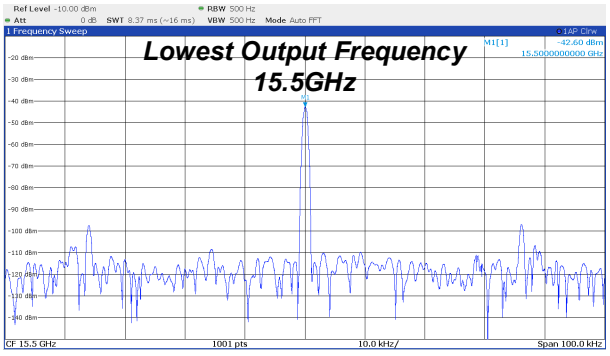
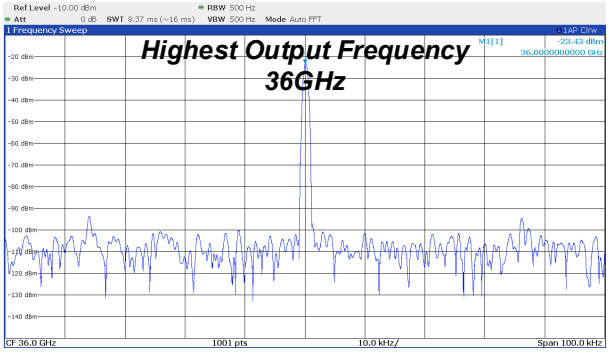


Fig. 29. Measured LR and FoM of chip#2 under different power supplies.



(a)



(b)

Fig. 30. Measured output spectra when chip#2 is locked under 0.5 V power supply at (a) the lowest frequency and (b) the highest frequency.

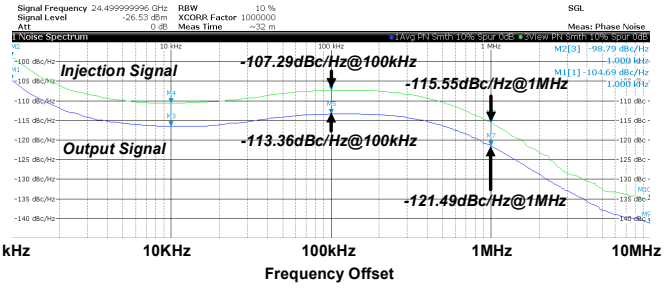


Fig. 31. Measured phase noise of chip#2 with 49 GHz input frequency, 0 dBm injection signal and 0.5 V power supply.

C. Chip#2

The measured input sensitivity curves under 0.7 V, 0.5 V and 0.4 V power supply are plotted in Fig. 28. With 0 dBm input power, 0.7 V power supply, and 3.84 mW power dissipation, the LR can reach up to 50.2 GHz (from 21.8 GHz to 72 GHz, 107% of the center frequency), which corresponds to a FoM of 13.1 GHz/mW. For low power considerations, when the power supply is 0.5 V, the LR remains 41 GHz (from 31 GHz to 72 GHz, 79.6% of the center frequency) with only 1.54 mW power dissipation, which corresponds to a FoM of 26.6 GHz/mW. Fig. 29 shows the measured LR and FoM under different power supplies. Chip #2 can work even with a 0.4 V power supply. Although only 25.6 GHz LR (from 43 GHz to 68.5 GHz, 45.9% of the center frequency) remains, a higher FoM of 31.7 GHz/mW is achieved. In summary, chip #2 realizes a wide LR and low power consumption under 0.5 V power supply. Fig. 30 shows the output spectra when chip #2 is locked at the lowest and highest frequencies under 0 dBm input power and 0.5 V power supply, respectively.

Phase noise performances are shown in Fig. 31 with a 49 GHz, 0 dBm injection signal. The phase noise difference is also around 6 dB at the offset frequencies from 1 kHz to 10 MHz.

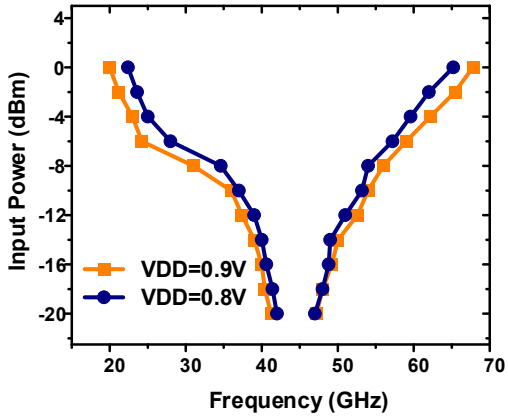


Fig. 32. Measured input sensitivity curves of chip#3 under 0.9 V and 0.8 V power supplies.

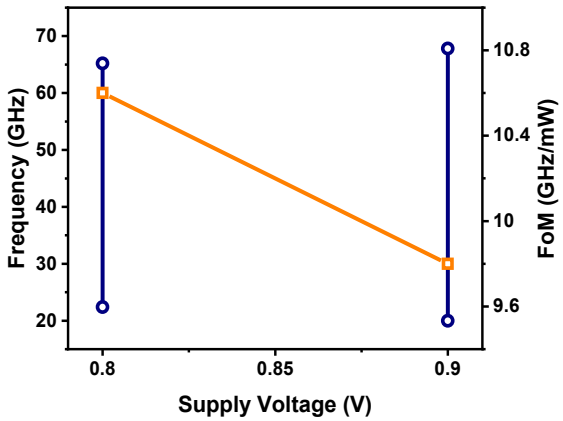


Fig. 33. Measured LR and FoM of chip#3 under 0.9 V and 0.8 V power supplies.

D. Chip#3

The measured input sensitivity curves under 0.9 V and 0.8 V power supply are illustrated in Fig. 32. With 0 dBm input power, 0.9V power supply and 4.9 mW power consumption, the LR is 47.8 GHz (from 20 GHz to 67.8 GHz, 108.9% of the center frequency), corresponding to a FoM of 9.8 GHz/mW. Fig. 33

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

	Process	Topology	Supply Voltage (V)	Operation Frequency (GHz)	Locking Range (GHz)	Input Power (dBm)	PN Diff. (dBc/Hz) 100k	PN Diff. (dBc/Hz) 1M	Power (mW)	Core Area (mm^2)	FoM[$] (GHz/mW)
This work #1	40nm	8th-Order Transformer-Based	0.9	28.8-91.9	63.1 (104.5%)	-4	6	6	5.8	0.02	10.9
			0.6	38-88	50 (79.4%)	-4	6	6	2.2		22.7
This work #2			0.7	21.8-72	50.2 (107%)	0	6	6	3.84	0.027	13.1
			0.5	31-72	41 (79.6%)	0	6	6	1.54		26.6
This work #3			0.9	20-67.8	47.8 (108.9%)	0	6	6	4.9	0.02	9.8
JSSC'17 [7]	65nm	Dynamic Latch (Divide-by-4)	1	16-67**	51 (122.2%)	-10	12	12	6.2-8.7	0.00312	5.87
JSSC'17 [11]	130nm SiGe	Distributed Injection Locking	1.15	35-44 41-59.5	9 (22.8%) 18.5 (36.8%)	0	6	0#	3.8	0.046	2.4 4.9
JSSC'13[12]	65nm	Frequency Tracking	0.8	53.4-79.4	26 (39.2%)	0	6#	6#	2.9	0.126	8.97
TCASI'16 [15]	65nm	Transformer-Distribution	1.2	58-77.8	19.8 (29.2%)	0	6	6	1.44	0.013	13.8
TMTT'17 [16]	90nm	Inductive Peaking and Forward-Body-Bias	0.6	12-32	20 (90%)	0	N/A	N/A	2.4	0.45*	8.3
TMTT'18 [17]	90nm	Split Transformer-Coupled Oscillator	0.7	71.5-97	21.9 (25.4%)	0	6	N/A	2.45	0.026	8.9
JSSC'18 [18]	65nm	4th-Order Transformer-Based	0.42	32.3-61.9	29.6 (62.7%)	0	6	6	1.2	0.07	24.7

* The overall chip size.
# Captured from the measurement phase noise figure.
$ FoM=locking range/power consumption (GHz/mW).
** The locking range is achieved by tuning mechanism, and the maximum frequency is limited by the available instrument.

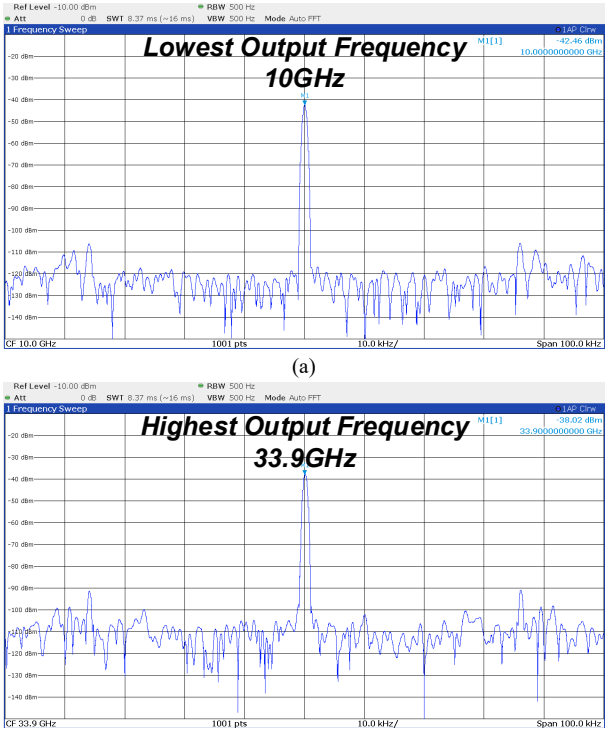


Fig. 34. Measured output spectra when chip#3 is locked under 0.9 V power supply at (a) the lowest frequency and (b) the highest frequency.

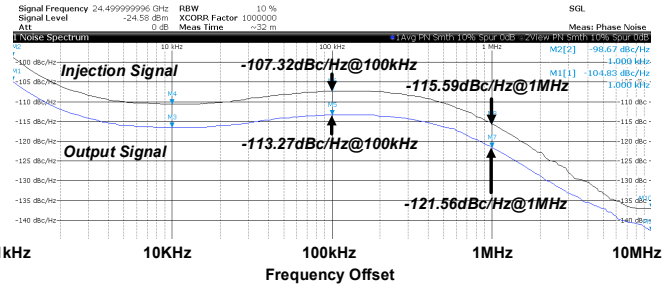


Fig. 35. Measured phase noise of chip#3 with 49 GHz input frequency, 0 dBm injection signal and 0.9 V power supply.

plots the measured LR and FoM under 0.9 V and 0.8 V power supply. Chip#3 cannot work when the power supply is lower than 0.8 V since the start-up condition is hard to satisfy. With 0 dBm input power, 0.8 V power supply and 4.05 mW power consumption, the LR is 42.8 GHz (from 22.4 GHz to 65.2 GHz, 97.7% of the center frequency), which corresponds to a FoM of 10.6 GHz/mW. Compared with chip#1 and chip#2, the measurement results of chip#3 further illustrate that the class-C structure is not a good option for power reduction in this design. The output spectra when chip#3 is locked at the lowest and highest frequencies under 0 dBm input power and 0.9 V power supply are shown in Fig. 34.

Phase noise performances are shown in Fig. 35 with a 49 GHz, 0 dBm injection signal. The phase noise difference is also around 6 dB at the offset frequencies from 1 kHz to 10 MHz.

Table I summarizes the measurement results of the designs in this work and compares them with recently reported state-of-the-art mm-wave ILFDs. Overall, compared with published mm-wave ILFDs, chip#1 exhibits a best-in-class LR, and chip#2 achieves the best FoM. Fig. 36 shows a comparison of the FOMs in this work with those of recent ILFDs in CMOS technologies.

V. CONCLUSION

In this paper, the LR limitation of ILFDs and methods to enhance the LR are discussed. By analyzing the impedance characteristic of the high-order transformer-based resonator in

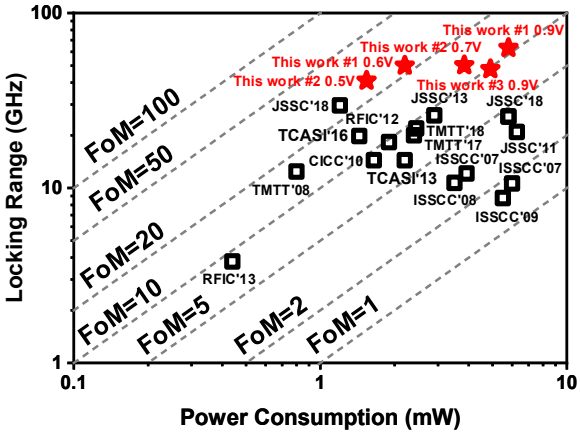


Fig. 36. FoM comparison.

ILFDs and comparing different orders of transformer-based resonators, the proposed resonator is proved to be the best choice for the ultra-wide LR ILFD design. The LR is improved significantly using the proposed 8th-order transformer-based resonator without an extra tuning mechanism or chip area. Furthermore, the resonator implementation methods and trade-offs are discussed. Three state-of-the-art tuning-less ILFDs are fabricated in 40 nm CMOS technology. Chip#1 exhibits a best-in-class LR of 104.5% from 28.8 to 91.9 GHz while consuming 5.8 mW from a 0.9 V power supply. Chip#2 achieves the best FoM of up to 26.6 GHz/mW and 79.6% from 31 to 72 GHz LR with a 0.5 V voltage supply. Finally, chip#3 measures an LR of 108.9% from 20 to 67.8 GHz while consuming 4.9 mW from a 0.9 V power supply. The phase noise performances are measured for these three chips, and 6 dB phase noise differences are achieved, which is close to the theoretical value. To the best of our knowledge, the proposed ILFDs achieve the best LR and the best FoM among the state-of-the-art mm-wave ILFDs.

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