Tuning-Less Injection-Locked Frequency Dividers with Wide Locking Range Utilizing 8th-Order Transformer-Based Resonator

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***Abstract*—This paper presents two tuning-less ultra-wide locking range (LR) injection-locked frequency dividers (ILFD). By utilizing an 8th-order transformer-based resonator, the LR can be improved significantly. Also, an inductive gain peaking technique is adopted to ensure start-up condition and achieve low power consumption. Two chips are fabricated in 40nm CMOS technology. The first chip exhibits a best-in-class LR of 104.5% from 28.8 to 91.9 GHz while consuming 5.8mW with a 0.9V power supply. The second chip achieves the best figure of merit (FoM) up to 26.6GHz/mW and 79.6% from 31 to 72 GHz LR with a 0.5V power supply.**

***Keywords*—high-order resonator, inductive peaking, injection-locked frequency divider, locking range, phase response, transformer.**

I. Introduction

The aggressively increasing demands of the millimeter-wave (mm-wave) communications, such as multi-band 5G mobile communication systems and 77GHz automotive radars, have attracted lots of attention in recent years. Frequency dividers are essential blocks for frequency synthesizers in mm-wave communication systems. Compared with the current-mode logic (CML) frequency divider and the miller frequency divider, the injection-locked frequency divider (ILFD) is more suitable for mm-wave applications. However, ILFD suffers from narrow locking range (LR), which is usually smaller than 20%. Distributed LC tanks were proposed to increase the LR by minimizing the parasitic capacitance [1], [2], but more inductors are required, which means larger chip area is inevitable. The frequency tracking [3-5] and transformer-distribution [6], [8] were other ways to improve LR, but still less than 40%. The inductive peaking and forward-body-bias techniques were applied to enhance LR, which can reach up to 90.9% [7]. A 4th-order transformer-based resonator was used to achieve a LR to 62.7% with only 1.2mW power consumption [9]. Although extraordinary performances have been achieved before, the LR can still be significantly enlarged to be suitable for multi-band mm-wave applications and consume less power with a compact chip area.

In this paper, two tuning-less ILFDs utilizing the 8th-order transformer-based resonator and the inductive peaking technique are proposed to achieve an ultra-wide locking range with low power consumption and compact chip area.

This paper is organized as follows. Section II reviews the limitation of conventional ILFDs and presents the proposed 8th-order transformer-based resonator. Section III describes the circuit implementation of the proposed ILFDs. Measurement results and conclusions are analysed in Section IV and Section V, respectively.

II. Proposed Locking Range Enhancement with 8th-order Transformer-based Resonator

A. Conventional ILFD

Figs. 1(a), 1(b) and 1(c) show the behaviour model, half-circuit and phasor diagram of a conventional ILFD based on a simple LC tank, respectively. The injection device M_{inj} acts as a mixer which mixes the input signal ω_{inj} and the oscillation signal ω_{osc}, then translates I_{inj} to $\omega_{osc} \pm \omega_{inj}$, with the sum component suppressed by the tank [10].

According to the phasor diagram, the locking range is typically limited by the maximum total phase shift Φ_{max} of the resonator and the injection current. Once I_{inj} and I_{osc} of the circuit are determined, Φ_{max} is fixed. Therefore, flattening the phase response of the resonator under the same Φ_{max} can significantly improve the LR.

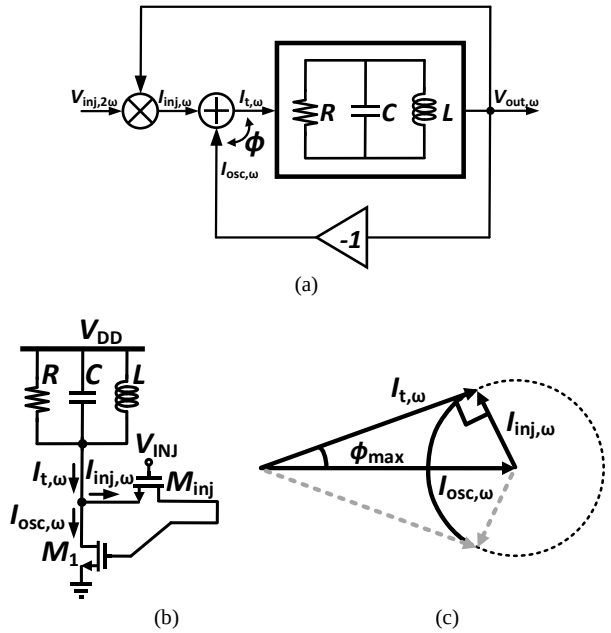


Fig. 1. Conventional ILFD: (a) behaviour model; (b) half-circuit; (c) phasor diagram.

B. Proposed 8th-order transformer-based resonator

Fig. 2 shows the phase curve comparisons among the LC-type resonator, the 4th-order transformer-based resonator, and the 8th-order transformer-based resonator. As shown in Fig. 2, the phase response of the proposed 8th-order resonator is much flatter，achieving a larger LR. Ideally, there should be seven zero-crossing points in 8th-order resonator's phase response.

However, to guarantee the magnitudes of the four peaks almost the same, achieving the same loading for the circuit, the phase response would decline rapidly, as plotted in Fig. 3(a), red curve. For the latter peaks, the inductances of former peaks have changed to the capacitances. Therefore, large inductances of the latter peaks are indispensable to compensate for former capacitances that can pull the phase response back upon zero. In other words, the magnitude of the four peaks should have a significant positive slope, as plotted in Fig. 3(a), green curve, and blue curve. Although the LR of the blue curve is 1.8 times larger than the red curve, it introduces an extensive unbalanced loading for the circuit.

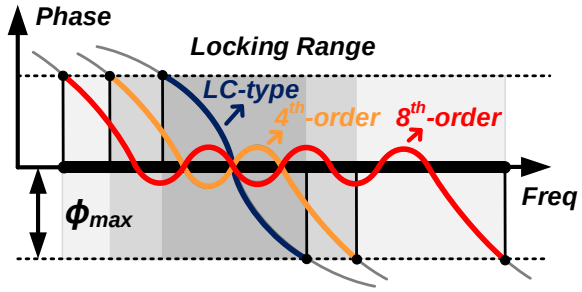


Fig. 2. Phase curve of the LC-type resonator, the 4th-order transformer-based resonator, and the 8th-order transformer-based resonator.

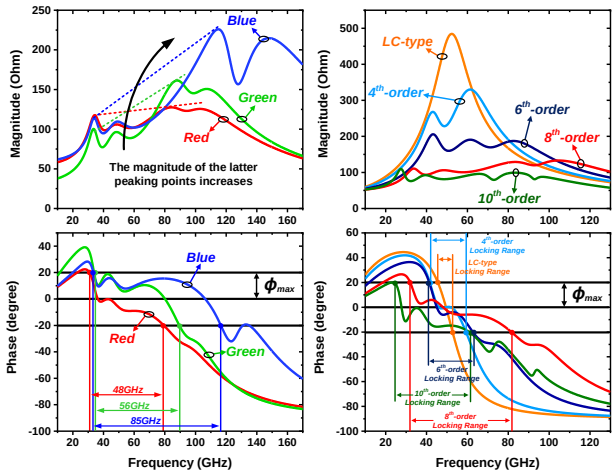


Fig. 3. (a) The simulated phase response comparison of different magnitude slope of the 8th-order resonator; (b) the simulated impedance of the same total tank Q of five different resonators.

The quality factor (Q) of each inductor in the 8th-order resonator and the whole tank is carefully designed to be low value. The reason is that high Q would introduce a large ripple for the phase response, which would be out of the upper and lower boundaries of Φ_{max}, and give rise to the in-band loss-of-lock. Fig. 3(b) illustrates the LR comparison of five different resonators under the same total tank Q. For the same loading consideration with the 8th-order resonator, the phase response of the 10th-order resonator decreases faster since it is more difficult to compensate for the former capacitances. Therefore, the 8th-order resonator has the widest LR among all of them. Furthermore, as depicted in Fig. 4(a), a test circuit is designed to compare the LR of these five resonators which have the same total tank Q, under the same power consumption. Just by changing the resonator from LC-type to 10th-order, the LR of 8th-order resonator is 5.6 times, 1.9 times, 1.5 times and 1.1 times larger than the LC-type, 4th-order, 6th-order and 10th-order resonators, respectively, as plotted in Fig. 4(b). These simulation results further illustrate that the 8th-order resonator is the best option for this work.

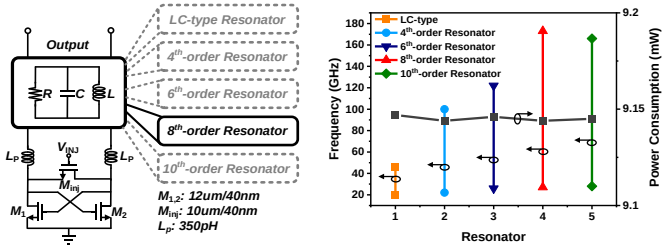


Fig. 4. (a) The schematic of a test circuit, and (b) the simulated locking range and power consumption comparison of the five resonators.

However, conventionally the gain condition cannot be satisfied due to the low impedance of the low-Q tank. To ensure the gain condition is met, a higher current is required, leading to higher power consumption. To solve this problem, a peaking inductor (L_p) is inserted between the cross-coupled pair and the resonator, so that the total impedance of the whole tank will be enhanced, which relaxes the gain condition and reduces power consumption simultaneously [9].

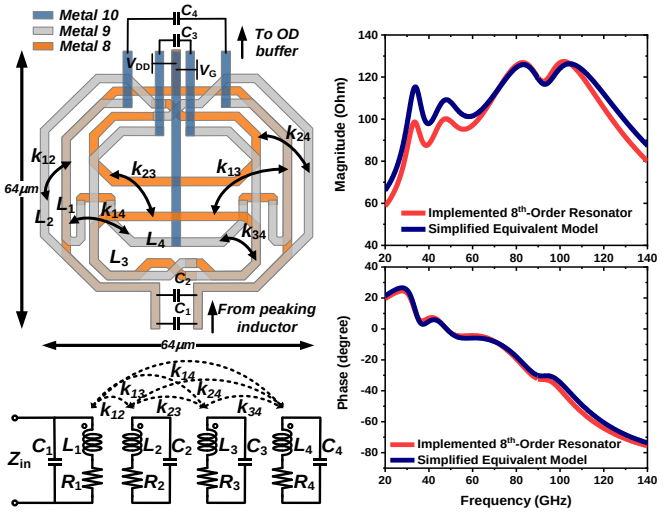
III. Circuit Implementation

Fig. 5(a) depicts the proposed 8th-order transformer-based resonator and its simplified equivalent model. In this work, lower metal layers, metal 9 and metal 8 with a narrow width and spacing, are used to design the resonator, which brings to a very compact area of the resonator with only 64μm × 64μm. The resonator is determined by at least eighteen parameters, including four self-inductances, four tuning capacitances, four series resistances, and six magnetic coupling coefficients. All parameters should be selected elaborately based on comprehensive performance and feasibility considerations. A practical method to design this resonator is to choose the different self-resonant frequencies of each coil first, then by tuning magnetic coupling coefficients and series resistances to find a set of suitable parameters. Fig. 5(b) presents the comparison of impedance simulations between the resonator using electromagnetic (EM) simulator and the equivalent model. Only a few acceptable mismatches exist between these two curves, which means this model is accurate enough to guide the design.

Fig. 6 shows the circuit realization of the proposed ILFD. An 8th-order transformer-based resonator is adopted to improve the LR. Two peaking inductors (L_p) are introduced to satisfy the gain condition and reduce power consumption. Moreover, two open-drain buffer transistors are used to drive the 50Ω loading of the instrumentations. The device ratio of the cross-coupled pair and injection transistor is optimized to suit for this work.

IV. Measurement Result

Two tuning-less transformer-based ILFDs are fabricated in 40nm CMOS technology. The chip microphotographs are shown in Fig. 7. The core area of each chip is 0.02mm^2 and 0.027mm^2, respectively. Both chip #1 and chip #2 use the implemented 8th-order transformer-based resonator, but with a different value of L_p and transistor size. Chip#1 focuses on an ultra-wide LR while consuming more power. Chip#2 aims at low power consumption, which could achieve a high figure of merit (FoM).



(a) (b)

Fig. 5. (a) Proposed 8th-order transformer-based resonator and the simplified equivalent model, and (b) comparison of simulated results on magnitude (top) and phase (bottom) of the resonator and the model.

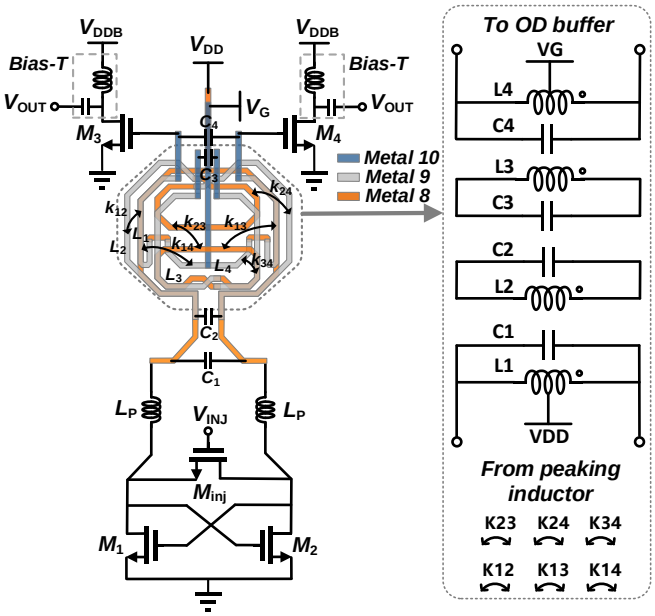
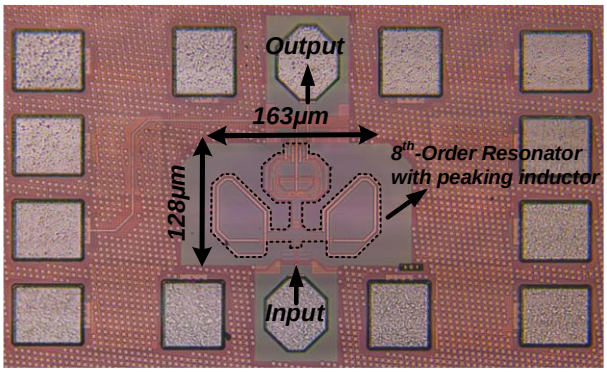


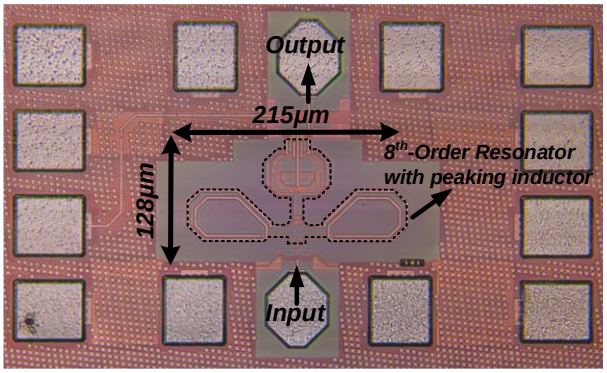
Fig. 6. Circuit schematic of the proposed ILFD.

The input signal is generated from SMA100B R&S signal generator and SMZ110 frequency multiplier, and a GSG probe is used for signal injection. The output is captured with a GSG probe and FSWP50 R&S Spectrum Analyzer. The measured input sensitivity curves of two proposed ILFDs under different power supplies are shown in Fig. 8. Due to the insufficient output power of the frequency multiplier, the maximum input power of chip#1 is −4dBm above 75GHz. With −4dBm input power, 0.9V power supply, and 5.8mW power consumption, its LR can achieve up to 63.1GHz (from 28.8GHz to 91.9GHz, 104.6% of the center frequency). The lowest and highest output frequency spectrums of chip#1 under −4dBm input power and 0.9V power supply were shown in Fig. 9. With 0dBm input power, 0.5V power supply, and only 1.54mW power dissipation, the LR of chip#2 can reach 41GHz (from 31GHz to 72GHz, 79.6% of the center frequency), which corresponds to a FoM of 26.6 GHz/mW.

Fig. 10 shows the measured phase noise of chip#1 with 84GHz input frequency and 0.9V power supply. Once the ILFD is locked, the phase noise difference is about 6dB, which is in good agreement with the theoretical value.



(a)



(b)

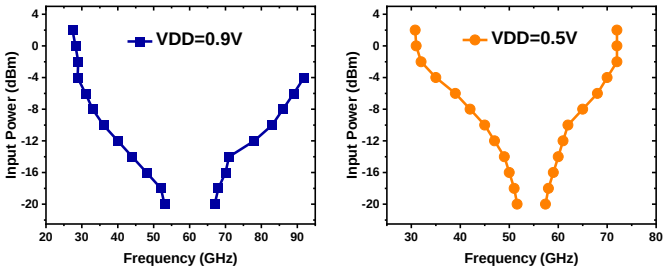
Fig. 7. Chip microphotographs: (a) chip#1; (b) chip#2.

Table I summarizes the measurement results of this work and compares them with that of recently reported state-of-the-art mm-wave ILFDs. Overall, compared with published mm-wave ILFDs, chip#1 exhibits a best-in-class LR, and chip#2 achieves the best FoM.

V. Conclusion

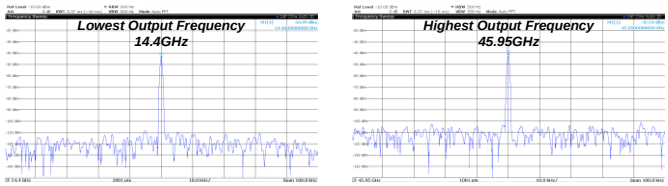
Two chips using the proposed 8th-order transformer-based resonator are implemented and fabricated in 40nm CMOS technology. Chip#1 exhibits a best-in-class LR of 104.5%

from 28.8 to 91.9GHz while consuming 5.8mW with a 0.9 V power supply. Chip#2 achieves the best FoM up to 26.6 GHz/mW and 79.6% from 31 to 72GHz LR with a 0.5V voltage supply. To the best of our knowledge, the proposed ILFDs achieve the best LR and the best FoM among all the state-of-the-art mm-wave ILFDs ever reported.



(a) (b)

Fig. 8. Measured input sensitivity curves of two proposed ILFDs: (a) chip#1, (b) chip#2.



(a) (b)

Fig. 9. Measured output spectrum of chip#1: (a)28.8GHz; (b)91.9GHz.

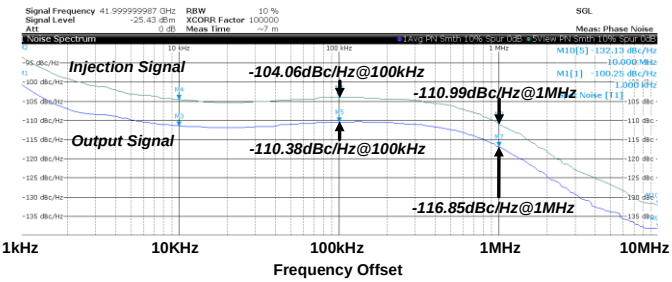


Fig. 10 Measured input and output phase noise at 84GHz input frequency of chip#1.

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REFERENCES

[1] B.-Y. Lin, K. Tsai and S. Liu, "A 128.24-to-137.00GHz injection-locked frequency divider in 65nm CMOS," in *IEEE International Solid-State Circuits Conference - Digest of Technical Papers*, pp. 282-283, 2009.

[2] A. Imani and H. Hashemi, "Distributed Injection-Locked Frequency Dividers," in *IEEE Journal of Solid-State Circuits*, vol. 52, no. 8, pp. 2083-2093, Aug. 2017.

[3] Y. Chao and H. C. Luong, "A 2.9mW 53.4–79.4GHz frequency-tracking injection-locked frequency divider with 39.2% locking range in 65nm CMOS," in *IEEE Radio Frequency Integrated Circuits Symposium*, pp. 337-340, 2012.

[4] J. Yin and H. C. Luong, "A 0.8V 1.9mW 53.7-to-72.0GHz self-frequency-tracking injection-locked frequency divider," in *IEEE Radio Frequency Integrated Circuits Symposium*, pp. 305-308, 2012.

[5] Y. Chao and H. C. Luong, "Analysis and Design of a 2.9-mW 53.4–79.4-GHz Frequency-Tracking Injection-Locked Frequency Divider in 65-nm CMOS," in *IEEE Journal of Solid-State Circuits*, vol. 48, no. 10, pp. 2403-2418, Oct. 2013.

[6] Y. Chao and H. C. Luong, "Analysis and Design of Wide-Band Millimeter-Wave Transformer-Based VCO and ILFDs," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 63, no. 9, pp. 1416-1425, Sept. 2016.

[7] J. Cheng, J. Tsai and T. Huang, "Design of a 90.9% Locking Range Injection-Locked Frequency Divider With Device Ratio Optimization in 90-nm CMOS," *IEEE Transactions on Microwave Theory and Techniques*, vol. 65, no. 1, pp. 187-197, Jan. 2017.

[8] Y. Lin and H. Wang, "Design and Analysis of W-Band Injection-Locked Frequency Divider Using Split Transformer-Coupled Oscillator Technique," *IEEE Transactions on Microwave Theory and Techniques*, vol. 66, no. 1, pp. 177-186, Jan. 2018.

[9] J. Zhang, Y. Cheng, C. Zhao, Y. Wu and K. Kang, "Analysis and Design of Ultra-Wideband mm-Wave Injection-Locked Frequency Dividers Using Transformer-Based High-Order Resonators," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 8, pp. 2177-2189, Aug. 2018.

[10] B. Razavi, "A study of injection locking and pulling in oscillators," *IEEE J. Solid-State Circuits*, vol. 39, no. 9, pp. 1415-1424, Sept. 2004.

Table 1. Performance summary and comparison

		This Work		JSSC'18 [9]	TMTT'18 [8]	TMTT'17 [7]	TCASI'16 [6]	JSSC' 13 [5]
		Chip#1	**Chip#2**					
Process		**40nm CMOS**		65nm CMOS	90nm CMOS	90nm CMOS	65nm CMOS	65nm CMOS
Supply Voltage (V)		**0.9**	**0.5**	0.42	0.7	0.6	1.2	0.8
Operation Frequency (GHz)		**28.8-91.9**	**31-72**	32.3-61.9	71.5-97	12-32	58-77.8	53.7-79.4
Locking Range (GHz)		**63.1 (104.5%)**	**41 (79.6%)**	29.6 (62.7%)	21.9 (25.4%)	20 (90%)	19.8 (29.2%)	26 (39.2%)
Input Power (dBm)		**-4**	**0**	0	0	0	0	0
PN Diff. (dBc/Hz)	100k	**6**	**6**	6	6	N/A	6	6
	1M	**6**	**6**	6	N/A	N/A	6	6
Core Area (mm^2)		**0.02**	**0.027**	0.07	0.026	0.45*	0.013	0.126
Power (mW)		**5.8**	**1.54**	1.2	2.45	2.4	1.44	2.9
FoM (GHz/mW) **		**10.9**	**26.6**	24.7	8.9	8.3	13.8	8.97

* The overall chip size.

** FoM=locking range/power consumption (GHz/mW).