



# Computer Architecture

## LAB 12

**Fasiha Tariq-53289**

BS-CS 4

Submitted to:

Ma'am Ayesha Ikram

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## Task 1:

INP

OUT

CLA

OUT

HLT

```
EXECUTING...  
Enter Inputs, the first of which must be an Integer: 9  
Output: 9  
Output: 0  
EXECUTION HALTED NORMALLY due to the setting of the bit(s): [HALT-BIT]
```

## Task 2:

INP

CMA

OUT

HLT

Registers					
Name	Width	Data			
AC	16	1111	1111	1111	0011
AR	12	0000	0000	0001	
DR	16	0000	0000	0000	0000
E	1	0			
I	1	0			
IR	16	1110	0000	0000	0001
PC	12	0000	0000	0101	
S	1	1			

Registers					
Name	Width	Data			
AC	16	1111	1111	1111	1100
AR	12	0000	0000	0001	
DR	16	0000	0000	0000	0000
E	1	0			
I	1	0			
IR	16	1110	0000	0000	0001
PC	12	0000	0000	0101	
S	1	1			

```

EXECUTING...
Enter Inputs, the first of which must be an Integer: 3
Output: 3
Output: -4
EXECUTION HALTED NORMALLY due to the setting of the bit(s): [HALT-BIT]

```

### Task 3:

INP

INC

OUT

HLT

```

EXECUTING...
Enter Inputs, the first of which must be an Integer: 5
Output: 8
EXECUTION HALTED NORMALLY due to the setting of the bit(s): [HALT-BIT]

```

## Task 4:

Format

Implementation

Execute sequence

AC(0)!=0

INCR-PC

End

Data

Dec

Registers

Name	Width	Data
AC	16	0
AR	12	1
DR	16	0
E	1	0
I	1	0
IR	16	-8191
PC	12	4
S	1	-1

SPA X

1 INP

2 SPA

3 OUT

4 HLT

S

Addr

Hex

Data

Dec

MAIN

Addr	Data
000	63488
001	10
002	62464
003	57345
004	0
005	0
006	0
007	0
008	0
009	0
00A	0
00B	0
00C	0
00D	0
00E	0
00F	0
010	0
011	0
012	0

EXECUTING...

Enter Inputs, the first of which must be an Integer: 7

Output: 0

EXECUTION HALTED NORMALLY due to the setting of the bit(s): [HALT-BIT]

## Task 5:

Execute sequence

AC(0)!=1

INCR-PC

End

Data

Dec

Registers

Name	Width	Data
AC	16	0
AR	12	1
DR	16	0
E	1	0
I	1	0
IR	16	-8191
PC	12	4
S	1	-1

SPA X

1

INP

2

SNA

3

OUT

4

HLT

5

Addr

Hex

Data

Dec

MAIN

Addr	Data
000	63488
001	11
002	62464
003	57345
004	0
005	0
006	0
007	0
008	0
009	0
00A	0
00B	0
00C	0
00D	0
00E	0
00F	0
010	0
011	0
012	0

EXECUTING...

Enter Inputs, the first of which must be an Integer: -7

Output: 0

EXECUTION HALTED NORMALLY due to the setting of the bit(s): [HALT-BIT]