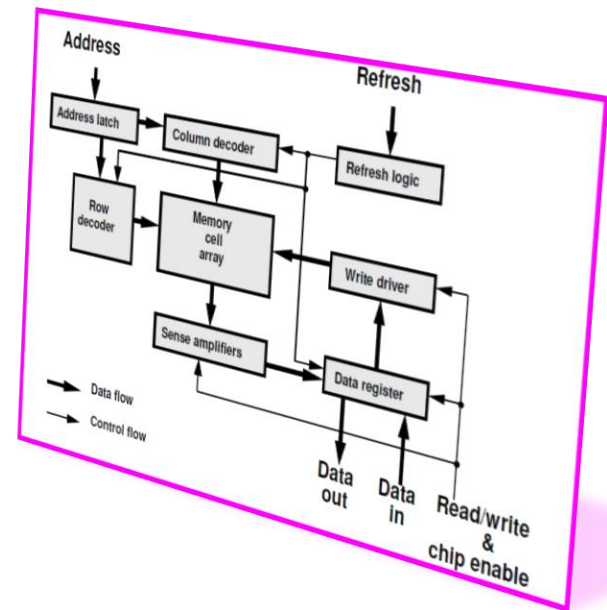


Outline

- Introduction
- Memory Fault Model
- Memory Test Algorithms
- Memory Fault Simulation* (not in exam)
- Memory Test Generation* (not in exam)
- Memory BIST* (not in exam)

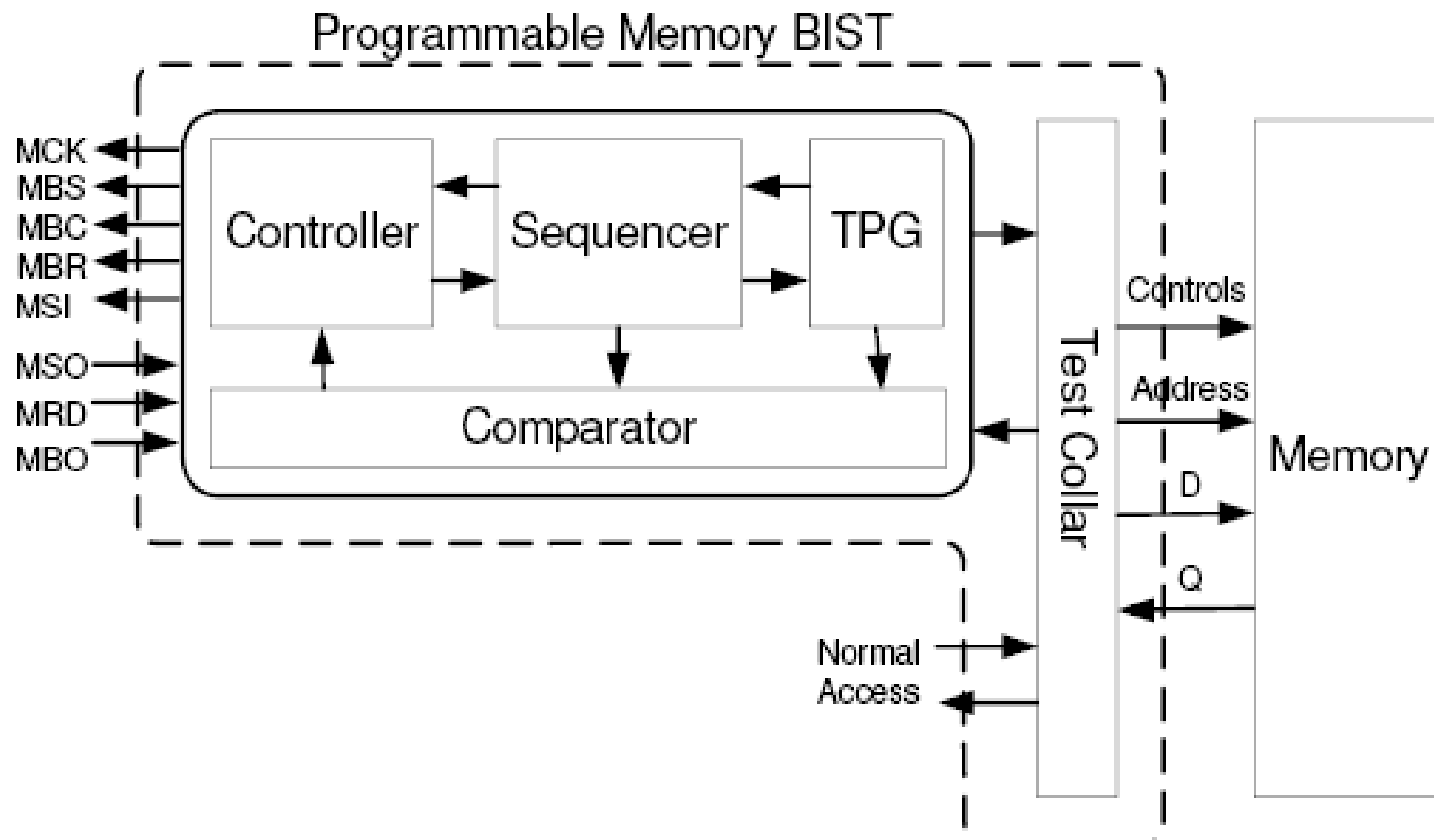


Typical RAM BIST Approaches

- Methodology (Architecture)
 - ◆ *Processor-based BIST*
 - * Programmable
 - ◆ *Hardwired BIST*
 - * Fast
 - ◆ Compact
 - ◆ *Hybrid*
- Interface
 - ◆ Serial (scan, 1149.1)
 - ◆ Parallel (embedded controller; hierarchical)
- Patterns (address sequence)
 - ◆ March & March-like
 - ◆ Pseudorandom
 - ◆ Others

General RAM BIST Architectures

- **Controller**: overall BIST flow
- **Sequencer**: address, data and timing sequence

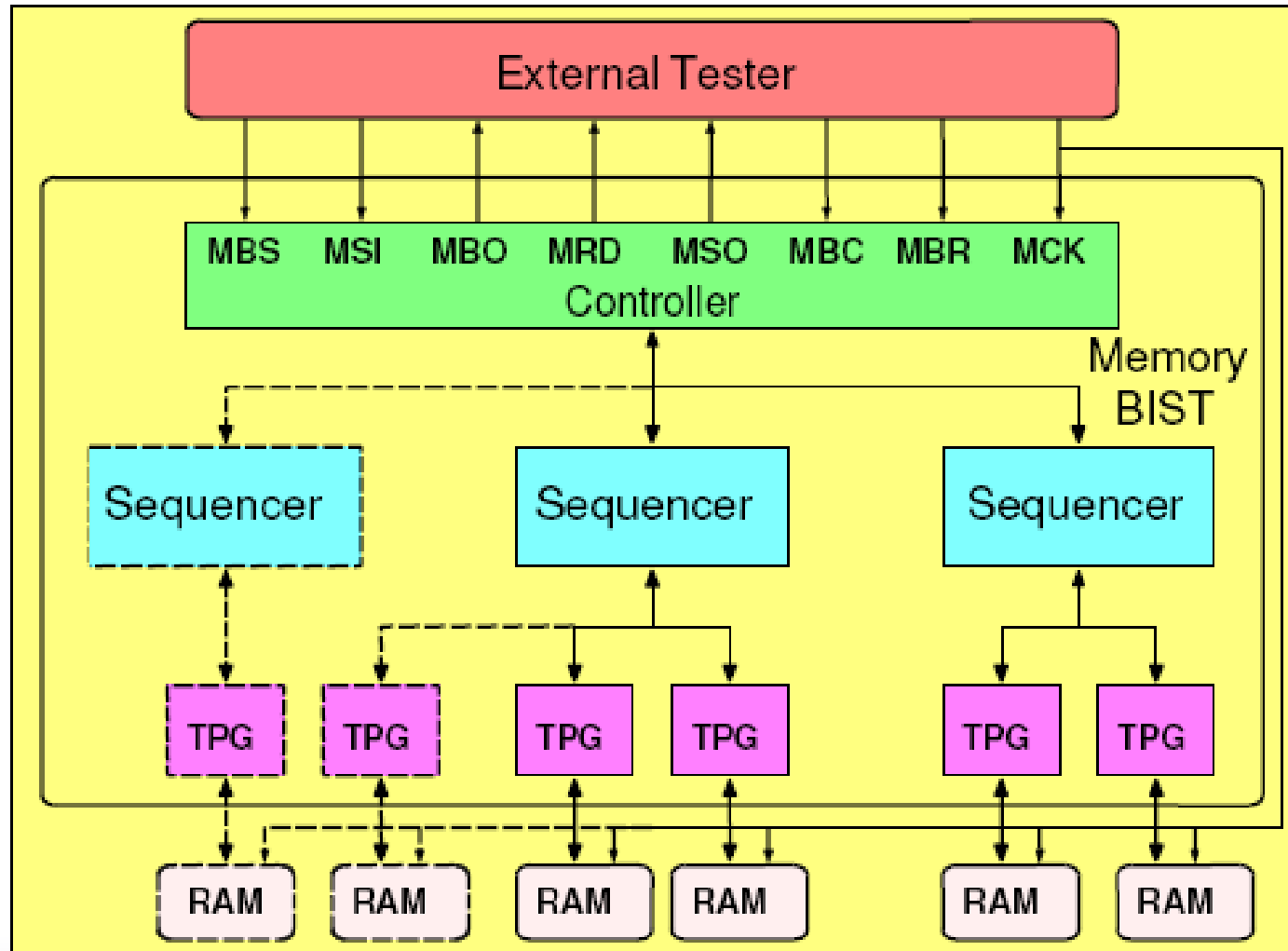


BIST I/O Pins

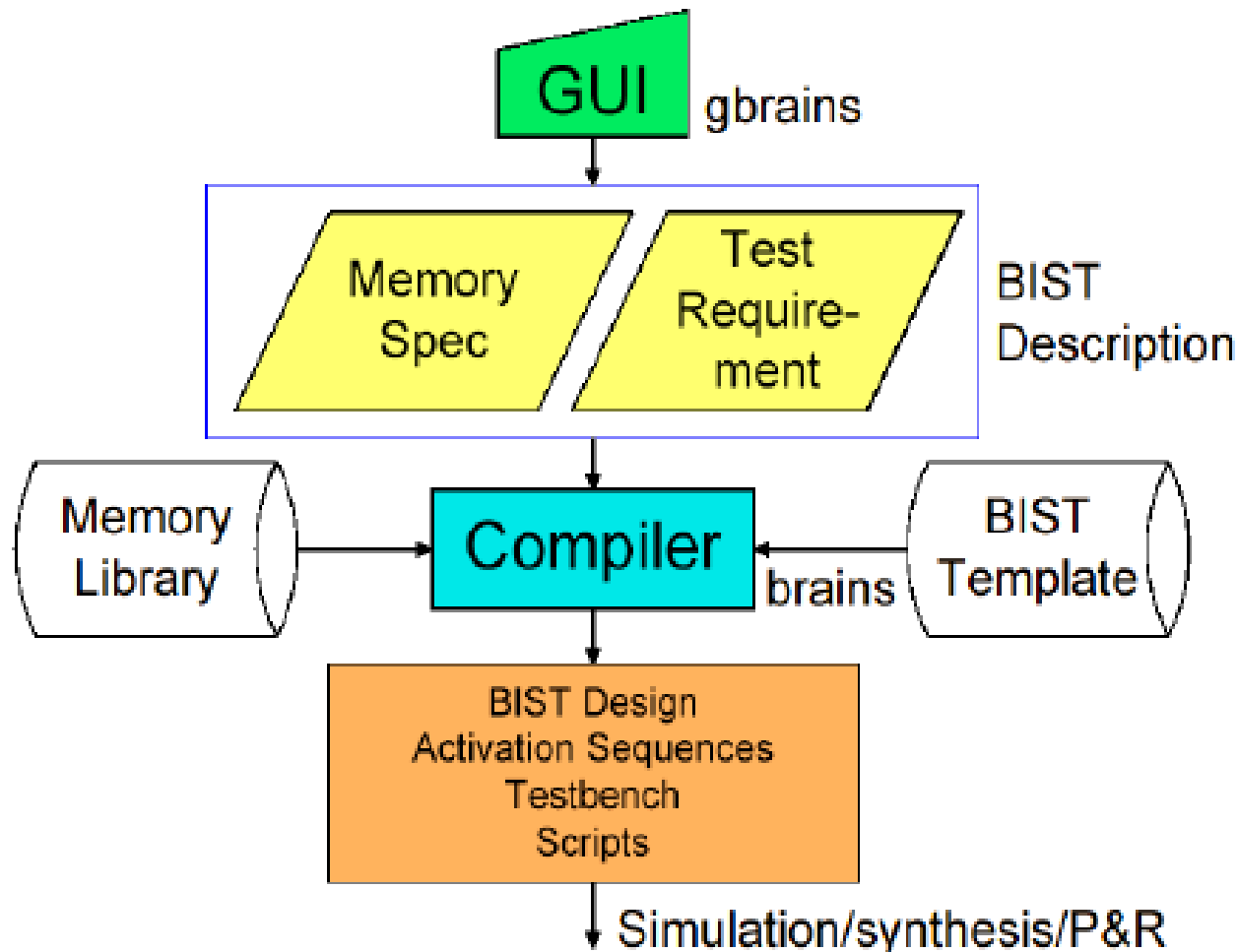
Name	IO	External IO	Descriptions
MBS	I	Yes	Memory BIST Selection
MBC	I	Yes	Memory BIST Control
MCK	I	Yes	Memory BIST Clock
MBR	I	Yes	Memory BIST Reset
MSI	I	Yes	Memory BIST command/data serial in
MSO	O	Yes	Memory BIST command/data serial out
MBO	O	Yes	Memory BIST Output
MRD	O	Yes	Memory BIST Output Ready
ADDR	O	No	Address Signals
D	O	No	Memory Data In
Q	I	No	Memory Data Out
CS	O	No	Chip Select
OE	O	No	Output Enable
WE	O	No	Write Enable

Multiple RAM Cores

- Controller and sequencer can be shared



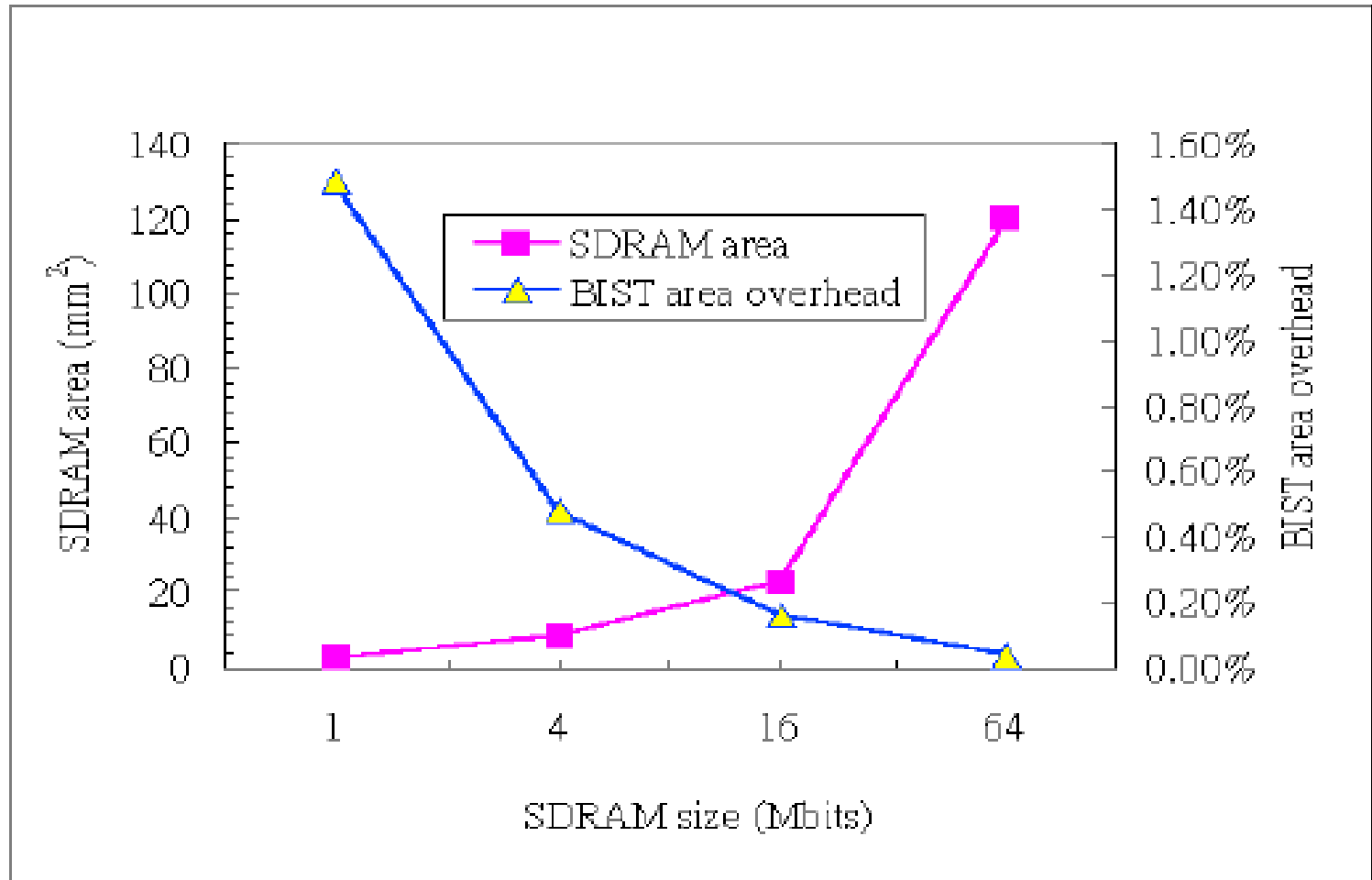
BRAINS Inputs and Outputs [Huang 99]



BRAINS Outputs

- **Synthesizable BIST design**
 - ◆ **At-speed testing**
 - ◆ **Programmable March algorithms**
 - ◆ **Optional diagnosis support**
 - * **Built-in Self Diagnosis, BISD**
- **Activation sequence**
 - ◆ **Test bench**
 - ◆ **Synthesis script**

Area Overhead



Summary

- **Memory testing are important**
- **Different memory requires different fault models**
- **March C is shortest march that detect all 4 fault models: 10N**
- **RAM BIST are needed for embedded memories**
 - ◆ **EDA tools available**

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