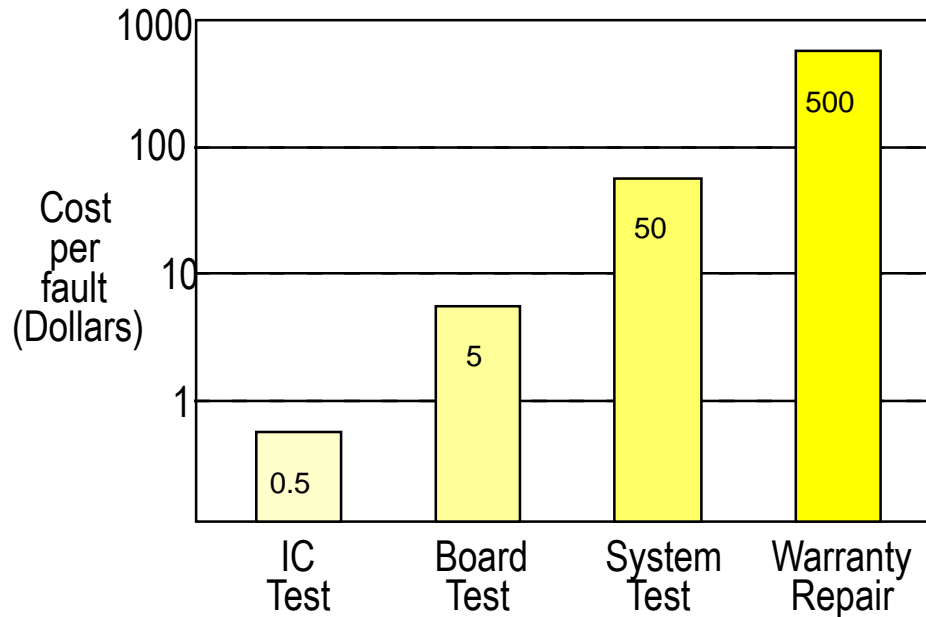# Introduction

- **What Is Testing**
- **Types of Testing**
- **Test Quality**
- <u>**Test Economics**</u>
  - ♦ <u>**Why and Who Invests in Test?**</u>
    - ∗ <u>**Global Semiconductor Industry**</u>
  - ♦ **How to Make Optimal Test Decision?**
- **Important Research Topics**
- **Conclusion**

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Why Invest in Testing?

- **Although testing is expensive**
  - ♦ **Repair cost is even more expensive!**
- **Rule of Tens [Davis 82]**

A Stitch in Time Saves Nine

15% Semiconductor Market Goes to Test

- **2021 global semiconductor market $555.9B USD WSTS)**
- **2021 Taiwan $145.8B USD, ~26% of global market**
  - ◆ **Fabless design $43.4B USD**
  - ◆ **Manufacture $79.6B USD**
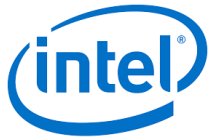 - ◆ **Packaging and testing $22.9B USD (~15%)**

Source TSIA
單位：億新台幣

2021年台灣IC產業產值統計結果

億新臺幣	21Q1	季成長	年成長	21Q2	季成長	年成長	21Q3	季成長	年成長	21Q4	季成長	年成長	2021	年成長	22Q1(e)	季成長	年成長
IC 產業產值	9,047	2.6%	25.0%	9,863	9.0%	31.6%	10,850	10.0%	25.1%	11,060	1.9%	25.4%	40,820	26.7%	11,034	-0.2%	22.0%
IC 設計業	2,602	5.3%	49.1%	3,069	17.9%	63.3%	3,301	7.6%	35.6%	3,175	-3.8%	28.5%	12,147	42.4%	3,110	-2.0%	19.5%
IC 製造業	5,001	1.4%	19.3%	5,284	5.7%	23.7%	5,869	11.1%	22.1%	6,135	4.5%	24.4%	22,289	22.4%	6,344	3.4%	26.9%
晶圓代工	4,374	0.1%	15.5%	4,554	4.1%	19.0%	5,081	11.6%	17.8%	5,401	6.3%	23.6%	19,410	19.1%	5,617	4.0%	28.4%
記憶體與其他製造	627	11.4%	54.1%	730	16.4%	64.0%	788	7.9%	60.5%	734	-6.9%	30.4%	2,879	51.0%	727	-1.0%	15.9%
IC 封裝業	984	0.4%	9.9%	1,020	3.7%	12.1%	1,150	12.7%	16.2%	1,200	4.3%	22.4%	4,354	15.3%	1,080	-10.0%	9.8%
IC 測試業	460	5.7%	13.6%	490	6.5%	12.6%	530	8.2%	20.5%	550	3.8%	26.4%	2,030	18.4%	500	-9.1%	8.7%
IC 產品產值	3,229	6.5%	50.0%	3,799	17.7%	63.5%	4,089	7.6%	39.7%	3,909	-4.4%	28.9%	15,026	44.0%	3,837	-1.8%	18.8%
全球半導體市場(億美元)及成長率(%)	-	-	-	-	-	-	-	-	-	-	-	-	5,559	26.2%	-	-	-

資料來源 TSIA：工研院產科國際所 (2022/02)

Many Companies Invest Heavily in Test

IDM

Fabless/Foundry

EDA

ATPG
Fault Sim.

Design

BIST, DFT
Boundary Scan

Manufacture

Fabrication, Assembly, Test
Physical Failure analysis

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World's Top EDA Companies

- **2019 global EDA market is about $10B USD**
  - ◆ **Growing ~10% each year**

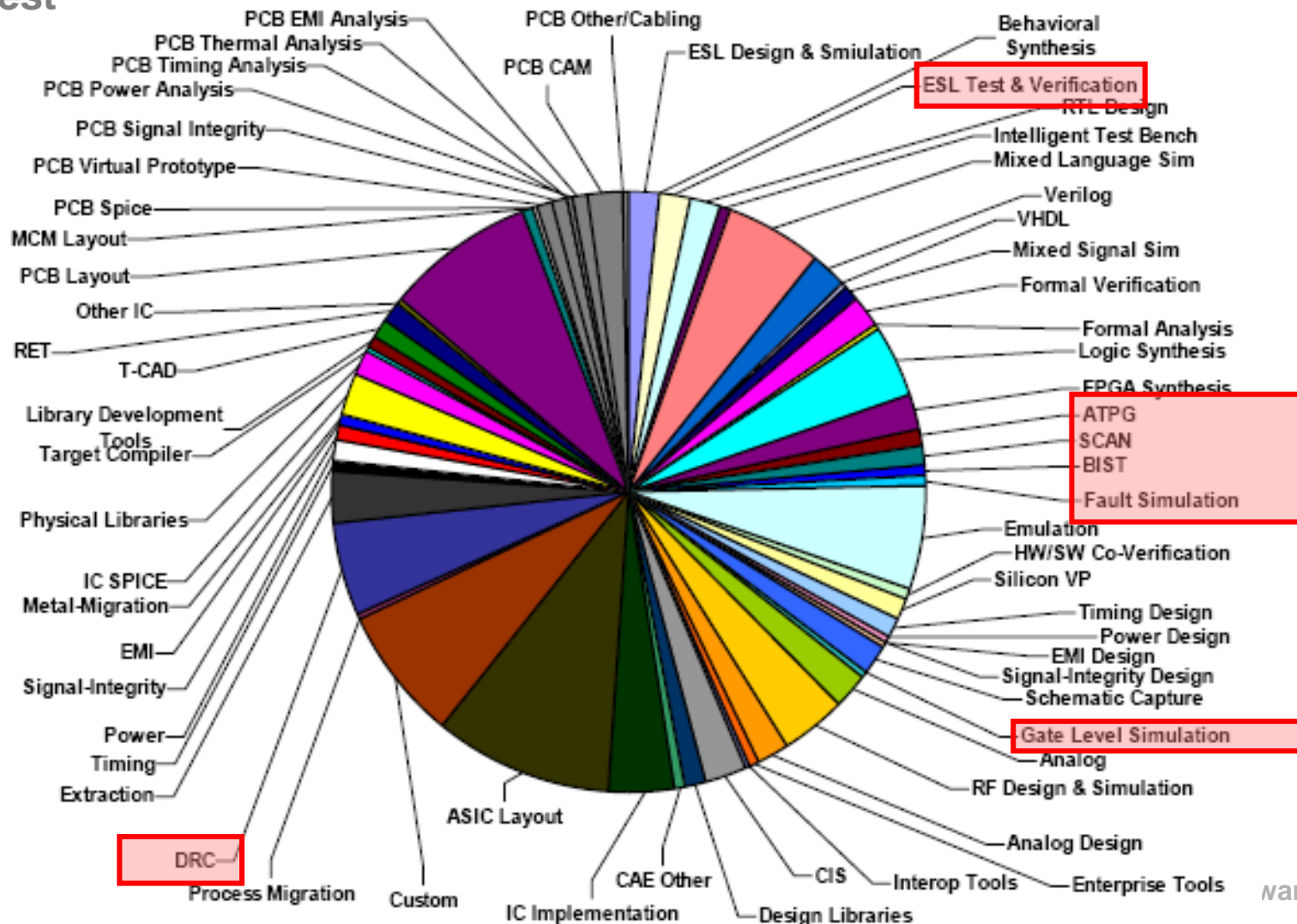| Company	Rank	Revenue	Country
Synopsys	1	$3.36 B	USA
Cadence	2	$2.33 B	USA
Mentor Graphics (now Siemens EDA)	3	$1.28 B (*2017)	Europe

SYNOPSYS®

cādence™

Mentor Graphics®

EDA Market by Tool

- **Test-related tools are about 5~10% EDA revenue**

dataquest 2012

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World's Top OSAT Companies

- *OSAT* = outsourced semiconductor assembly and test
- **About 1/2** IC tested by Taiwan

Analysis, 2020

Company	Rank	Market	Country
日月光 ASE	1	21.8%	Taiwan
艾克爾 Amkor	2	18.5%	USA
矽品 SPIL	3	14.4%	Taiwan
長電科技JCET	4	13.4%	China
力成 PTI	5	10.3%	Taiwan

Test Important for IC Industry

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Test?   **Repair?**

How to Make Optimal Decision?

- **Optimal test not only technical issue, but also economics issue**
  - Trade off between **test cost** and **repair cost**
- **Different product has different optimal decision**
  - **No single best decision** for all products!

What Cost Can We Optimize?

- **EDA**: ATPG, fault simulator …
  - Typically **10K ~ 100K** USD
- **Design:** insert DFT/BIST circuitry
  - Area/power/delay overhead about **5~10%**
- **OSAT:**
  - Equipment
    * Tester (Automatic Testing Equipment, ATE)
      - Typically **0.5~3 M** USD
    * Handler, probe station, Burn-in oven
  - Test application time (TAT)
    * Around **$50 to $300** USD per hour
    * ASIC takes **2~3** seconds. CPU can be **0.5~1** minute
  - load board, probe card
    * **$1K ~ 20K** USD

Many Decisions to Make

Case 1: DFT or Not?

Q1: Without DFT
   Y=98%, FC=70%. DL=?

A: 6,043 DPM

Q2: With DFT
   Y=97%, FC=99%. DL=?

A: 304 DPM

$$DL = 1 - Y^{(1-FC)}$$

Technically, DFT Improves DPM
Economically, Is DFT Worth Doing?

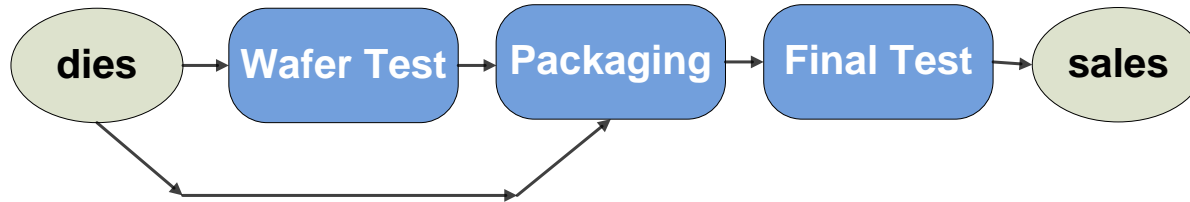# Case 1: DFT or Not? (Cont'd)

- **Q: Is it economical to insert DFT?**
- **A: Yes. This is true for many products.**
  - ◆ **Although Y drops, DL improves significantly**

$$DL = 1 - Y^{(1-FC)}$$

Item	w/o DFT	with DFT
Total # of **D**ies	1,000,000	900,000
Yield	98%	97%
FC fault coverage	70%	99%
DL =1-Y$^{(1-FC)}$	6,043 DPM	304 DPM
Sales=D x Y x $1	980,000	873,000
Repair cost=D x Y x DL x $100	592,163	26,587
Profit = S – R	387,837	846,413

DFT Is Worth Doing!

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Case 2: Wafer Test or Not?

Item	bad yield = 64%		good yield = 81%	
	with WT	no WT	with WT	no WT
Total # of **D**ies	1,000,000	1,000,000	1,000,000	1,000,000
C_{WT} = D x $0.02	20,000	0	20,000	0
Y_{WT}	80%	100%	90%	100%
C_{PK} = D x Y_{WT} x $0.1	80,000	100,000	90,000	100,000
C_{FT} = D x Y_{WT} x $0.06	48,000	60,000	54,000	60,000
Y_{FT}	80%	64%	90%	81%
Sales = D x Y_{WT} x Y_{FT} x $1	640,000	640,000	810,000	810,000
Cost = C_{WT} + C_{PK} + C_{FT}	148,000	160,000	164,000	160,000
Profit = S - C	492,000	480,000	646,000	650,000

WT or not Depends on Yield

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Case 3: To Burn or Not To Burn?

Q: Is it worth doing burn-in (BI)?
BI cost is $2 per die. BI improves quality by 1,000DPM.
Fabrication cost is 30% of price. Repair cost is 30 times price.

Item	ASIC, Price per die= $10		CPU, Price per die= $100	
	with BI	no BI	with BI	no BI
D_F=# of Dies fab	1,000,000	1,000,000	1,000,000	1,000,000
D_S=# of dies sold	999,000	1,000,000	999,000	1,000,000
D_B=# of bad dies sold	0	1,000	0	1,000
Sales = D_S x P	9,990,000	10,000,000	99,900,000	100,000,000
C_{FB}=D_F x P x 30%	3,000,000	3,000,000	30,000,000	30,000,000
C_{BI}=D_F x $2	2,000,000	0	2,000,000	0
C_{RP}=D_B x P x 30	0	300,000	0	3,000,000
Profit=S-C_{FB}-C_{BI}-C_{RP}	4,990,000	6,700,000	?	?

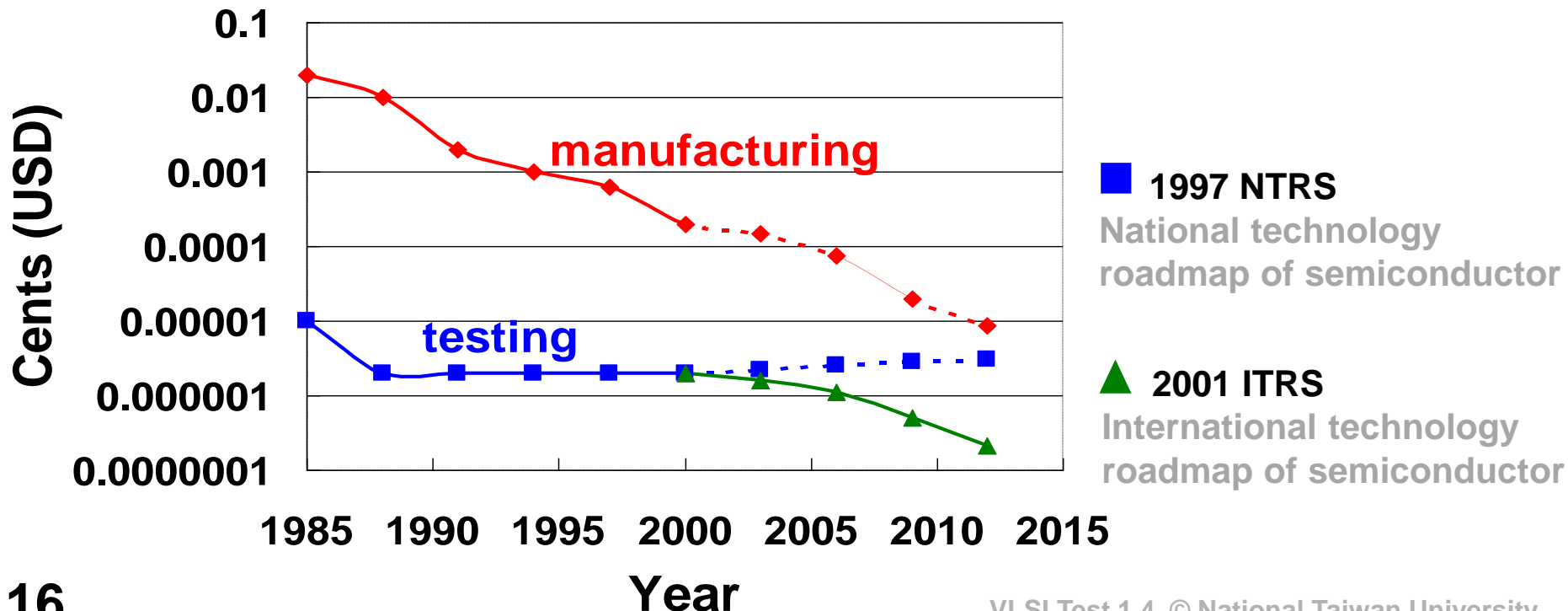**BI or not Depends on Price**

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Test Needs Continuing Improvements

- **NTRS 1997** predicted test cost will be greater than manufacturing cost
  - assume that historical trends continued
- **ITRS 2001** revised the prediction
  - Significant research efforts applied to push test cost down

Cost per Transistor

manufacturing

testing

■ 1997 NTRS
National technology roadmap of semiconductor

▲ 2001 ITRS
International technology roadmap of semiconductor

Important Research Topics

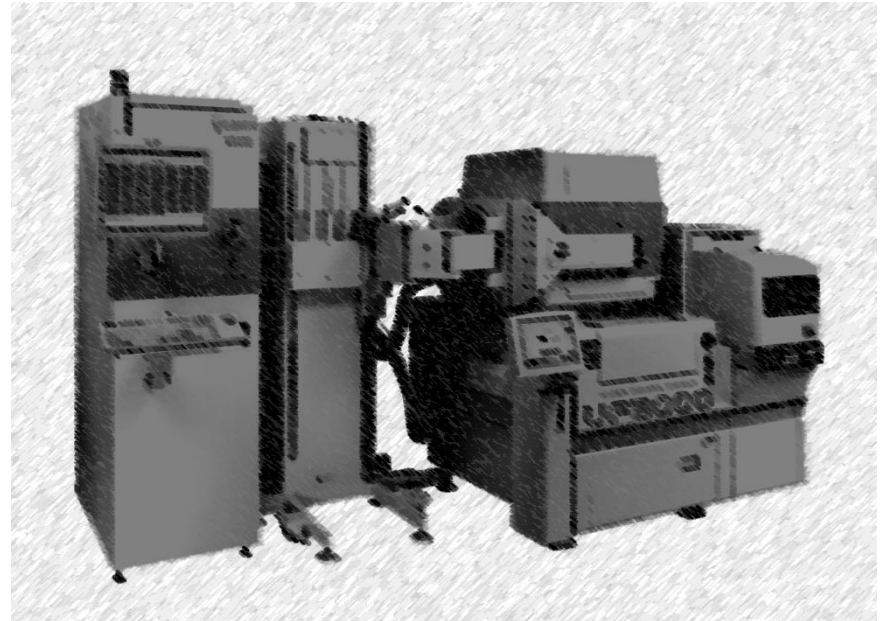- **Reduce test cost**
  - ♦ **Reduce test equipment cost**
    - ∗ *Built-in Self Test (BIST)*
  - ♦ **Reduce test data volume, test application time**
    - ∗ *Test compression, ATPG, Memory tests*
- **Improve test quality**
  - ♦ **Better *fault models, delay tests***
  - ♦ ***Design for testability (DFT)***
- **Improve yield**
  - ♦ ***Diagnosis***
- **Better/faster EDA tools**
  - ♦ **ATPG, Fault simulator, optimization algorithms**

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Major Conferences and Journals

- **International Conferences**
  - **IEEE Int'l Test Conference (ITC)**
  - **IEEE/ACM Design Automation Conference (DAC)**
  - **IEEE VLSI Test Symposium (VTS)**
  - **IEEE Asian Test Symposium (ATS)**
  - **IEEE European Test Symposium (ETS)**
  - **IEEE Design and Test in Europe (DATE)**
  - **IEEE Int'l Conference on CAD (ICCAD)**
- **Journals**
  - **IEEE Trans. On Computer-Aided Design (TCAD)**
  - **IEEE Trans. On VLSI Systems (TVLSI)**
  - **IEEE Trans. On Computers (TC)**
  - **ACM Trans. On Design Auto. of Electronic Systems (TODAES)**
  - **Journal of Electronic Testing : Theory and Application (JETTA)**
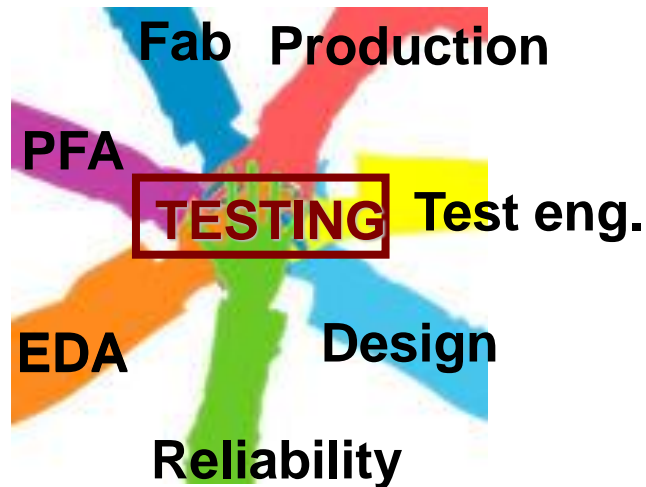- **IEEE Design & Test Magazine (D&T)**

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Conclusion

- **WHY test?**
  - It is **important to invest** in test because of **rule of ten**
- **HOW to test?**
  - Optimal test not only **technical issue**, but also **economics issue**
  - **No single best test solution for all products!**
- **WHO responsible?**
  - Testing is joint responsibility of **everybody**

Fab **Production**

PFA

TESTING **Test eng.**

EDA **Design**

Reliability

Without Testing, It Is a Gamble!

Testing Does, and Also Will, Play Very Important Role in High-tech Industry.

References

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- **[Davis 82] B. Davis, The Economics of Automated Testing. McGraw-Hill: London, UK**

- **[McCluskey 88] E.J. McCluskey ; F. Buelow, "IC quality and test transparency," Int'l Test Conf., 1988.**

- **[Williams 81] T. W. Williams, N. C. Brown, "Defect Level as a Function of Fault Coverage," IEEE Trans. on Computers, vol. C-30, no. 12, pp. 987-988, Dec.1981.**