



VLSI Testing

積體電路測試

Delay Test

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Course Roadmap (EDA Topics)

Logic Sim.

Fault Collapsing



Fault Simulation

Testability

Comb. ATPG



Diagnosis

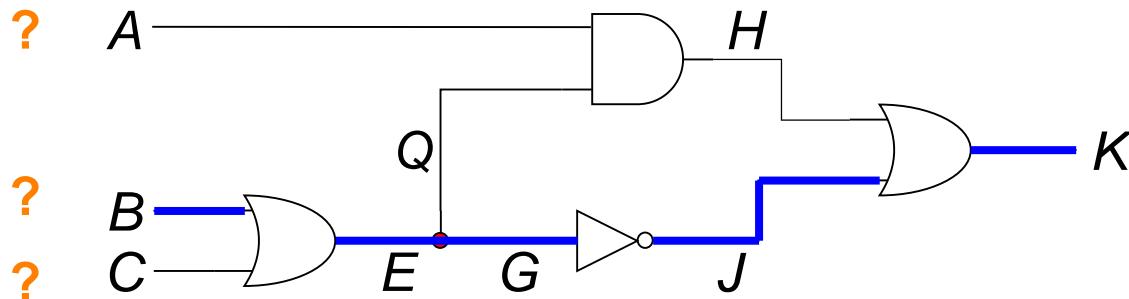
Seq. ATPG



Delay Test

Motivating Problem

- You already know stuck-at test very well.... but not enough
- Manager asks you to generate a test pattern to validate IC speed
 - ◆ make sure path BEGJK **timing** is correct



Why Am I Learning This?

- In this chapter, we learn :
 - ◆ Delay fault models
 - ◆ Generate test patterns for delay faults
 - ◆ Delay fault simulation

*“Delay always breeds danger
and to protect a great design
is often to ruin it.”*

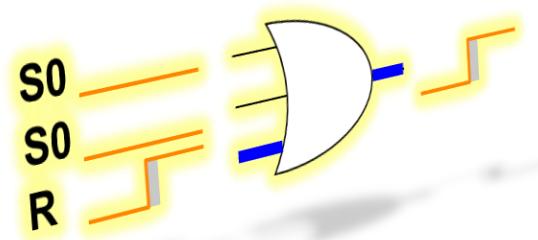
(Miguel de Cervantes)

Test Generation

Fault Models	Combinational Circuits (or Sequential ckt. with scan)	Sequential Circuits
No fault model	PET	Checking experiment
Single Stuck-at Fault Model	D PODEM FAN	Extended D 9-valued
Delay Fault Model	Path Delay Transition Delay	Launch on Capture Launch on Shift

Delay Test

- Introduction
 - ◆ What and why
 - ◆ Delay fault models: PDF, TDF
 - ◆ Comparison
- Path Delay Fault [Smith 85]
- Transition Delay Fault [Barzilai 83][Levendel 86]
- Experimental Results* (not in exam)
- Issues of Delay Tests* (not in exam)
- Conclusions



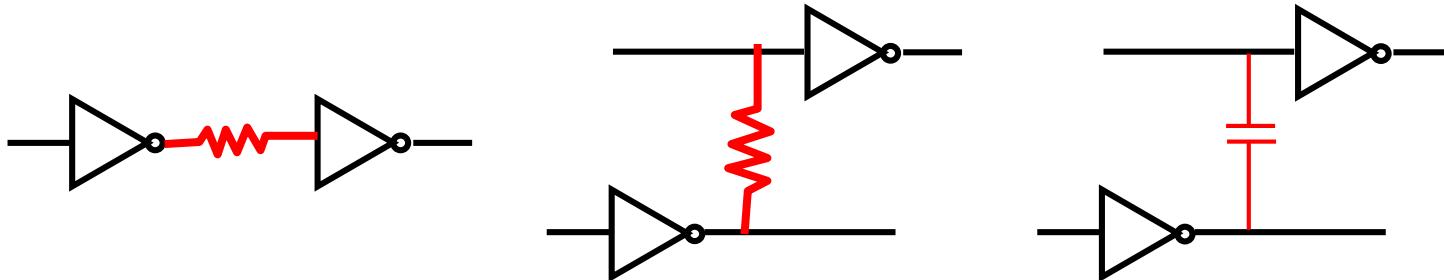
What is Delay Test ?

- ***Delay tests*** (aka. ***delay fault testing***) [Breuer 74]
 - ◆ Apply test patterns to detect ***delay faults***
- Functional verification test patterns can be applied at system speed
 - ◆ However, not enough to detect delay faults
- Delay test is also called ***AC test***
 - ◆ As opposed to ***DC test*** for stuck-at faults

Delay Test Detects Delay Faults

Why Delay Test?

- Some defects change circuit **timing** but not function
 - ◆ **Random defects:** Resistive opens, resistive bridging,
 - ◆ **Systematic defects:** crosstalk, process variation in V_t

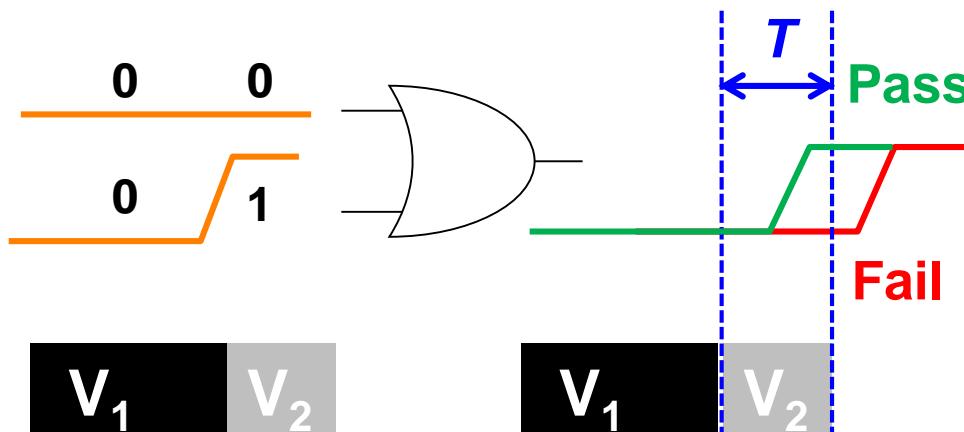


- IC becomes faster, ***small delay defects (SDD)*** become significant
 - ◆ 100 ps SDD
 - * only 1% for 100MHz clock period, insignificant
 - * but 10% for 1GHz clock period, **very significant**

Delay Tests Important for Advanced IC

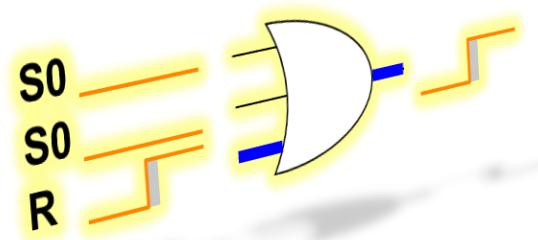
How Delay Test?

- Delay faults needs **two-pattern test**
 - ◆ As opposed to **one-pattern** test for stuck-at faults
- A two-pattern test consists of a pair of test patterns (**test vectors**)
 - ◆ V_1 : initialize circuit state
 - ◆ V_2 : **launch** transition, **propagate fault effect** to output
- Control timing (T) between V_1 and V_2 carefully
 - ◆ If T is as fast as system operation, this is called **at-speed testing**



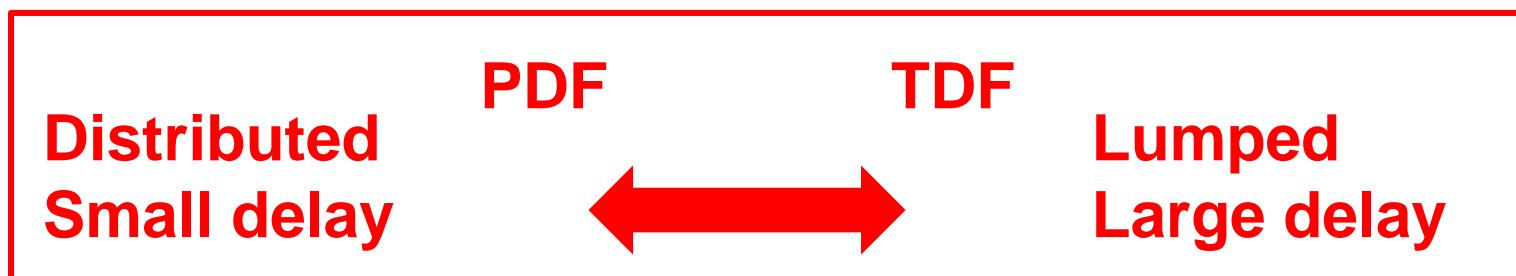
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Two Delay Fault Models

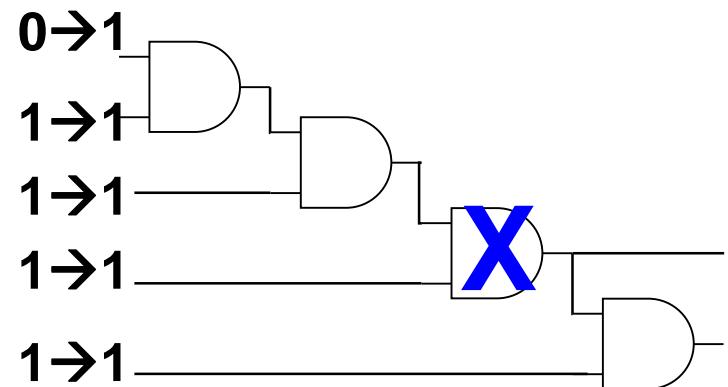
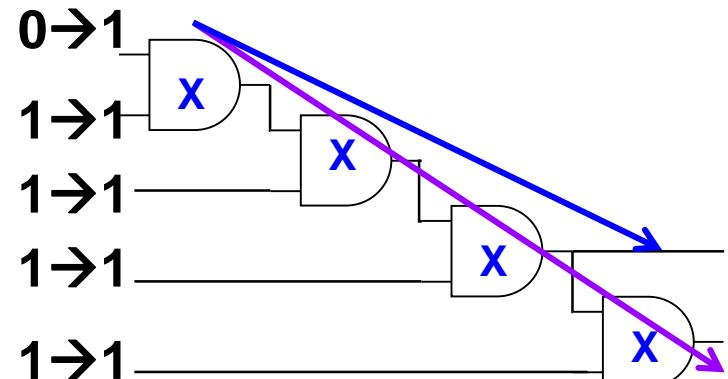
- **Path Delay Fault, PDF** [Smith 85]
 - ◆ Path delay of the faulty path > clock period
- **Transition (Delay) Fault, TDF** [Barzilai 83] [Levendel 86]
 - ◆ Path delay of all paths through the fault > clock period
- Other delay fault models
 - ◆ Gate delay fault [Iyengar 88]
 - ◆ Segment delay fault [Heragu 96]
 - ◆ ...



Example

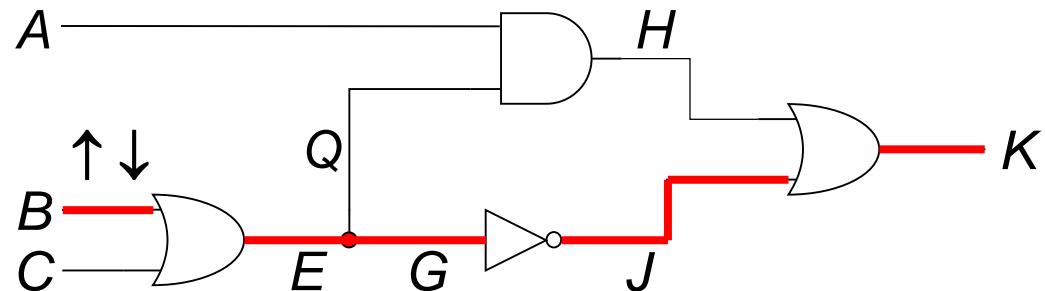
- Clock period = 10.0ns, good gate delay = 2.0ns
- For good circuit
 - ◆ short path delay = 6.0ns
 - ◆ long path delay = 8.0ns
- PDF (fault distributed along path)
 - ◆ $\underline{3.0} + \underline{2.6} + \underline{2.7} = 8.3 < 10 \rightarrow \text{pass}$
 - ◆ $\underline{3.0} + \underline{2.6} + \underline{2.7} + \underline{2.9} = 11.2 > 10 \rightarrow \text{fail}$
- TDF (lumped fault = 9.0 ns)
 - ◆ $2.0 + 2.0 + 2.0 + \underline{9.0} = 15.0 \rightarrow \text{fail}$
 - ◆ $2.0 + 2.0 + 2.0 + \underline{9.0} + 2.0 = 17.0 \rightarrow \text{fail}$

fault size = extra delay caused by fault

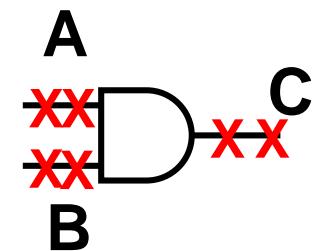


Number of Delay Faults

- PDF: Two path delay faults for each path
 - ◆ Rising (notation \uparrow) Falling (notation \downarrow)
 - ◆ Example: two PDF
 - * BEGJK \uparrow, \downarrow



- NOTE: Number of paths is worst-case **exponential** to gate count
- TDF: Two faults for each node
 - ◆ Slow-to-rise (STR) fault; Slow-to-fall (STF) fault
 - ◆ Example: six TDF in AND
 - * A STR, A STF, B STR, B STF, C STR, C STF
 - ◆ NOTE: Number of faults is **linear** to gate count



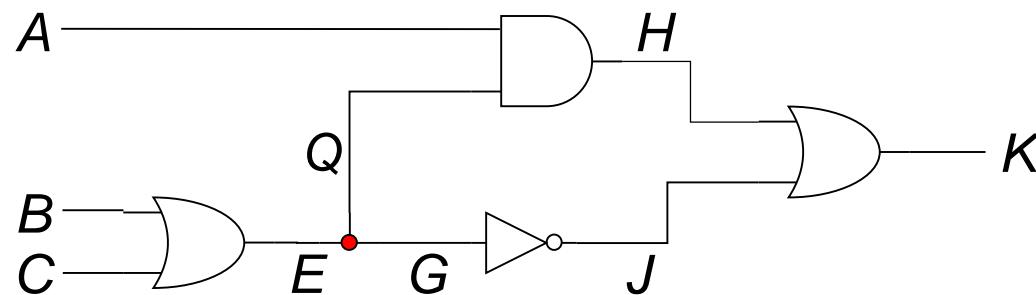
Quiz

Q1: How many PDF in this circuit?

A:

Q2: How many TDF in this circuit?

A:



Comparison: PDF vs. TDF

	Path Delay Fault	Transition Delay Fault
Number of faults	😢 WC exponential (need path list)	😊 linear
Fault size and distribution	😊 small delay faults 😊 distributed	😢 large delay faults only 😢 lumped
Silicon speed Validation	😊 useful	😢 not useful
ATPG	😢 less mature tool 😢 FC not high	😊 mature ATPG 😊 FC very high

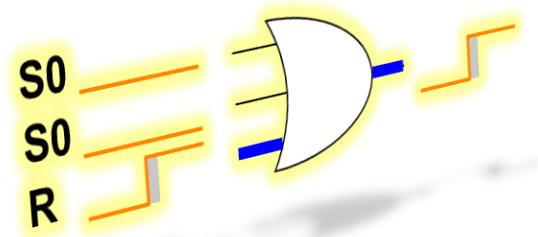
General definition
Difficult for ATPG



Specific definition
Easier for ATPG

Summary

- Introduction and delay fault models
 - ◆ PDF assumes distributed fault
 - * Worst-case exponential in numbers, difficult for ATPG
 - ◆ TDF assume lumped fault
 - * linear in numbers, easiest for ATPG
- Path Delay Fault
- Transition Delay Fault
- Delay Test Application
- Circuit Model for Delay Test ATPG
- Experimental Results* (not in exam)
- Issues of Delay Tests* (not in exam)
- Conclusions



FFT

- Number of paths is worst-case exponential to number of gates
 - ◆ Q: why? Please give an example

