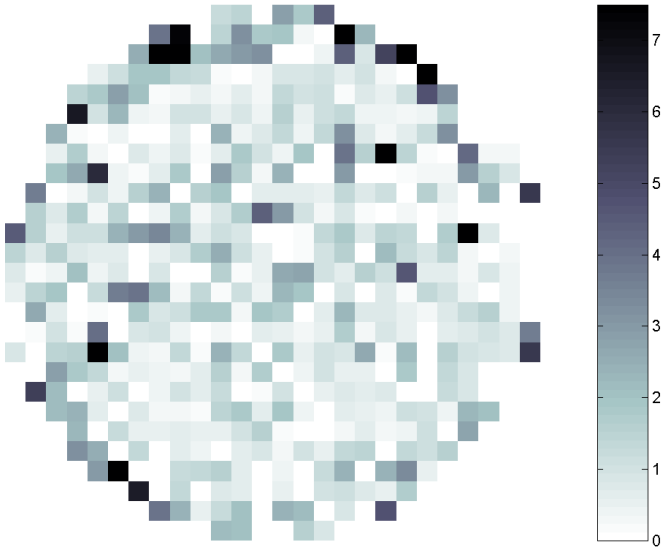
Advanced Topics: DBT

- Introduction
- Defect-based Testing
  - VLV Testing (1982)(Stanford 1993)
  - IDDQ Testing (1981)
- Advanced ATPG
- Conclusion



Introduction

- What is *Defect Based Testing* (DBT)
  - Testing without specific fault model involved
  - Aims to educes DPM (and also reliability defects)
- Why Defect Based Testing?
  - Defects do not always behave as faults
  - 100% fault coverage is not good enough
- Popular DBT techniques:
  - *Very low voltage (VLV) testing*
    - Example : Gate oxide short defects
      - Pass nominal V_{DD} by fail at low V_{DD}
  - *IDDQ testing*
    - Example : High impedance bridging defects
      - Cause abnormal static current but pass Boolean test

Test Escape vs. Yield Loss

- *Test escapes* = defective chips that pass test
- *Yield loss* = good chips that fail the tests
- Goal of DBT: reduce test escape
- Side effect of DBT : increases yield loss

	Good chips	Defective chips
Pass tests	True PASS	Test Escapes
Fail tests	Yield Loss	True Reject

DBT Trades-off between Test Escapes and Yield Loss

Very-Low Voltage (VLV) Testing [Ager 82][Hao 93]

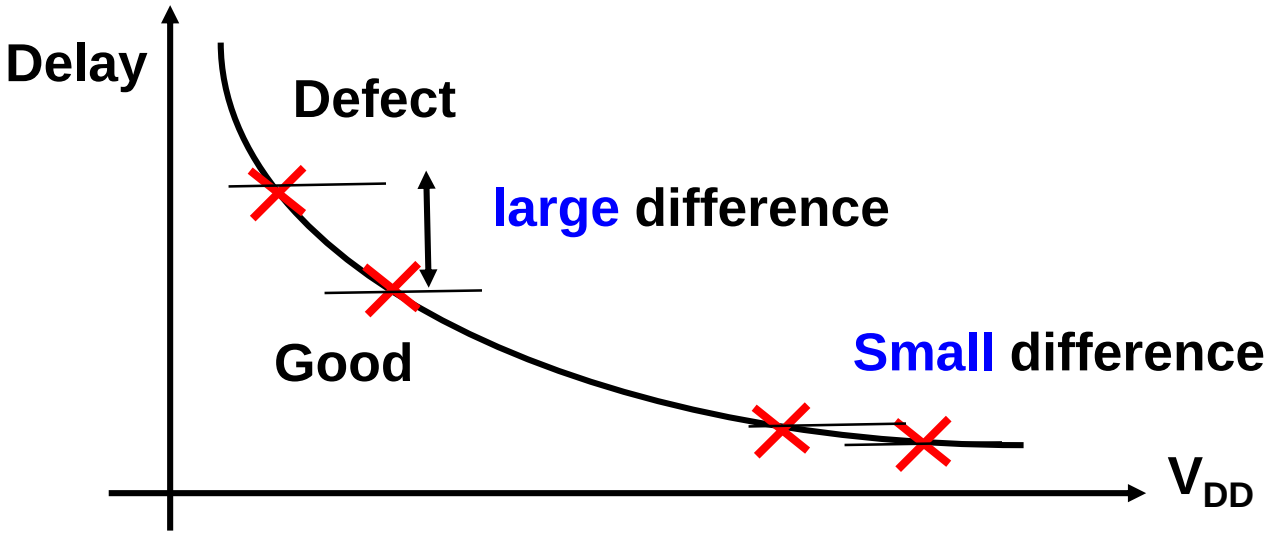
- **Definition**
  - **Boolean tests performed at V_{DD} much lower than nominal V_{DD}**
  - **as low as 2 to 2.5 times V_t [Chang 96]**

- **Important notes about VLV:**
  - **Not just a little lower (e.g. 10%) than nominal V_{DD}**
    - **Do not confused with characterization test**
  - **Test voltage and speed need careful characterization**
    - **Large variation at low V_{DD}**
    - **Aggressive voltage or speed could result in yield loss**

VLV is Complement to,
NOT Replacement for, Nominal V_{DD}

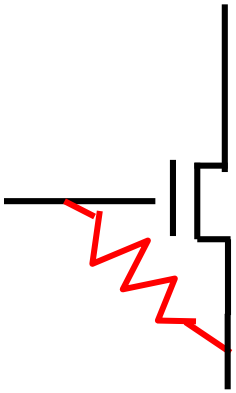
Idea of VLV

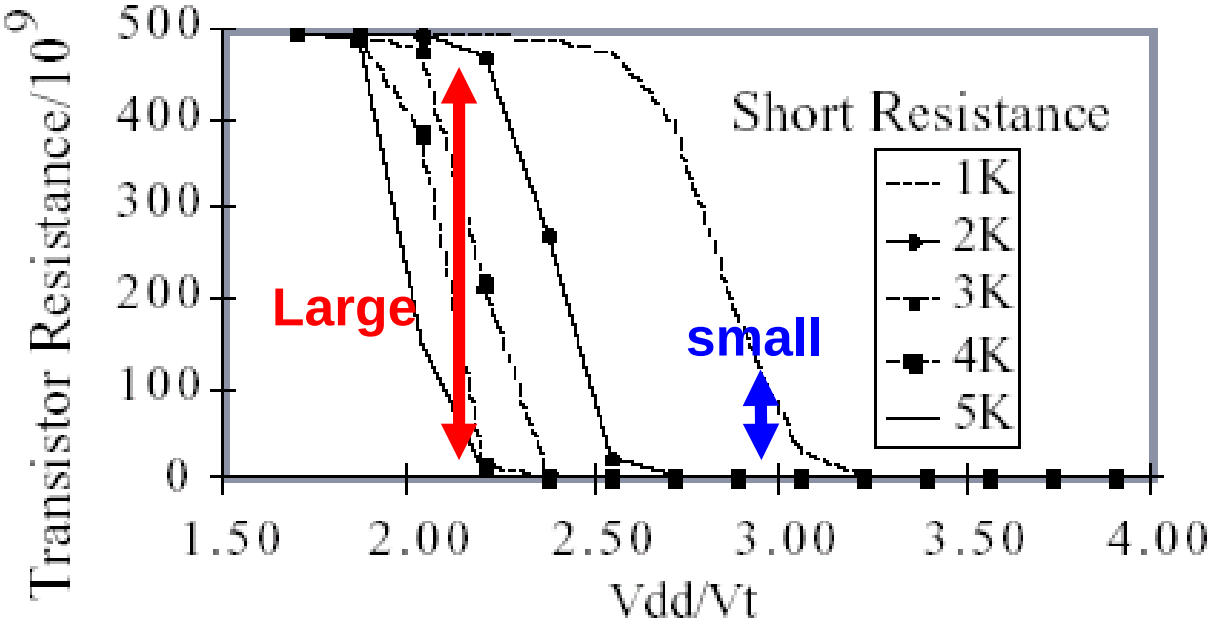
- Idea
  - Difference between good and bad chips magnified at lower V_{DD}
- Example:
  - Gate oxide shorts
  - Difference in delay can be magnified by VLV testing

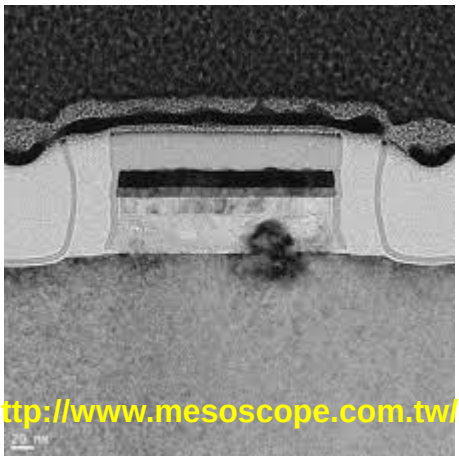


Gate Oxide Shorts

- Transistor turn-on resistance (R_{on})
  - Not very different at nominal voltage
  - Very different at VLV
- Simulation results from [Chang 96]





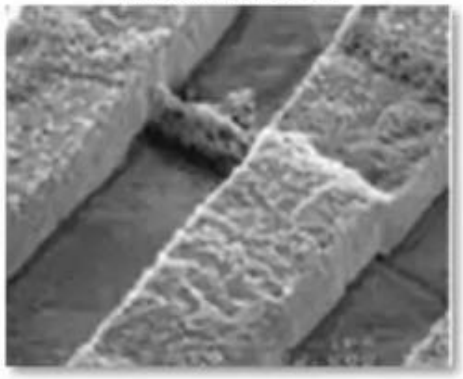


Defects Potentially Detectable by VLV

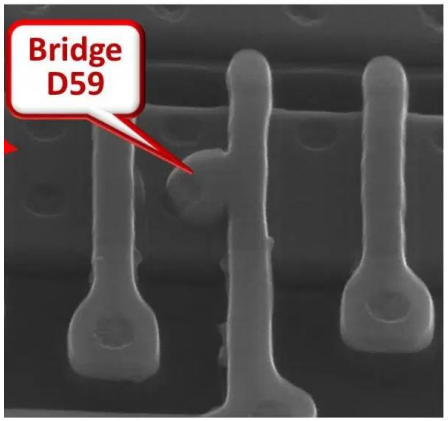
- Shorts/bridging
  - Gate oxide shorts
  - Metal
- Weakly driven gates
  - Signals fail to reach full swing
- V_t shift
- Transmission gate opens
- Tunneling opens [Li 00]

*These photos are for illustration only.

Metal short



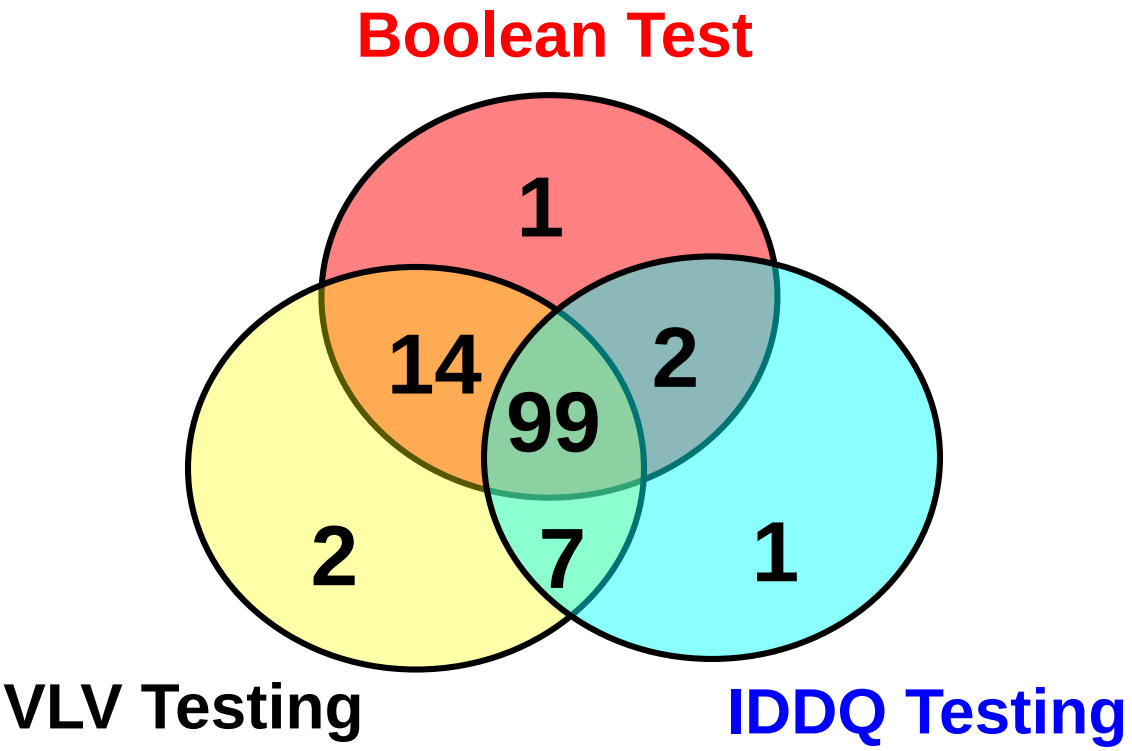
D. Payne (Synopsys), "Catching IC Manufacturing Defects With Slack-Based Transition Delay Testing", SemiWikli.com, 2014



P. Maxwell, et.al, "Cell-Aware Diagnosis: Defective Inmates Exposed in their Cells", European Test Symposium (ETS) 2016

Experimental Results

- Stanford Murphy experiment [McCluskey 00]
- Totally 5.5K chips tested
  - 116 chips failed nominal voltage Boolean test
  - 9 chips failed VLV testing only, pass nominal V_{DD} testing



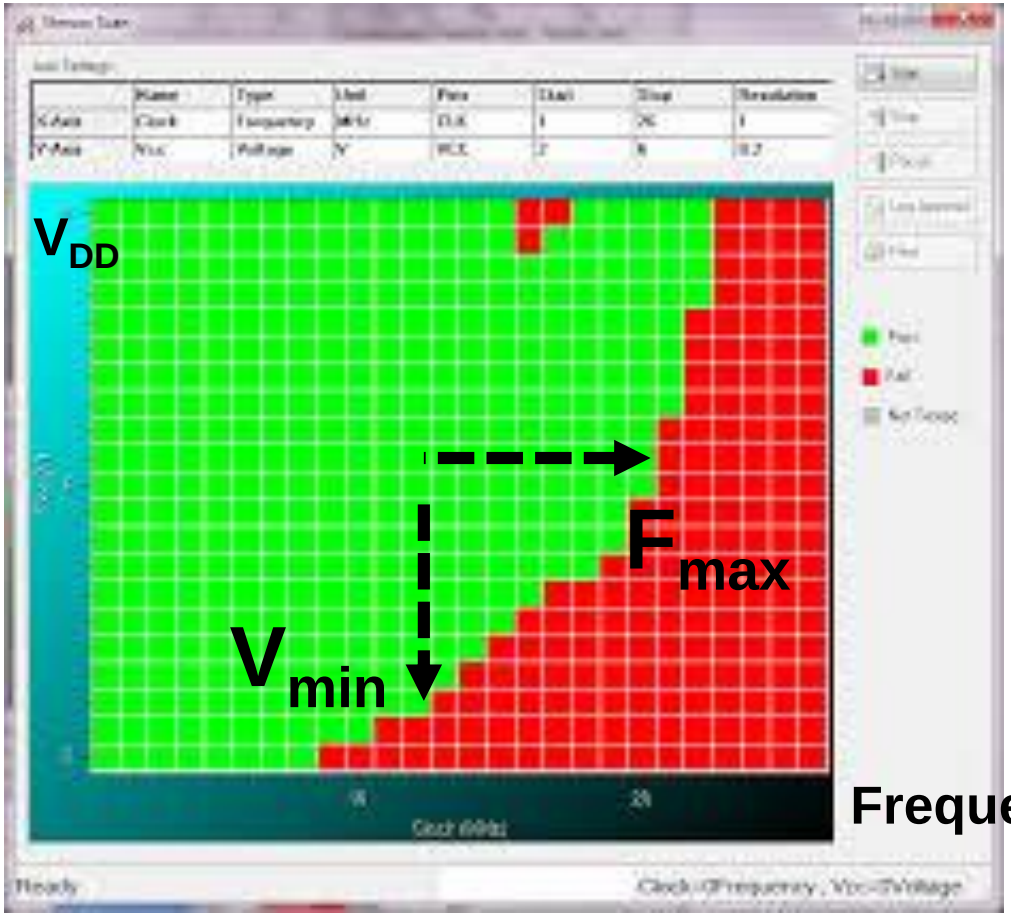
Problems with VLV

- Nominal voltage keep dropping in advanced technologies
  - No room for lowering V_{DD}
- Test voltage and test speed need careful characterization
  - Large variation at low V_{DD}
- Detect any reliability problems?
  - 5.5K chips tested, 9 failed VLV-only chips
    - 7 passed burn-in [Li 00]
  - Need more data to verify

VLV Needs Careful Characterization and Verification

Other Similar DBT Techniques

- V_{min}
  - Measure the lowest operational V_{DD} at specified frequency
- F_{max}
  - Measure maximum frequency at specified voltage



Example Shmoo Plot

Requires Long Test Time to Search

Quiz

Q: Which of following is NOT correct ?

A: VLV could potentially detect defects not detectable at nominal V_{DD}

B: DBT tries to improve DPM, not fault coverage

C: VLV testing can replace traditional SSF testing

Conclusion

- **Defect-based Testing (DBT) reduces DPM**
  - **Focus on defects, not faults**

- **Very low Voltage Testing**
  - **Boolean testing applied at much lower V_{DD}**
  - **Magnify difference between good and weak chips**
  - ☺ **Potentially detects defects that may escape nominal V_{DD} tests**
  - ☹ **Test voltage and test speed needs careful characterization**

- **Other similar DBT**
  - **V_{min}, F_{max}**

DBT Becomes Important for Automobile Electronics

References

- [Ager 82] D. Ager, “The application of marginal voltage measurements to detect and locate defects in digital microcircuits,” Microelectronics Reliability, 1982.
- [Chang 96] J. Chang, EJ McCluskey, “Quantitative analysis of very-low-voltage testing,” VLSI Test Symp, 1996.
- [Hao 93] H. Hao, E.J. McCluskey, “Very-low-voltage testing for weak CMOS logic Ics,” Int’l Test Conf. 1993.
- [Li 00] J. C. M. Li and E. J. McCluskey, "Testing for tunneling opens," Proceedings International Test Conference 2000, pp. 85-94.
- [McCluskey 00] E. J. McCluskey and C. W. Tseng, "Stuck-fault tests vs. actual defects," Int’l Test Conf., 2000.