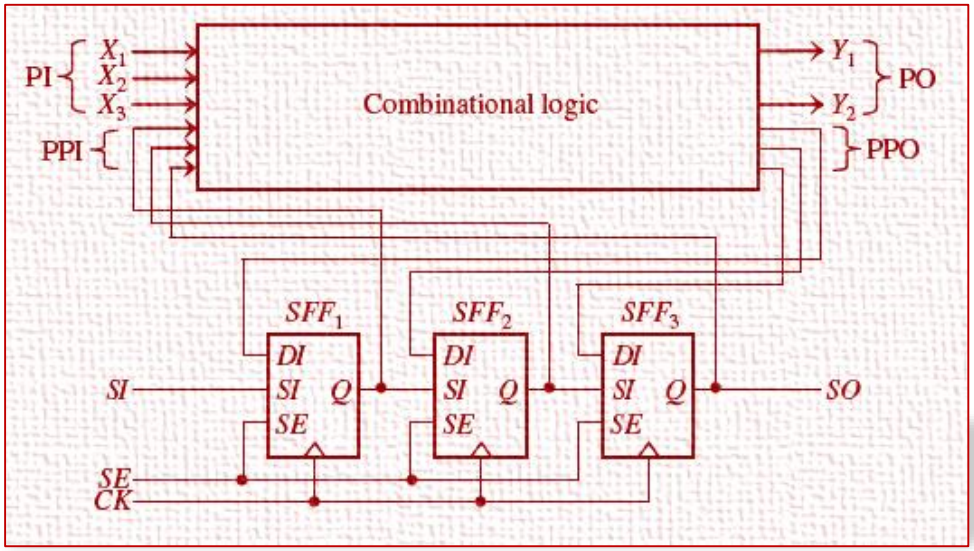
DFT - Part 1

- Introduction
- **Internal Scan**
  - FF-based
    - MUXed-D scan (1973, Stanford)
    - Clocked scan (1968, NEC)
  - Latch-based
    - LSSD (1977, IBM)
- Scan Design Flow
- Issues and Solutions
- Conclusion



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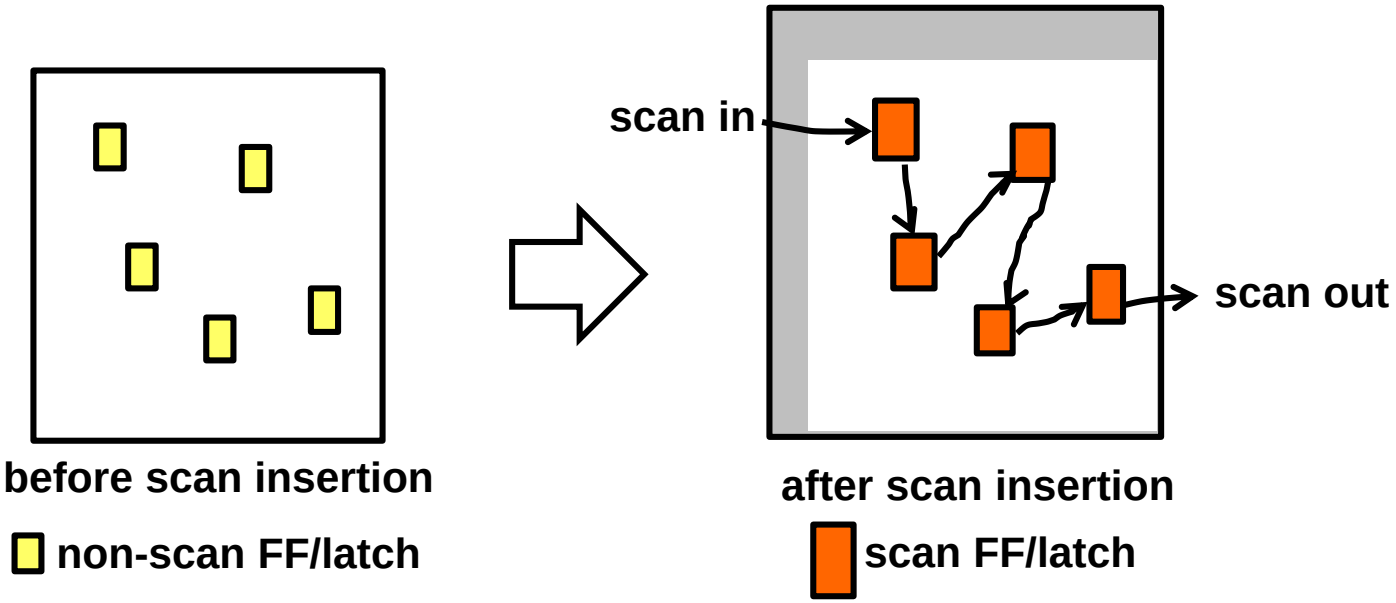
Scan Chains

- Scan: connect (internal) FF/latches as shift register
  - Control and observe FF/latches in test mode
  - Remain original function in normal mode
- Proposed in early 1970's [Williams 73][Eichelberger 77]
  - Most important DFT for synchronous digital circuits
- *Scan chain insertion*: aka. *DFT insertion*, *DFT synthesis*
  - 1. Replace FF/latch 2. Stitch FF/latch into a chain



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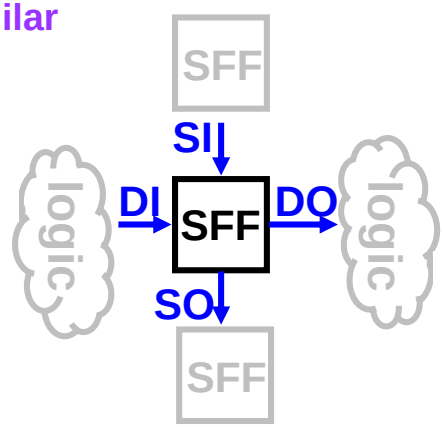
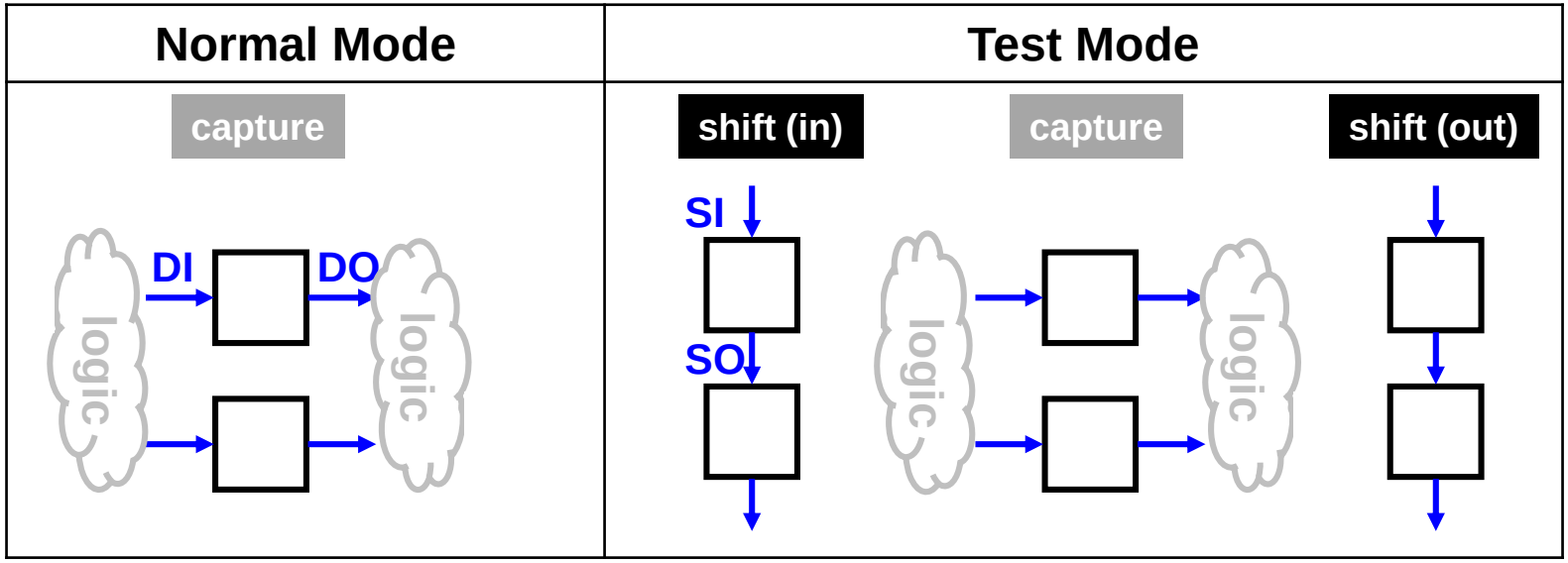
Scan Flip-Flop (SFF) *scan latch is similar



- SFF has four main pins:
  - Scan Chain: *Scan Input* (SI), *Scan output* (SO)
  - Logic: *Data Input* (DI), *Data Output* (DO)
    - DO and SO can be shared
- SFF has two functions: *shift* and *capture*
- Circuit has two operation modes: *Normal* mode and *Test* mode



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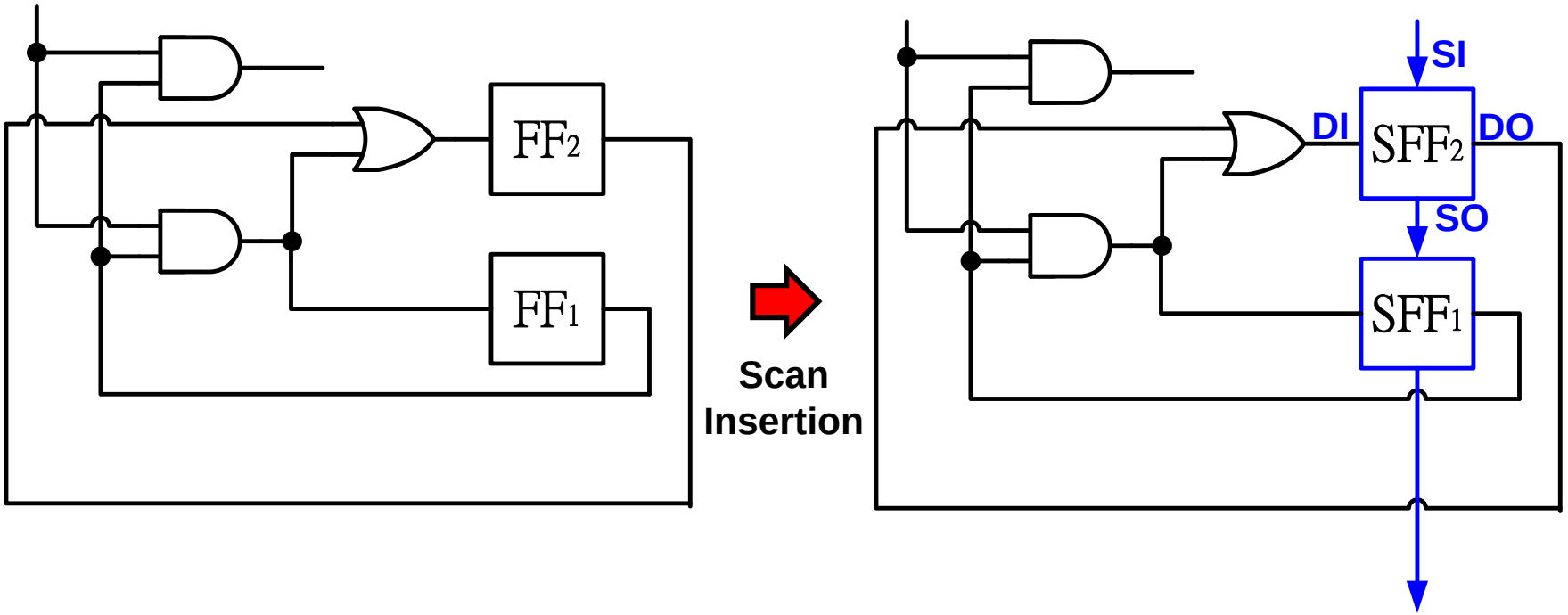
Example: Scan Insertion



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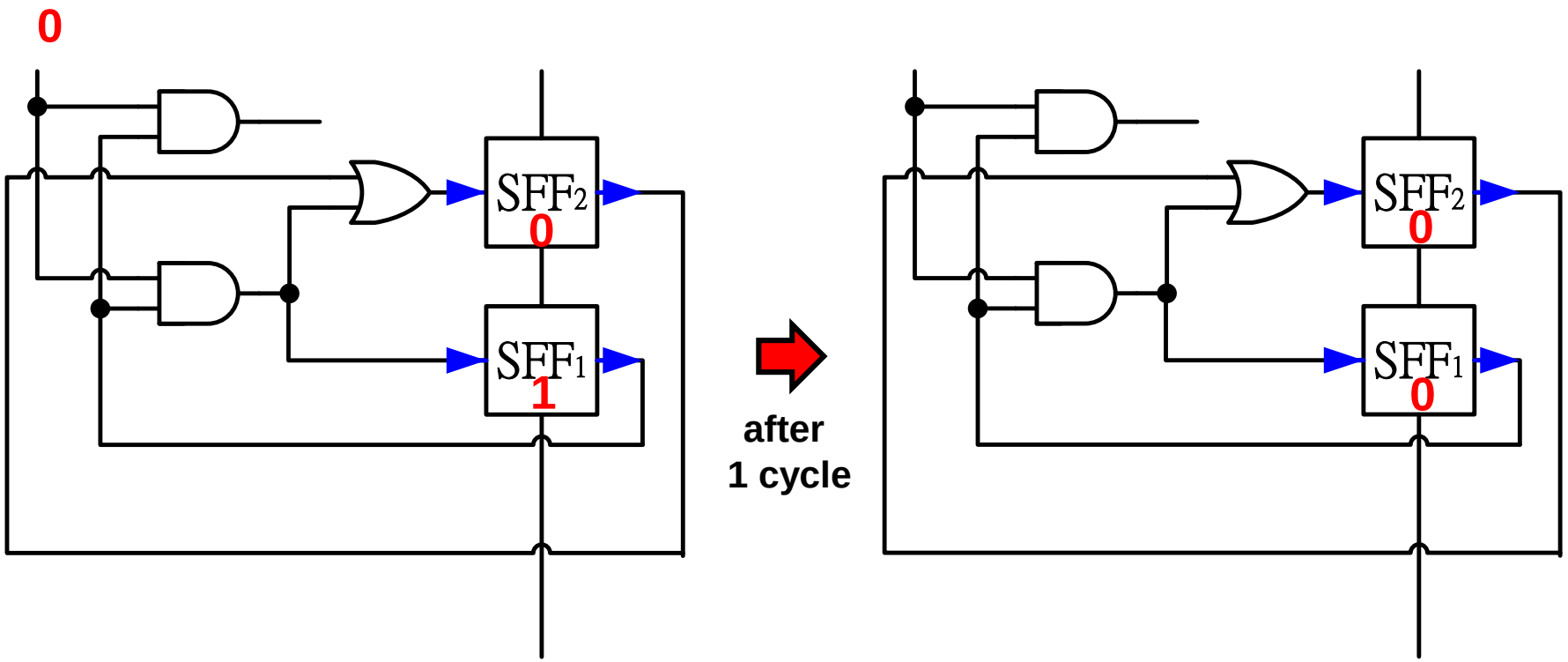
Example: Normal Mode

- **Scan-FF same as non-scan FF**



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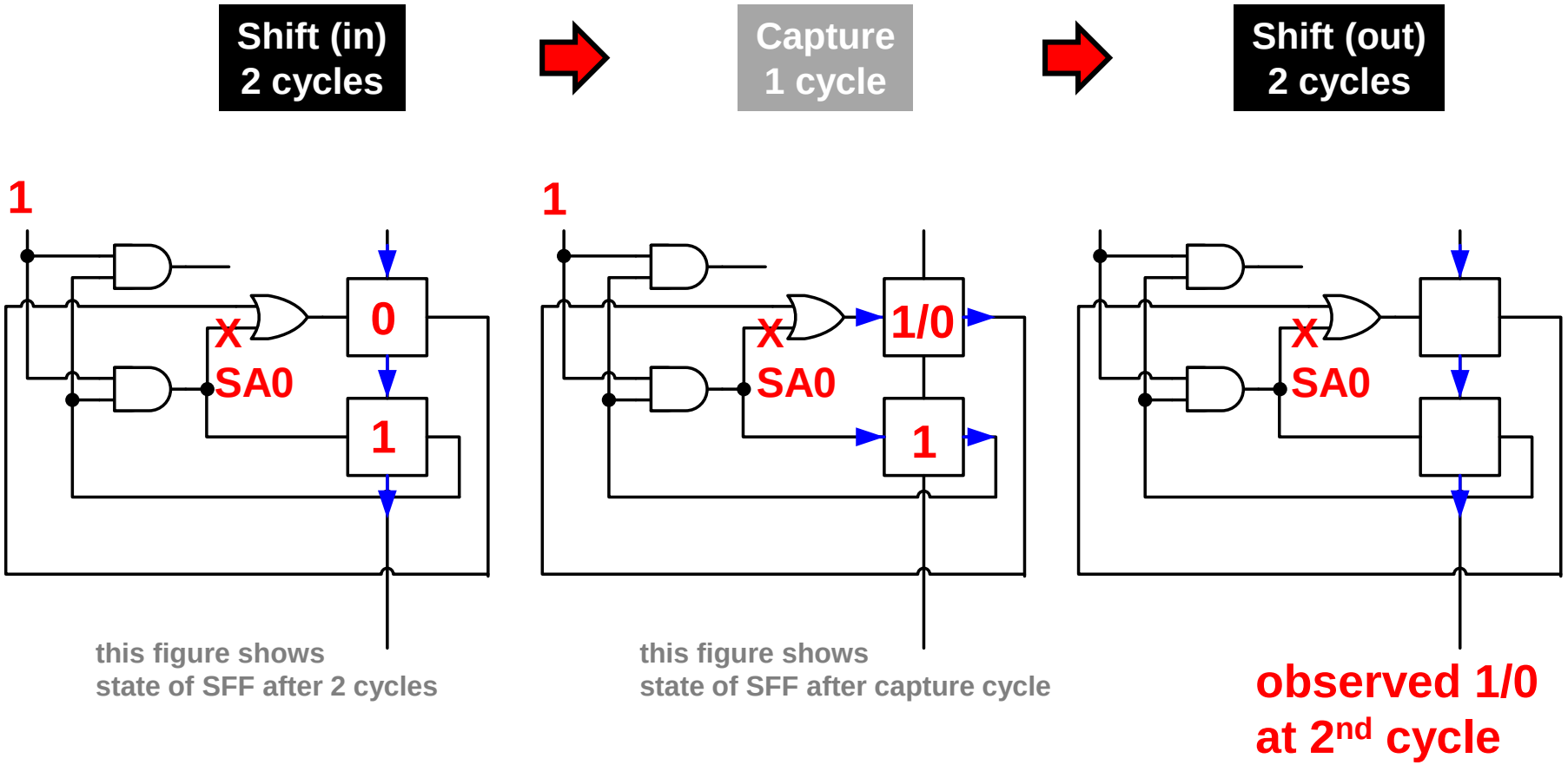
Example: Test Mode



Fault Detected in Test Mode

NOTE: this fault untestable in Normal Mode. why?

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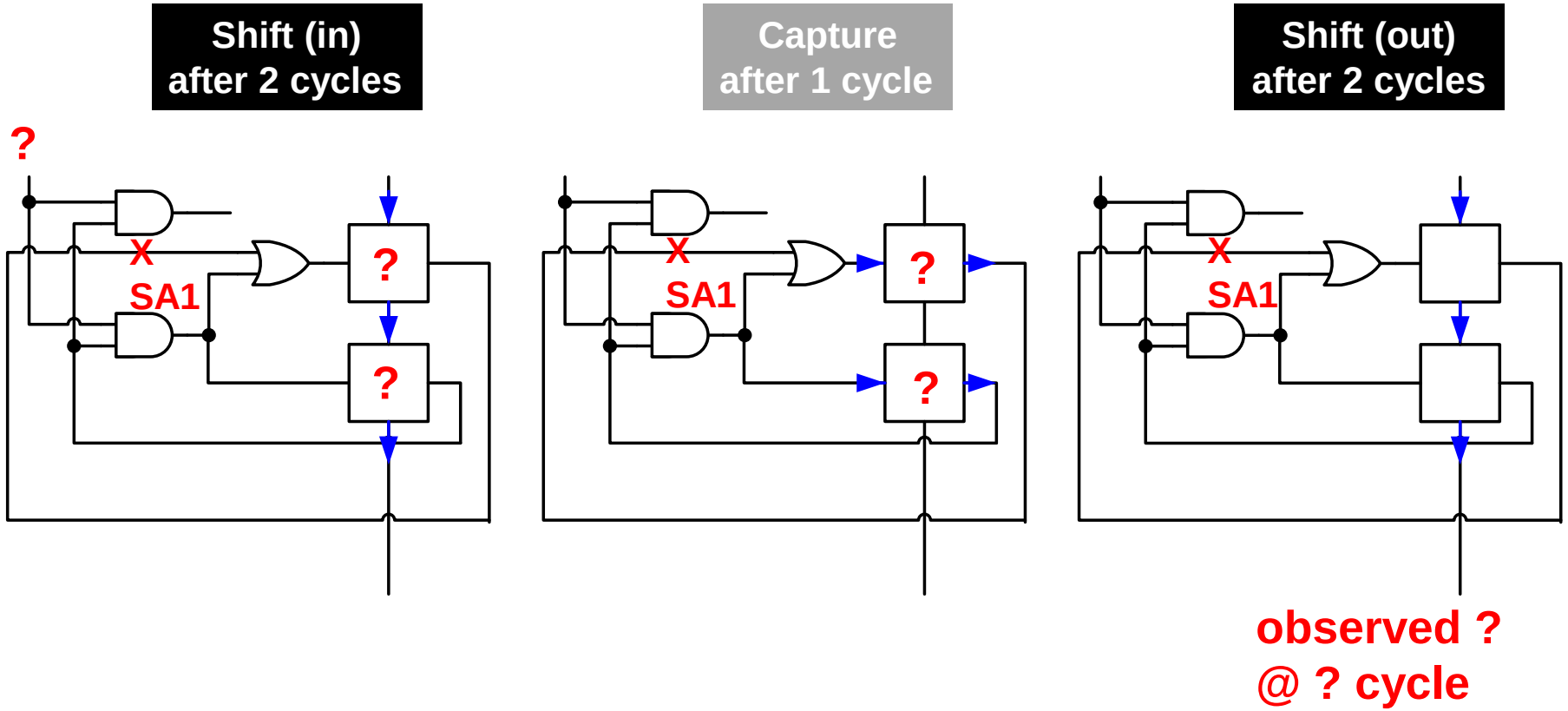
Quiz

Q: Consider SA1 fault, please fill in values of ?



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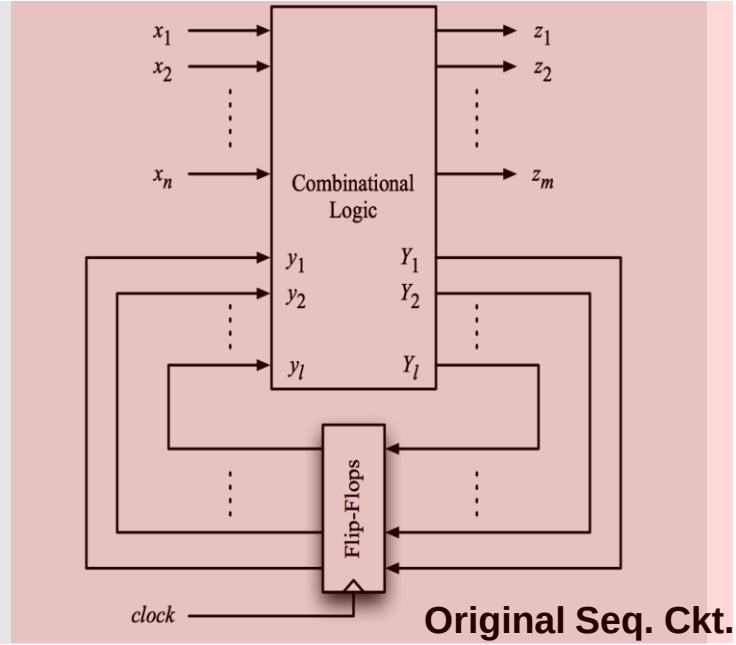
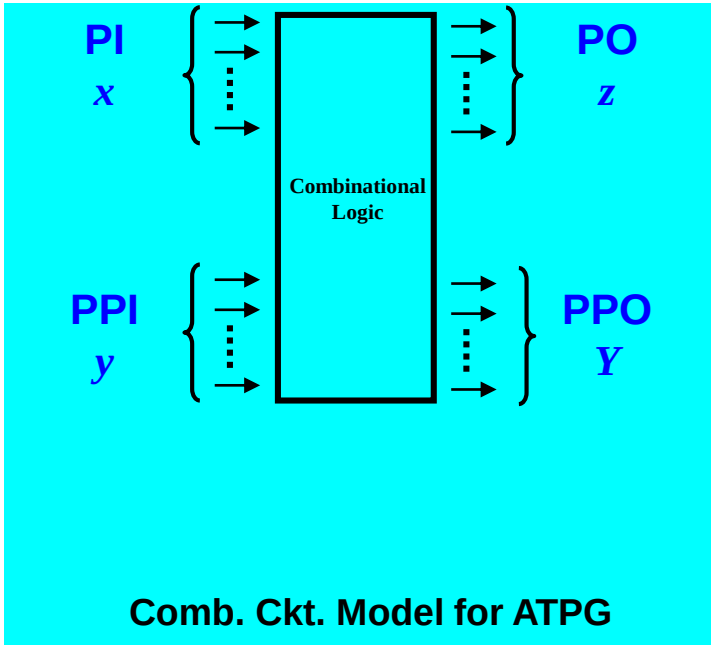
Scan Turns Seq. Ckt. to Comb. Ckt.

- Scan turns sequential ckt into combinational ckt in test mode
  - ATPG sees only comb. ckt. model
- SFF DO become *Pseudo Primary Input* (PPI), fully controllable
- SFF DI become *Pseudo Primary Output* (PPO), fully observable





Scan Makes ATPG Easier!

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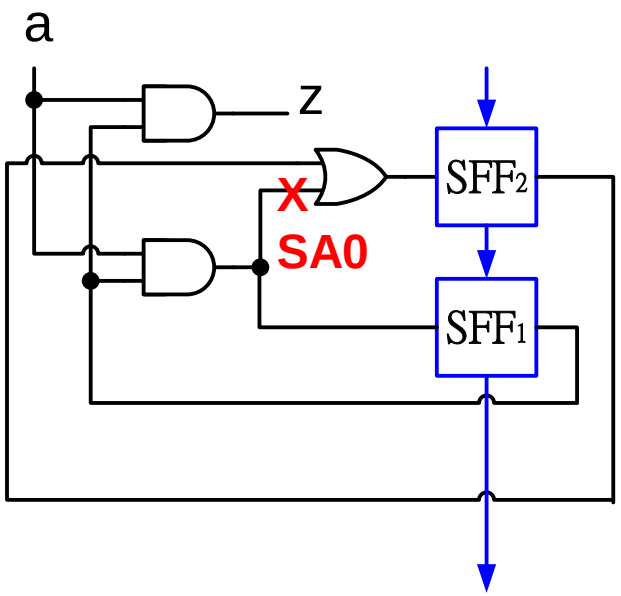
QUIZ

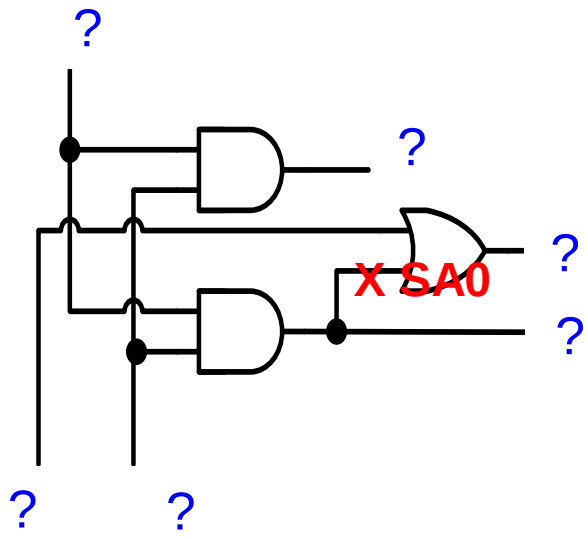
We insert scan into this circuit so we can remove FF in ATPG model.

Q1: Which pins are PI? PO? PPI? PPO?

Q2: If we want to detect SA0 fault, what are their values?

ANS:





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Pros and Cons of Scan

- Advantages of scan
  - Systematic DFT, not *ad hoc.* Many automatic tools.
  - Easy ATPG: faster run time and higher fault coverage (see 11.4)
  - Easy *silicon debugging* or *diagnosis*
- Disadvantages of scan
  - Area overhead (typically, 5~10% OH acceptable)
    - larger SFF area + routing for scan chains
  - Performance overhead
    - SFF has longer setup time, hold time
  - Pin overhead
    - scan in, scan out, *scan enable*, *scan clocks* … (11.3, 11.5)
  - Power overhead
  - Extra design efforts
    - scan insertion, verification (11.7, 11.8)

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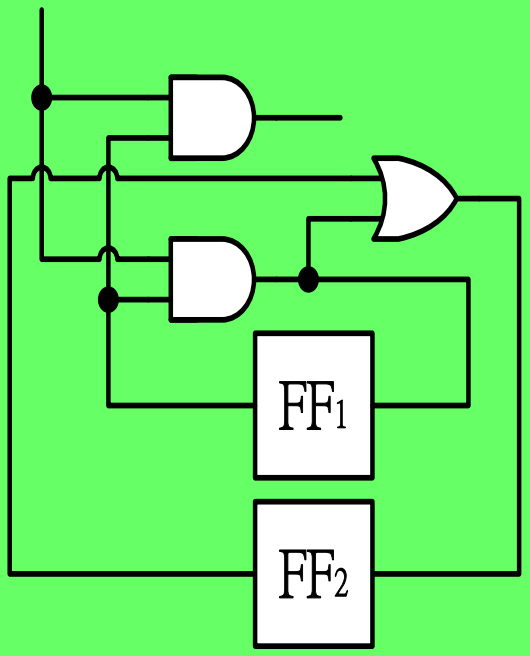
QUIZ

We insert scan into this circuit and replace non-scan FF by scan FF.

Q: Given the gate area table, what is area overhead of scan DFT?



Gate	area
OR	3
AND	3
non-scan FF	5
scan FF	6

ANS:

$$\text{area O.H.} = \frac{\text{area}_{afterDFT} - \text{area}_{beforeDFT}}{\text{area}_{beforeDFT}} =$$

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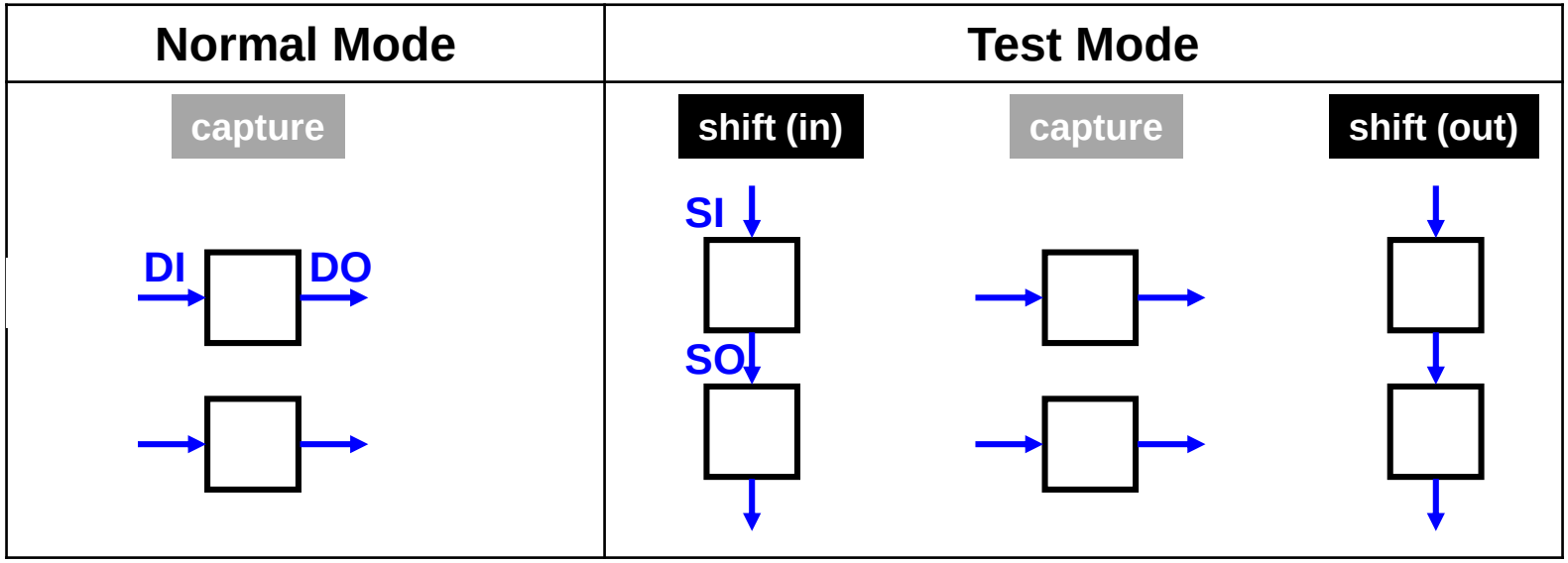
Summary

- Scan is most popular DFT for digital VLSI
- Scan FF has four pins: SI, SO, DI, DO
- Circuit has two operation modes: normal mode, test mode
  - Test mode: shift (in), capture, shift (out)
- Scan makes ATPG easier at cost of overhead (area/performance …)



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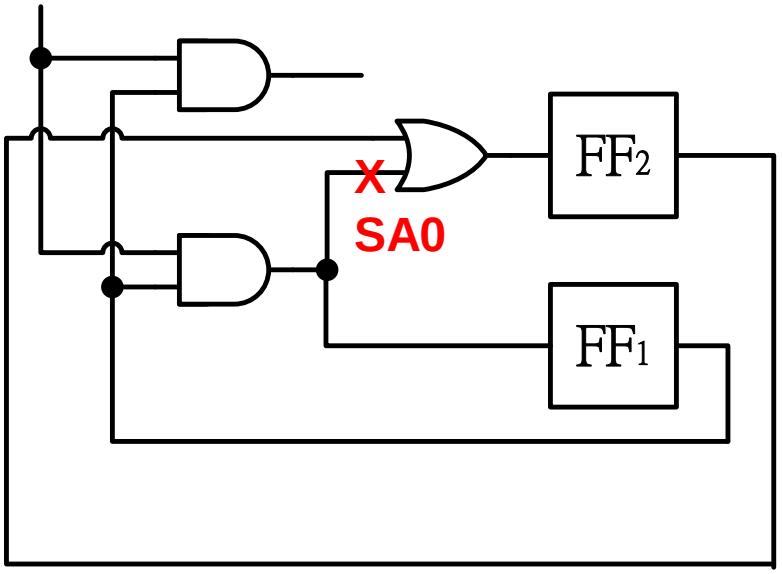
FFT

- **Q1: This stuck-at zero fault is untestable in normal mode, why?**
- **Q2: Since it is untestable in normal mode, why do we care about it?**



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