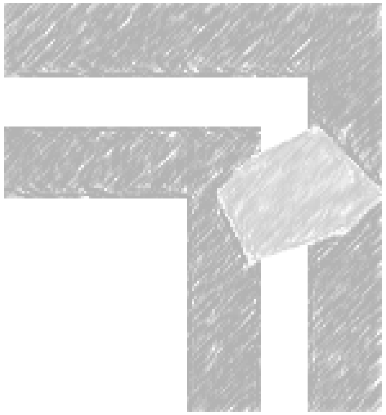
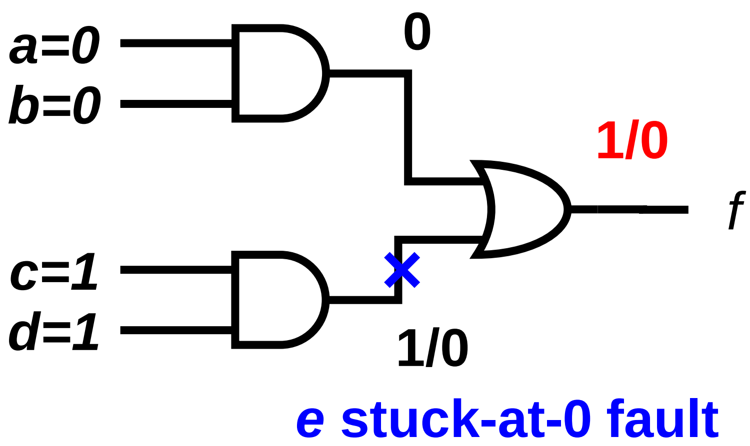
Fault Modeling

- Introduction
- Fault Models
- <u>Fault Detection</u>
- Fault Coverage
- Conclusion



Fault Detection

- A test pattern ***detects*** a fault if
  - output of faulty circuit $\neq$ output of good circuit



f = ab + cd

test pattern (a,b,c,d) = (0,0,1,1)

detects *e* stuck-at-0 fault

notation 1/0:
good value=1; faulty value =0

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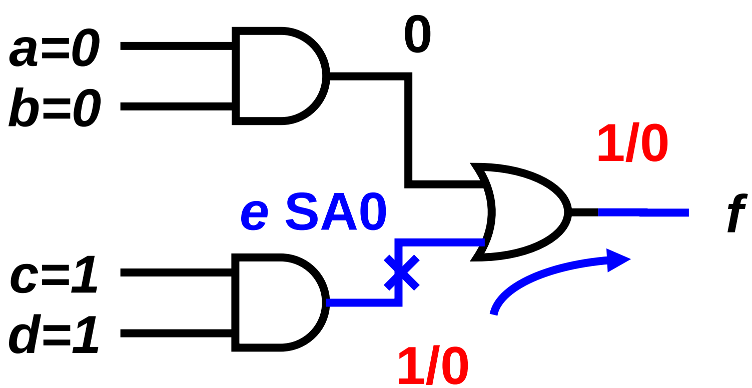
Activation & Propagation

- A fault is detected if two conditions are satisfied
  - (1) *Fault activation*:
    - different value at *fault site* (opposite to faulty value)
  - (2) *Fault effect propagation:* (aka. *error propagation*)
    - Propagate *fault effect* to any primary output
    - Signal *x* is *sensitized* if output changes when *x* changes
    - A path of sensitized signals is called *sensitized path*



Fault activation: *c=d=1*
Fault Effect Propagation*:* *a=b=0*
e is sensitized to output
e-f is sensitized path

Detection Requires (1) Activation & (2) Propagation

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Fault Classes

- *Untestable faults*[*] = faults that cannot be detected by any test pattern

- *Testable faults* = faults that cannot be proven untestable
  - Detected faults
  - Undetected faults
  - Oscillatory faults (see fault simulation)
  - Potentially detected faults (see fault simulation)
  - …

* *untestable* faults is aka. *undetectable faults*
but very confusing so not used in lecture

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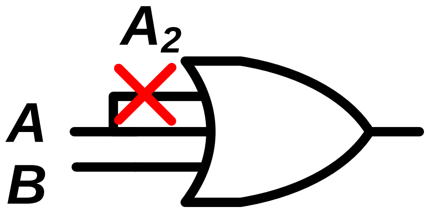
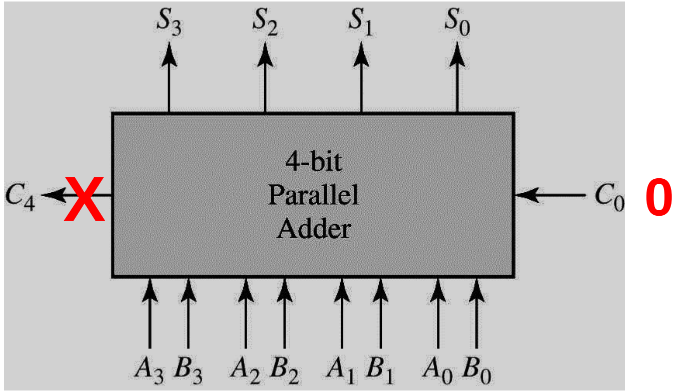
Untestable Faults

- Definition
  - Faults that cannot be detected by any test pattern (proven)
  - Aka ***redundant faults***
- Proving untestable fault is *NP-complete*
  - same as ***satisfiability (SAT)***
- Examples of untestable faults
  - 1. Redundant circuitry
    - *A_2* stuck-at zero fault is untestable



  - 2. Unused output or tied input
    - C_4 is not used
      - SA0,SA1 untestable
    - C_0 is tied to zero
      - SA0 untestable



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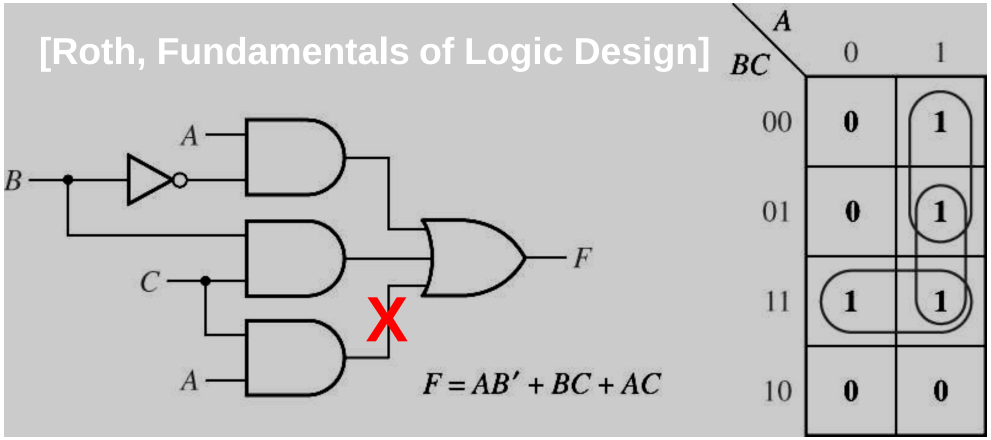
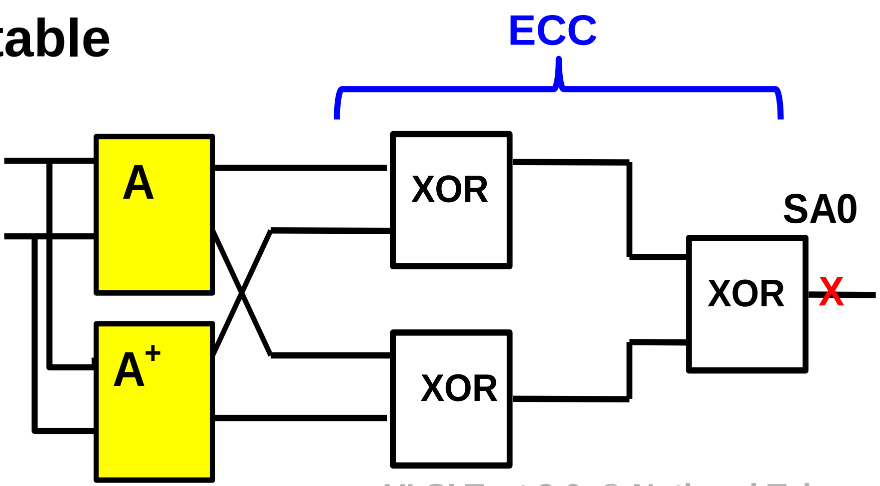
Untestable Faults (2)

- **3. Hazard control circuitry**
  - **AB’ + BC + AC = AB’+BC**
  - **AC SA0 is untestable**
  - **Used for hazard prevention**



- **4. Error control circuitry**
  - **A and A^+ always produce same output**
  - **ECC output SA0 is untestable**

- **5. ATPG constraints**
  - ***e.g.* set PI=1**



Undetected Faults

- Definition
  - Faults that are not detected by the given test set
- Due to ATPG runtime limitation
  - Cannot prove it untestable
  - Cannot find test pattern, either

- NOTE: do not confuse *untestable faults* with *undetected faults*
  - Former: no test pattern exists (proven)
  - Latter: no test pattern so far (may exist but not sure)

Untestable Faults ≠ Undetected Faults

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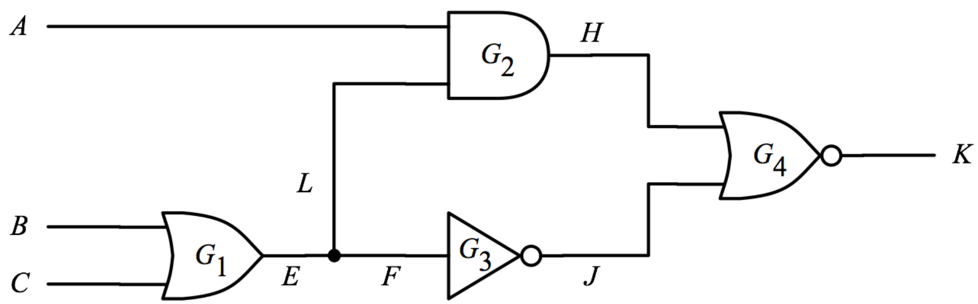
Quiz

Q1: Apply two patterns {000, 001}. Which fault (s) are undetected?
A:
Q2: Now consider all patterns. Which fault(s) are untestable?
A:



Input			Output						
A	*B*	*C*	good	*E/0*	*F/0*	*L/0*	*E/1*	*F/1*	*L/1*
0	0	0	0	0	0	0	1	1	0
0	0	1	1	0	0	1	1	1	1
0	1	0	1	0	0	1	1	1	1
0	1	1	1	0	0	1	1	1	1
1	0	0	0	0	0	0	0	1	0
1	0	1	0	0	0	1	0	0	0
1	1	0	0	0	0	1	0	0	0
1	1	1	0	0	0	1	0	0	0

Consider only six faults on *EFL*

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More Metrics

- ***Fault coverage (FC):*** **measure quality of test set**

$$\frac{number\ of\ \textbf{detected}\ \ faults}{number\ of\ \textbf{total}\ \ faults}\times 100\%$$

- ***Test coverage :*** **measure quality of test set (testable faults only)**

$$\frac{number\ of\ \textbf{detected}\ \ faults}{number\ of\ \textbf{testable}\ \ faults}\times 100\%$$

- ***ATPG effectiveness :*** **measure quality of ATPG algorithm**

$$\frac{number\ of\ \textbf{detected}+\textbf{untestable}\ \ faults}{number\ of\ \textbf{total}\ \ faults}\times 100\%$$

*NOTE: Each ATPG has its own definition. Details see ATPG manual.

Quiz

Item	Number
Total Faults	1,234
Detected faults	1,000
Untestable faults	230
Undetected faults	4
Fault Coverage	
Test Coverage	
ATPG effectiveness	

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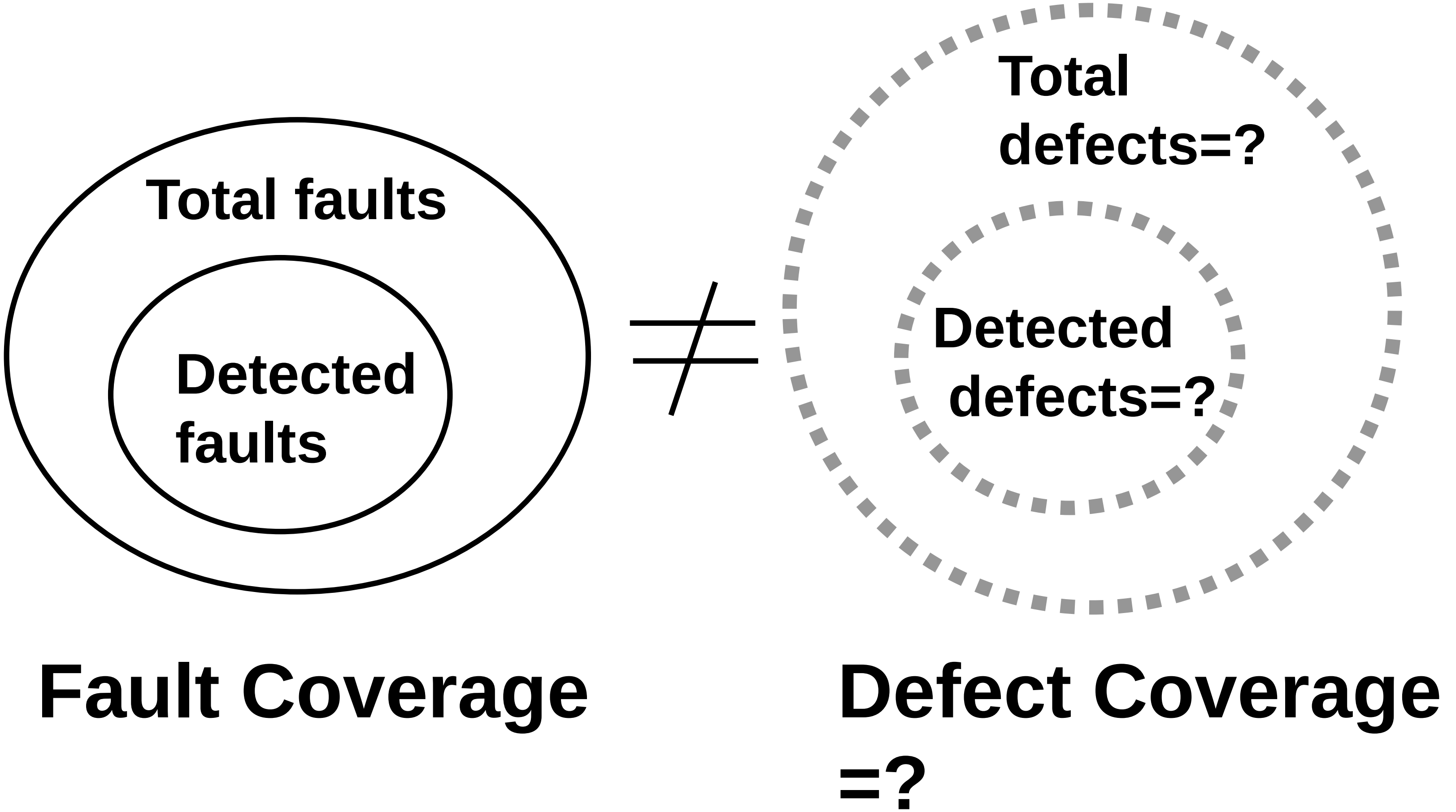
Revisit: DL $=1-Y^{(1-FC)}$

- **In practice, does 100% FC mean 0 DPM?**
  - **NO! Fault coverage does *NOT* represent defect coverage**



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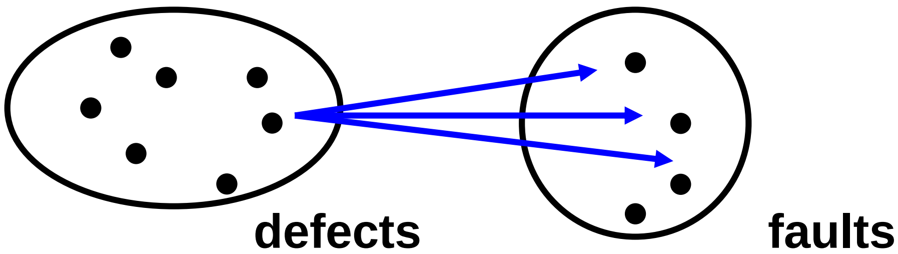
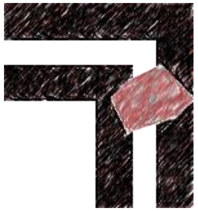
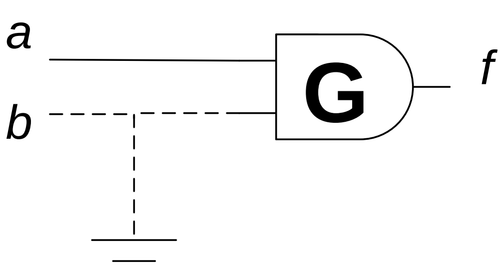
Defect → Faults

- Sometimes, one defect can be modeled by more than one fault



- Example:
  - unwanted wire between b and ground
    - *b* stuck-at zero SSF
    - *f* stuck-at zero SSF
    - *b* slow-to-rise transition fault
    - Gate delay fault in *G*
    - …





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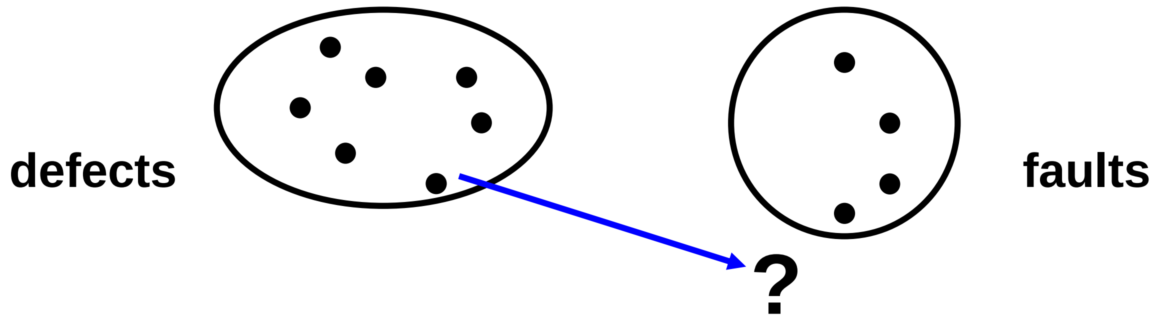
Defect → Faults (2)

- Sometimes, one defect cannot be well modeled by any fault



- Examples:
  - Slow process cannot be well modeled by SSF
    - (maybe path delay fault)
  - Reliability defects cannot be well modeled by SSF
  - Fault masking
  - …

Experimental Results

- 0.7μm CMOS, Murphy experiment, Stanford Univ. [McCluskey 00]
  - Total population 5.5K chips tested
    - 116 defective chips
    - Only 1/3 of defects behaves like SSF
    - 2~6 chips escaped 100% SSF test sets
- *N-detect* SSF test patterns
  - Detect each SSF at least *N* times by different patterns
  - No chip escaped *N*=3
  - Why? Accidental detection of unmolded defects

100% FC ≠ 0 DPM
Diversified Test Patterns Are Good

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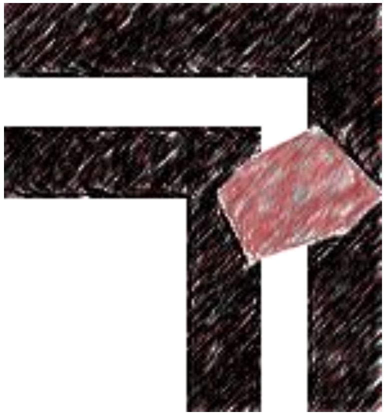

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Concluding Remarks

- Fault model is very important for test automation
  - Automatic test pattern generation
  - Quantify quality of test patterns
- Although many fault models, only a few used in practice
  - Single stuck-at faults is applied for sure
  - Transition delay faults may be applied
  - Other fault models adopted according to product needs
- NOTICE! Fault model can be deceiving
  - Fault models do not always match behavior of defects
    - Only 1/3 of defects behaves like SSF
  - 100% fault coverage DOES NOT guarantee zero DPM

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Isn’t 99.9% Good Enough?

- Look at the consequences of “almost, but not quite” perfect.
- If 99.9% is good enough then:
  - 2 million documents will be lost by IRS this year
  - 12 babies will be given to the wrong parents today
  - 2 plane landings daily at LAX airport will be unsafe
  - 18K pieces of mail will be mishandled in the next hour
  - ...

Because There are Many Faults
Small Δ in FC Makes Large Difference

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