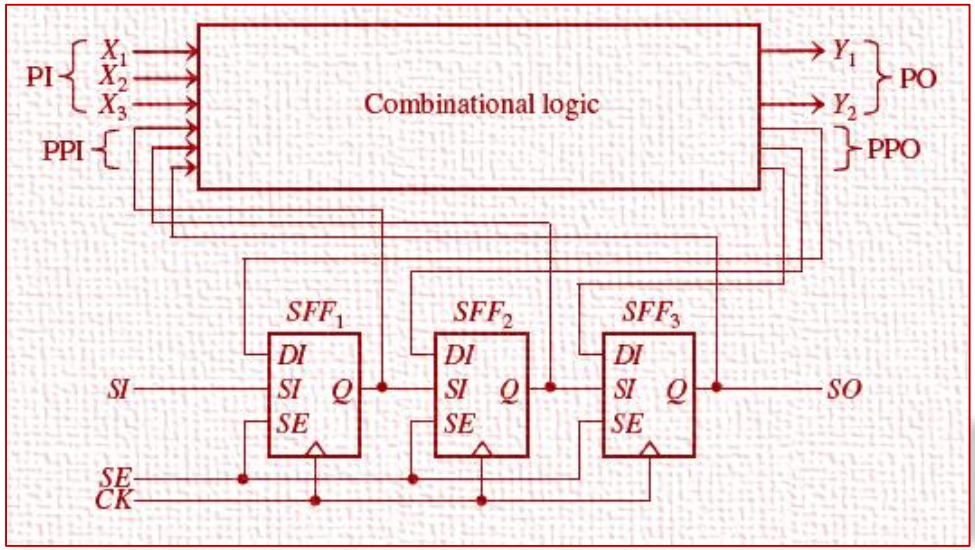
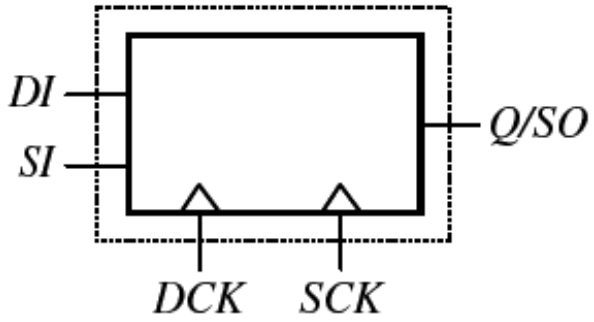
DFT - Part 1

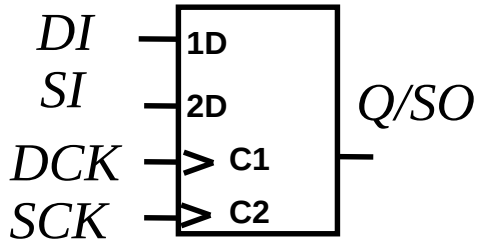
- Introduction
- **Internal Scan**
  - **FF-based**
    - MUXed-D scan (1973, Stanford)
    - **Clocked scan (1968, 1975 NEC)**
    - **Other scan**
  - Latch-based
    - LSSD (1977, IBM)
- Scan Design Flow
- Issues and Solutions
- Conclusion



Clocked Scan FF [Kobayashi 68][Funatsu 75]

- 2 inputs
  - Data in (DI): from logic
  - Scan in (SI): from previous scan FF
- 2 independent clocks
  - Scan clock (SCK): capture SI
  - Data clock (DCK): capture DI
- Data output (Q) and Scan Output (SO) share same pin

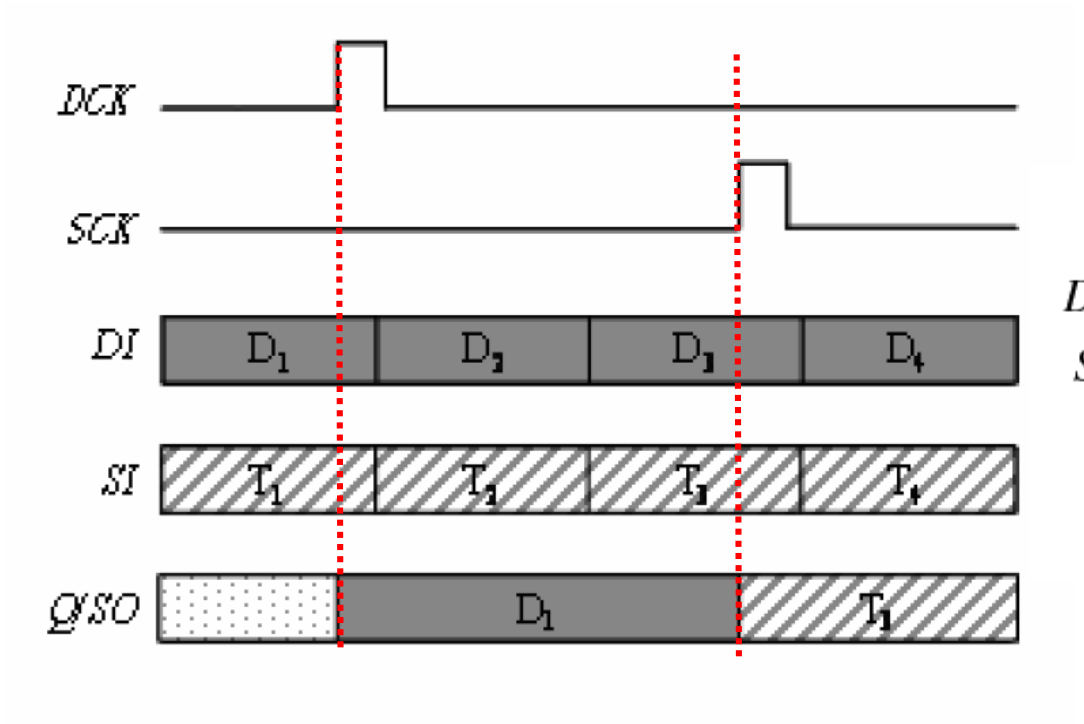


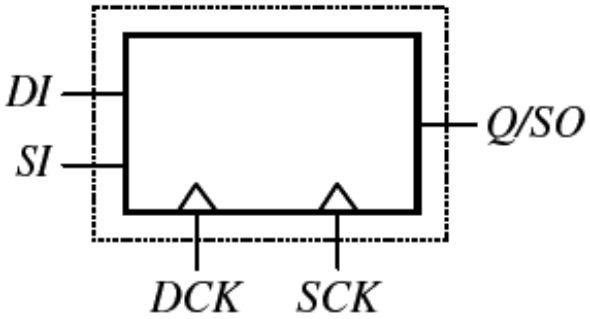


IEEE symbol

Clocked Scan FF (2)

- DI → Q at positive DCK edge
- SI → Q at positive SCK edge



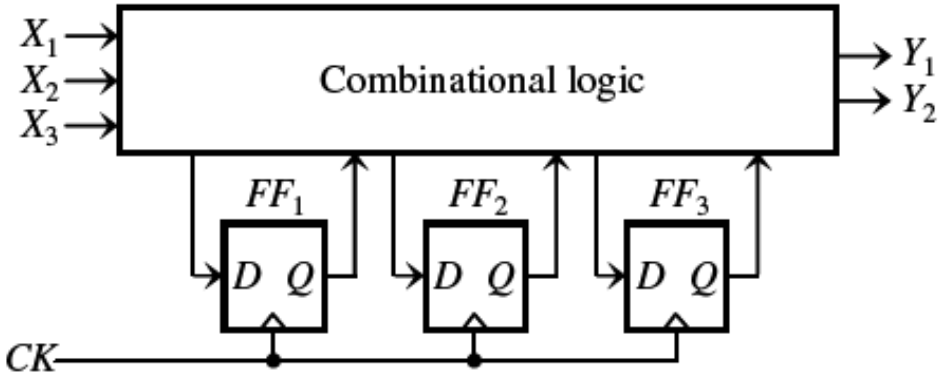


(WWW. Fig 2.11)

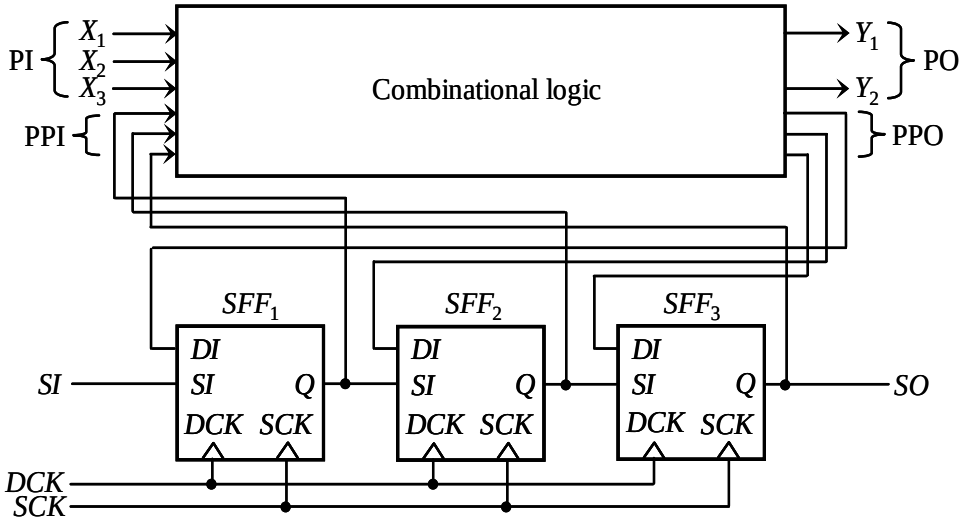
SCK/DCK Do NOT Overlap

Clocked Scan Architecture

- Original circuit
  - Single clock: CK
  - Regular D-FF

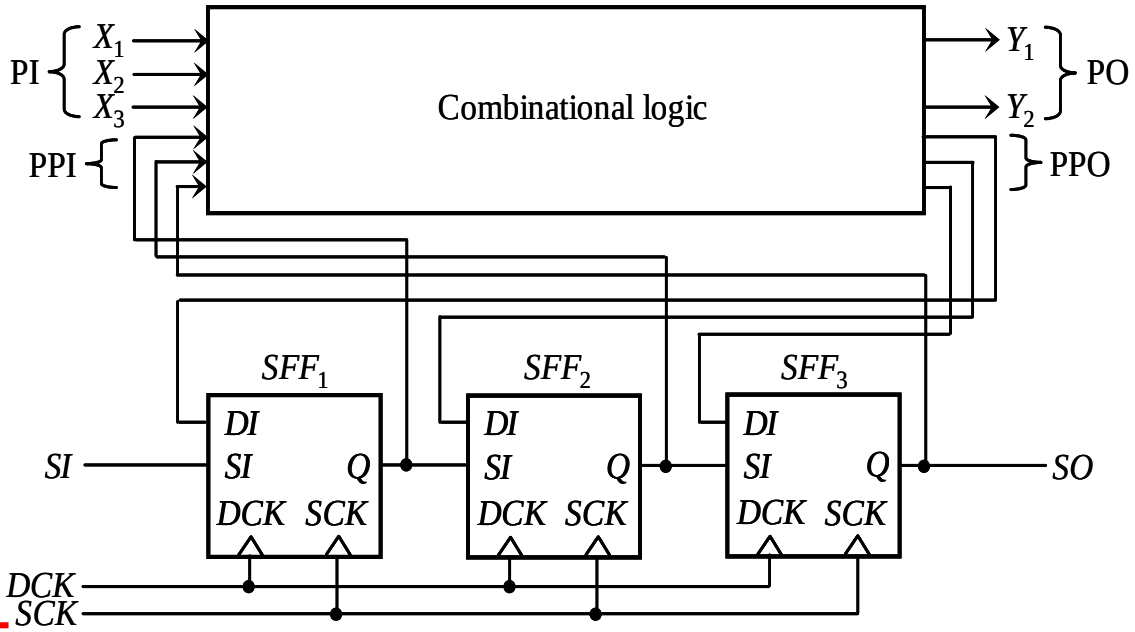


- After scan insertion
  - Two extra I/O pins
    - SI, scan input
    - SO, scan output
  - One extra clock
    - SCK



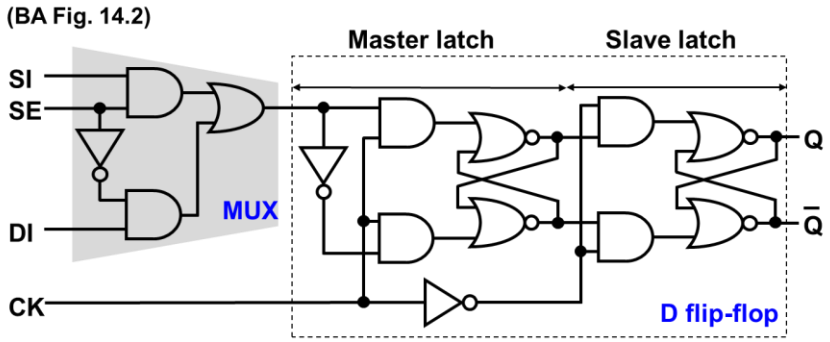
Clocked Scan Operation

- **Normal Mode**
  - **DCK, DCK …**
- **Test Mode**
  - **Shift: SCK, SCK, SCK (load scan chain)**
  - **Capture: DCK**
  - **Shift: SCK, SCK, SCK (unload scan chain)**

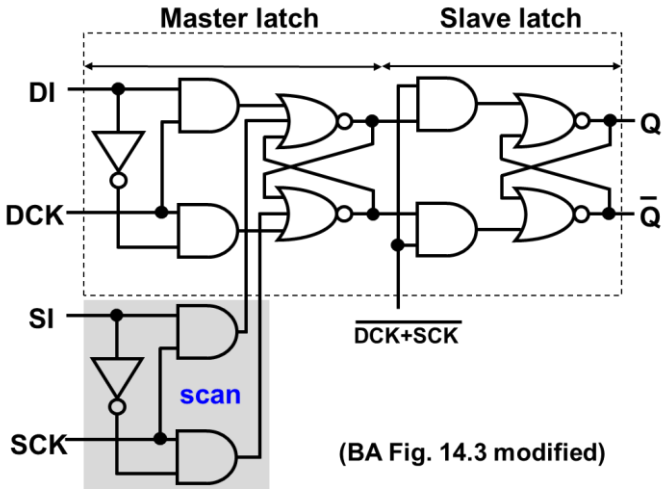


Pros/Cons of Clocked Scan

- Advantage
  - Faster than MUXed-D scan
    - Less delay overhead
- Disadvantage
  - Larger routing overhead than MUXed-D scan
    - Needs one extra clock distribution (SCK)



MUXed-D scan



Clocked scan

CS Faster but Larger

Quiz

Q: Which of the following is NOT true about clocked scan?

A. Clocked scan is better than MUXed-D scan

B. Clocked scan has two clocks

C. Clocked scan is faster than MUXed-D scan

D. Clocked scan is useful for high speed circuits

ANS:

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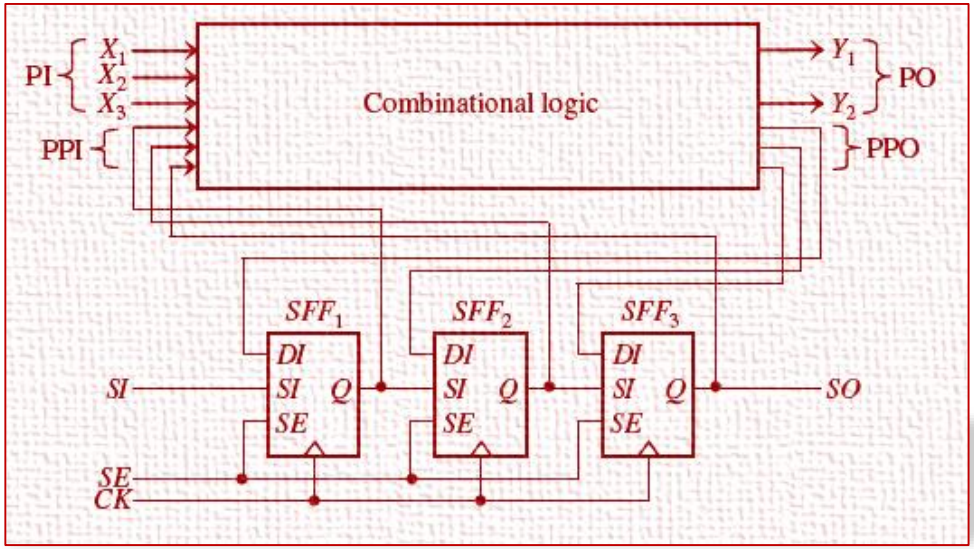
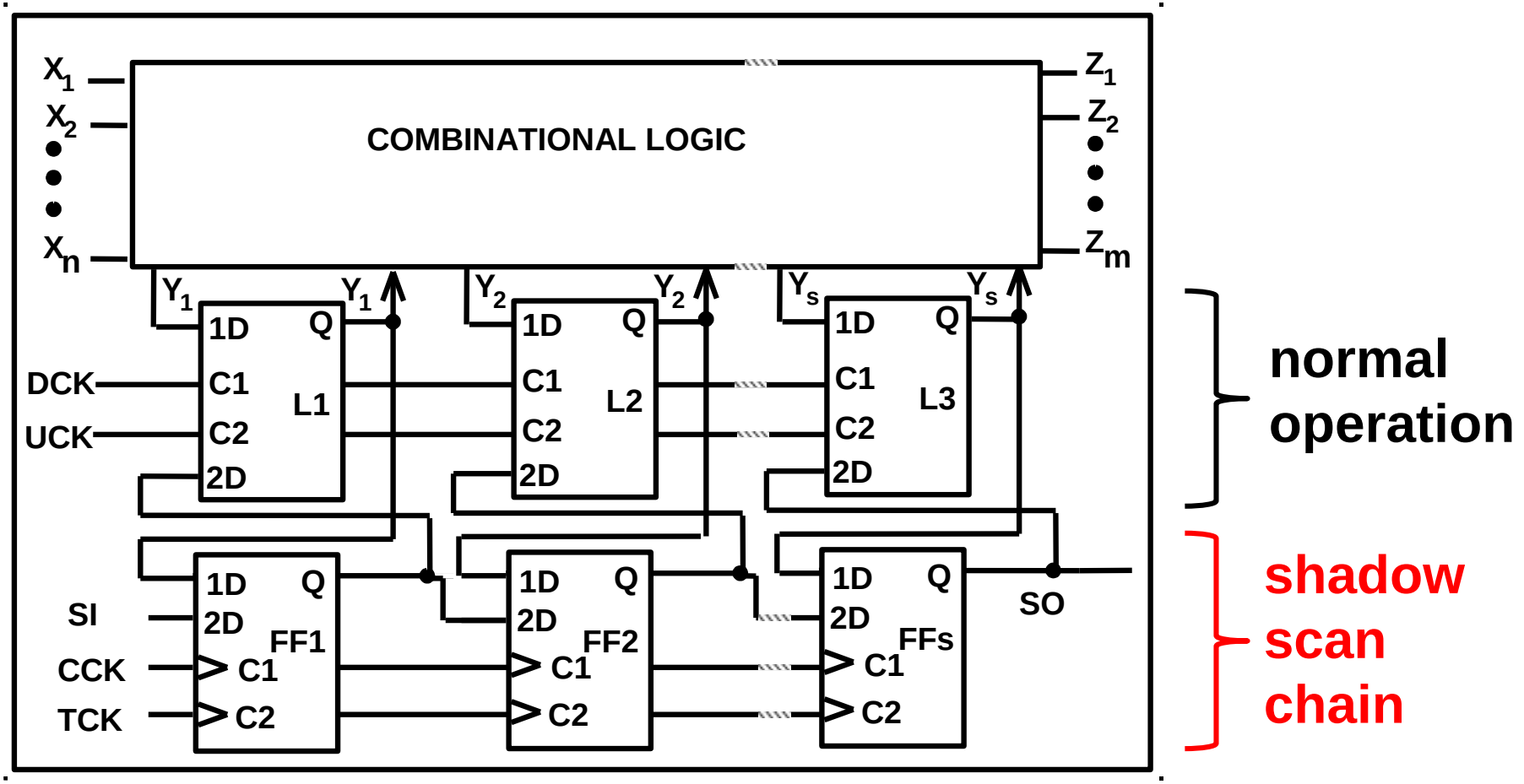
  - **FF-based**
    - MUXed-D scan (1973, Stanford)
    - **Clocked scan (1968, 1975 NEC)**
    - **Other scan**
      - **Shadow scan chain**
      - Random access scan, scan tree… (not in lecture)
  - Latch-based
    - LSSD (1977, IBM)
- Scan Design Flow
- Issues and Solutions
- Conclusion



Shadow Scan Chain

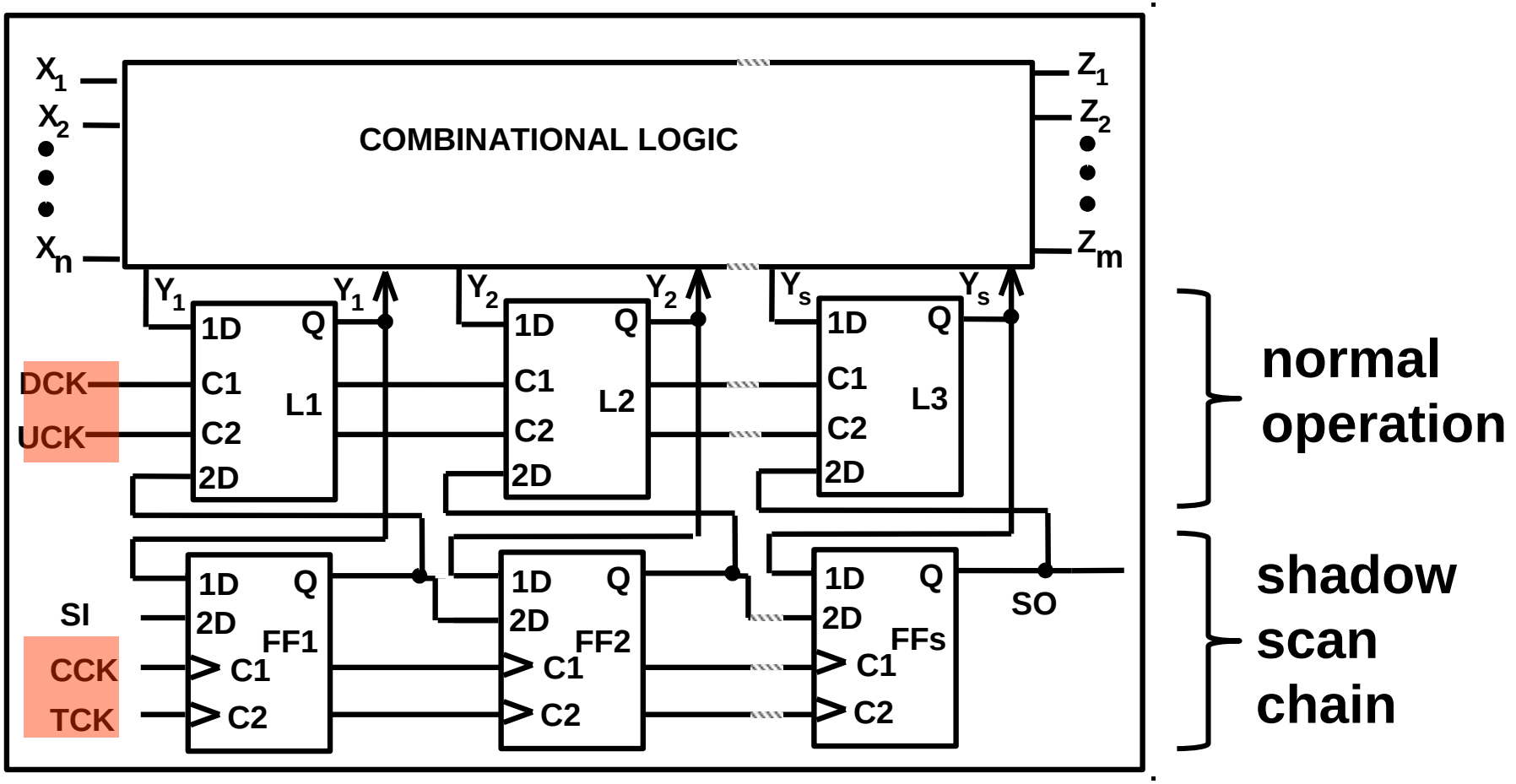
- *Design for Debug (DfD).* **More expensive than DfT**
  - **Duplicate FF!**
- **Purpose: Allow normal operation during scan chain shifting**



(Courtesy of Prof. McCluskey)

Shadow Scan Chain (2)

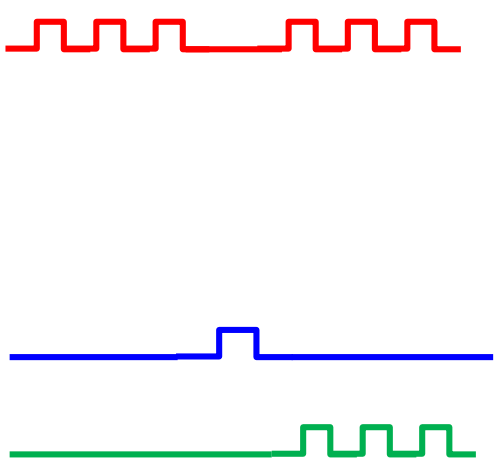
- Four clocks!
  - Normal: DCK
  - Capture: CCK. Shift: TCK. Update: UCK

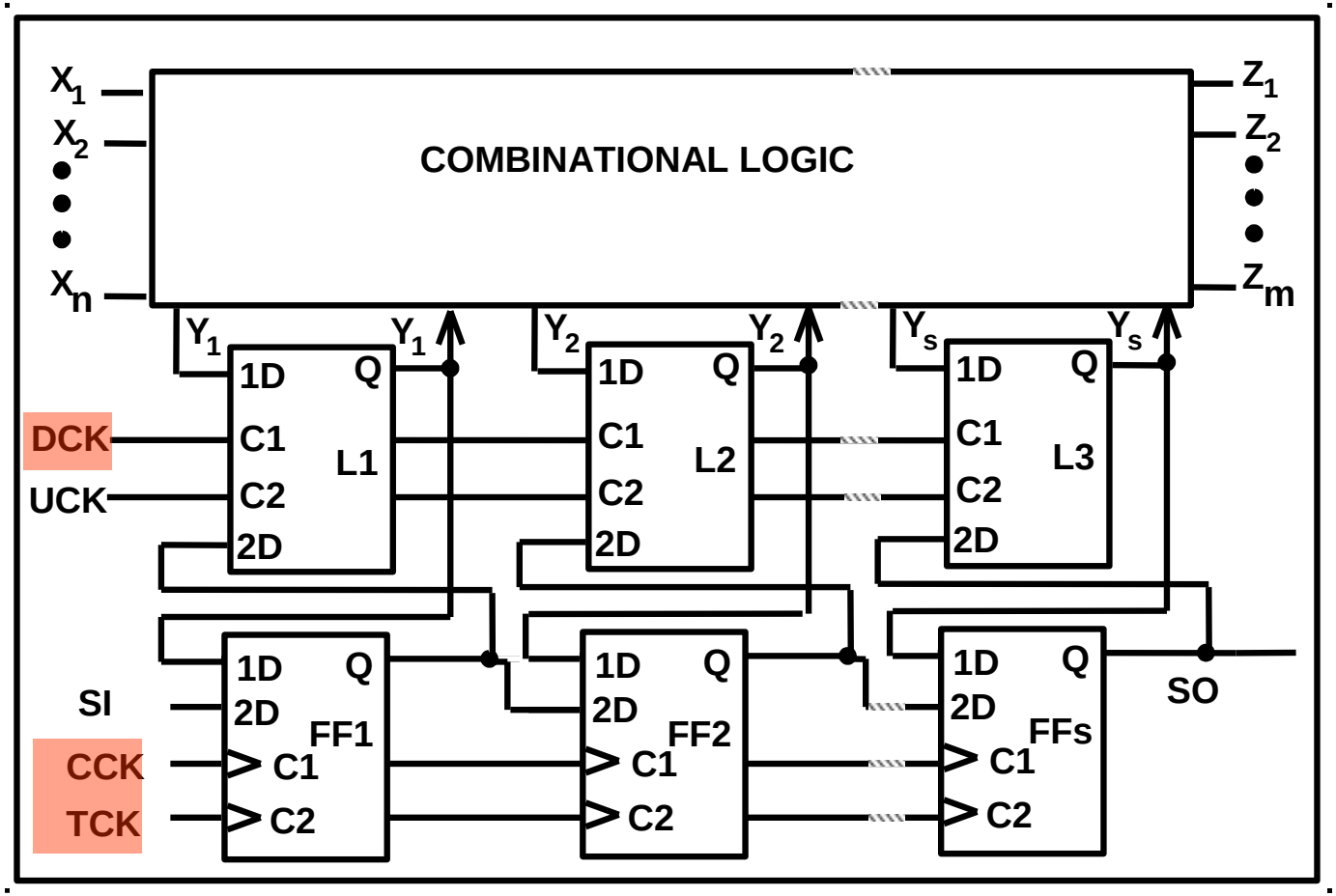


(Courtesy of Prof. McCluskey)

Observe FF Contents

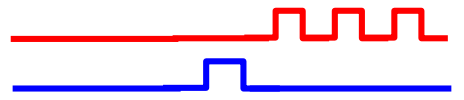
- **Normal operation: DCK, DCK …**
  - **Capture: CCK**
  - **Shift out: TCK, TCK, TCK. Normal operation: DCK, DCK ….**

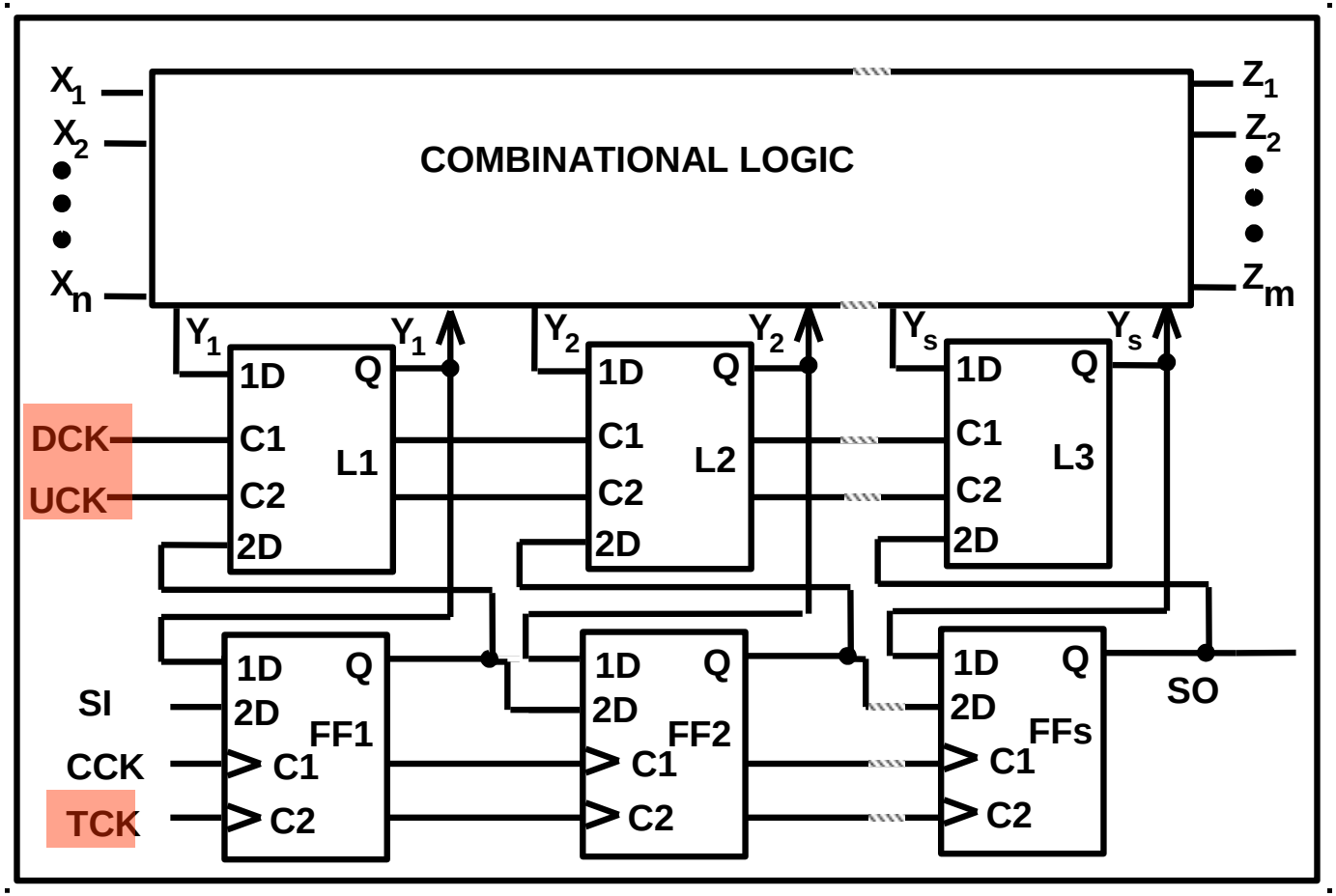




Control FF Contents

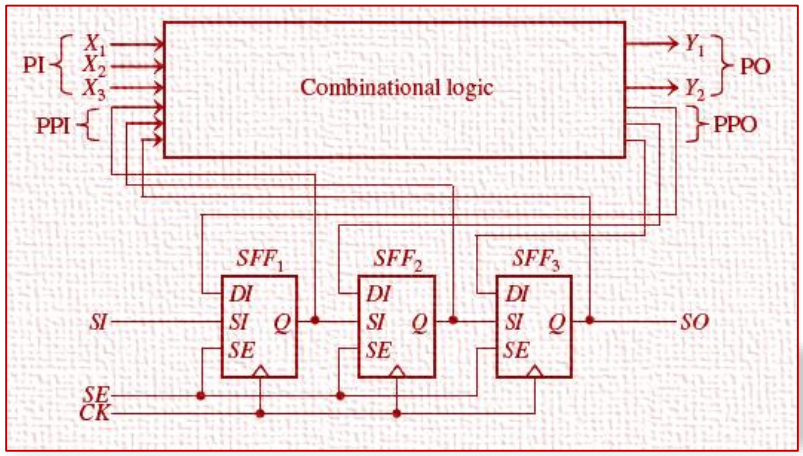
- **Shift in: TCK, TCK, TCK**
  - **Update: UCK**
  - **Begin normal mode: DCK, DCK …**





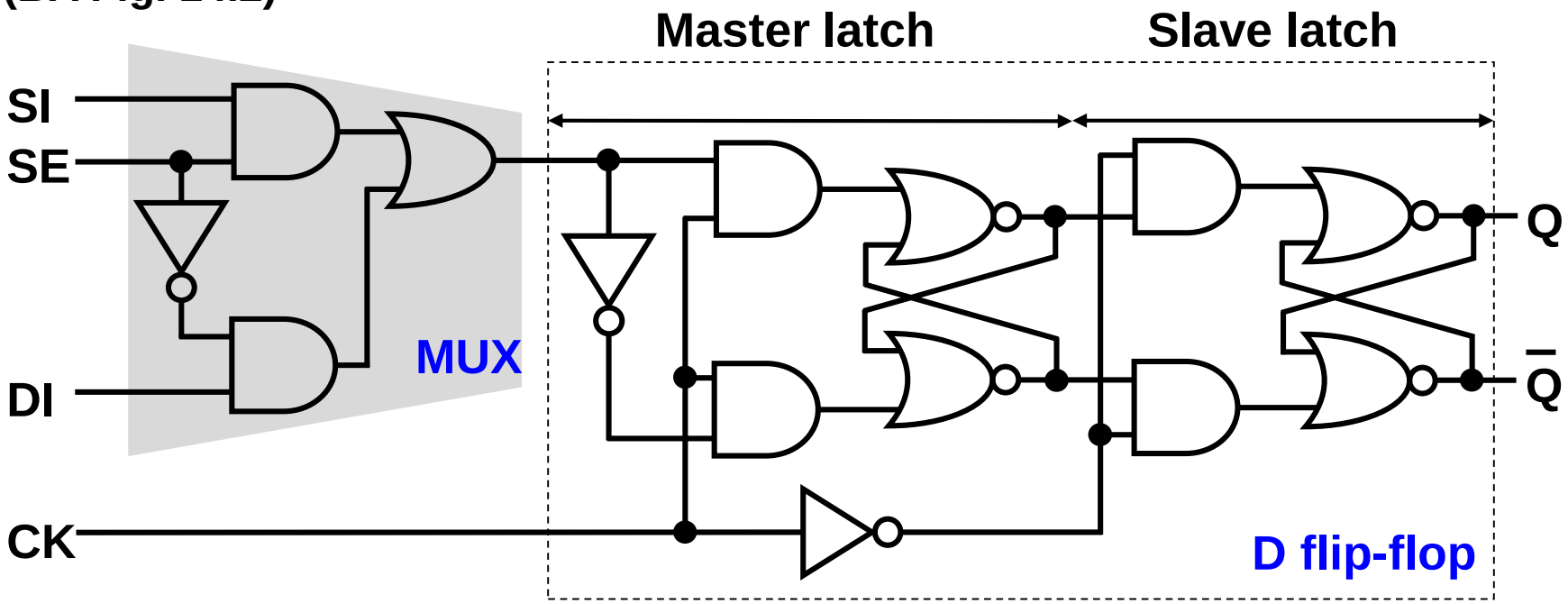
Summary

- Clocked scan : Two clocks
  - ☺ Faster than MUXed-D scan
  - ☹ Larger than MUXed-D scan
    - Useful for high speed circuits
- Shadow scan :
  - Control and observe contents of FF during normal operation
  - ☺ Useful Design for Debug (DfD)
  - ☹ Hugh area overhead !
    - Used in very expensive circuits

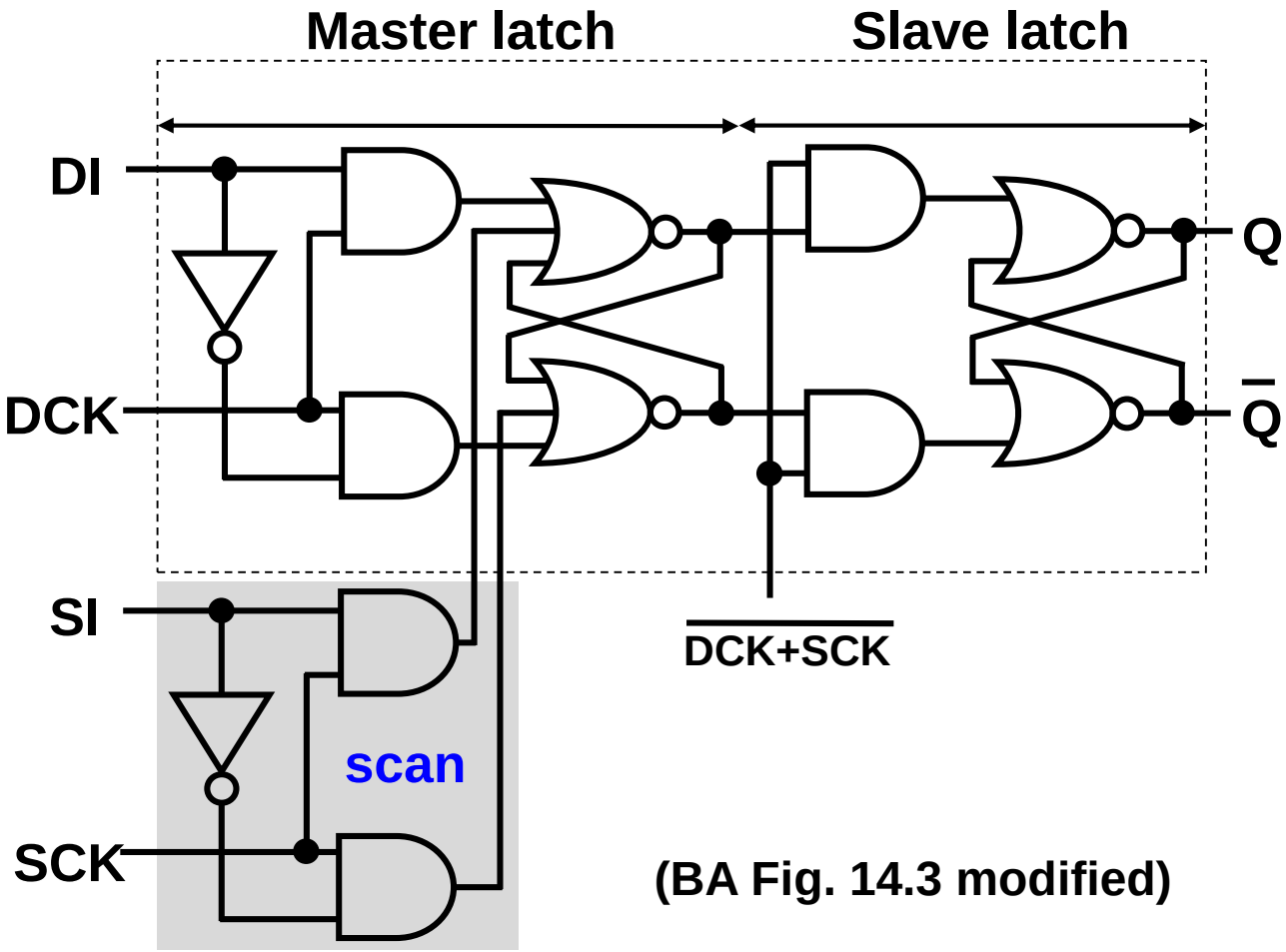


APPENDIX: Schematic of MUXed-D Scan

(BA Fig. 14.2)



APPENDIX: Schematic of Clocked Scan



(BA Fig. 14.3 modified)