DFT - Part 1

- **Introduction**
- **Internal Scan**
  - ♦ **FF-based**
    - ∗ **MUXed-D scan (1973, Stanford)**
      - ■ **MUXed-D scan flip-flop**
      - ■ **Test Mode Operation**
    - ∗ **Clocked scan (1968, NEC)**
    - ∗ **Other scan**
  - ♦ **Latch-based**
    - ∗ **LSSD (1977, IBM)**
- **Scan Design Flow**
- **Issues and Solutions**
- **Conclusion**

1
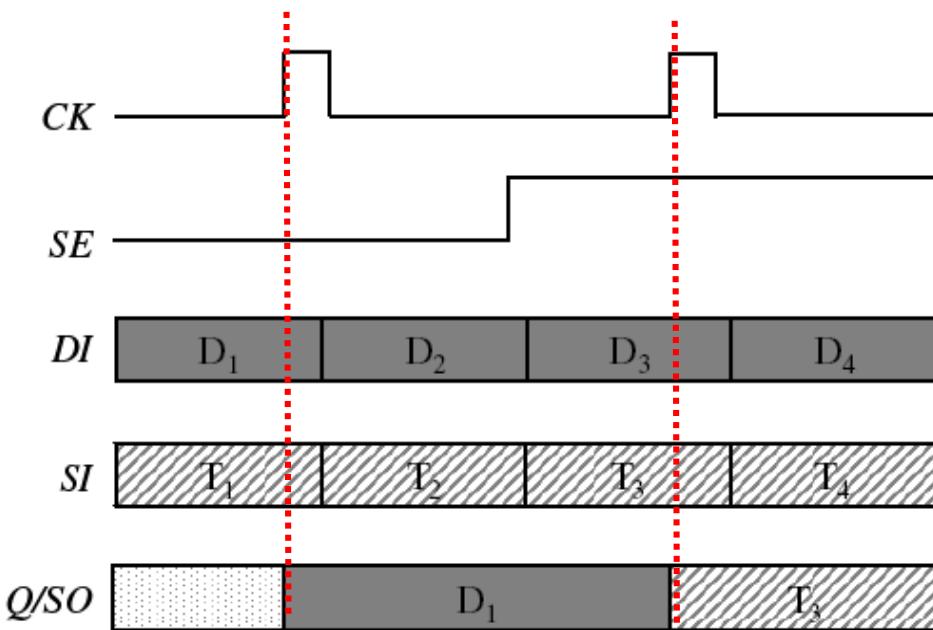
MUXed-D Scan Flip-flop [Williams 73]

- **Often used in flip-flop based, standard cell design**
- **3 input, 1 output, 1 clock pin**
- *Scan Enable* **(SE) pin selects inputs**
  - *Data in* **(DI): from logic**
  - *Scan in* **(SI): from previous scan FF**
- *Data output* **(DO) and** *Scan output* **(SO) often share same pin (Q)**
- **One multiplier (MUX) slower and larger than regular non-scan FF**

FF

logic

Scan in (SI)

Data in (DI)

1

0

D

ck

Q

Data output (DO)
Scan output (SO)
shared same pin (Q)

Scan enable (SE)

2
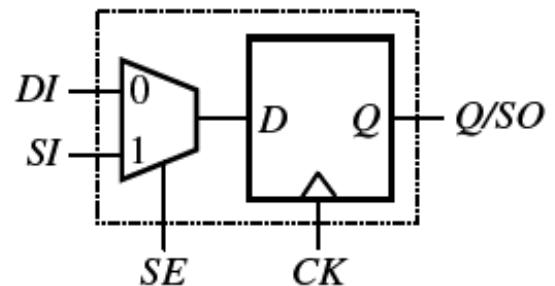
MUXed-D Scan Flip-flop

- **Positive edge triggered MUXed-D scan FF (WWW Fig. 2.9)**
  - **SE=1**, **SI$\rightarrow$ Q at positive clock edge**
 - **SE=0**, **DI$\rightarrow$ Q at positive clock edge**
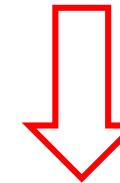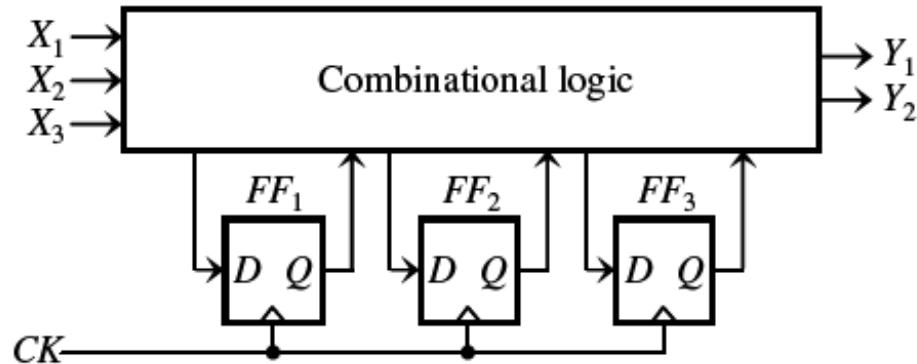
|	operation
SE=0	Capture (DI$\rightarrow$Q)
SE=1	Shift (SI$\rightarrow$SO)

SE = 1 enables scan
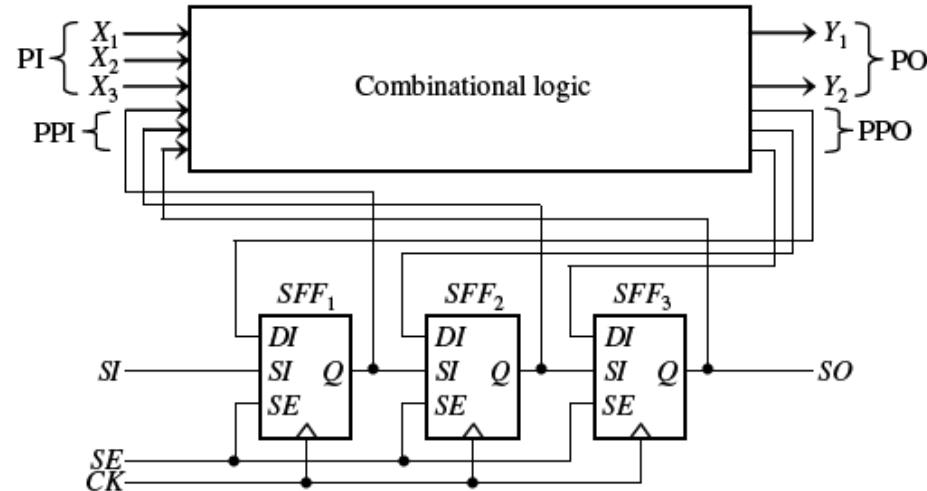
Muxed-D Scan Architecture

- **Original circuit**
  - ♦ **Single clock**
  - ♦ **Positive edge triggered**
  - ♦ **Non-scan DFF**

- **After scan insertion**
  - ♦ **Three extra pins**
    - ∗ **SI, SE, SO**
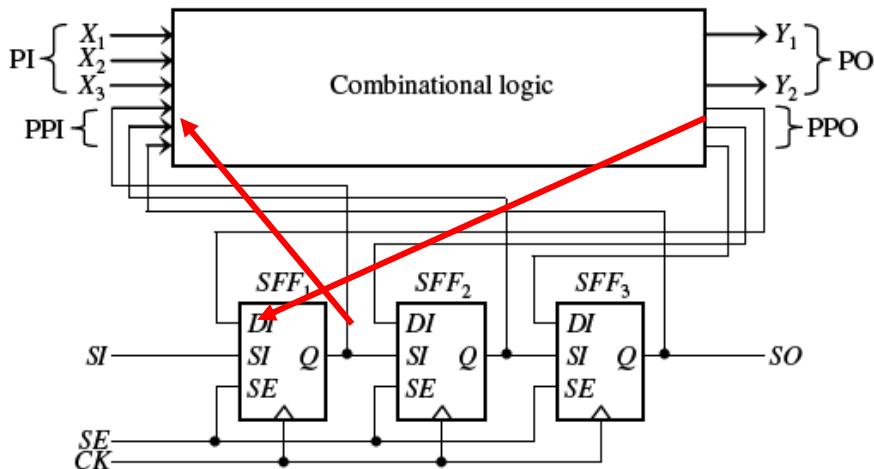
SFF = scan FF

Normal Mode Operation
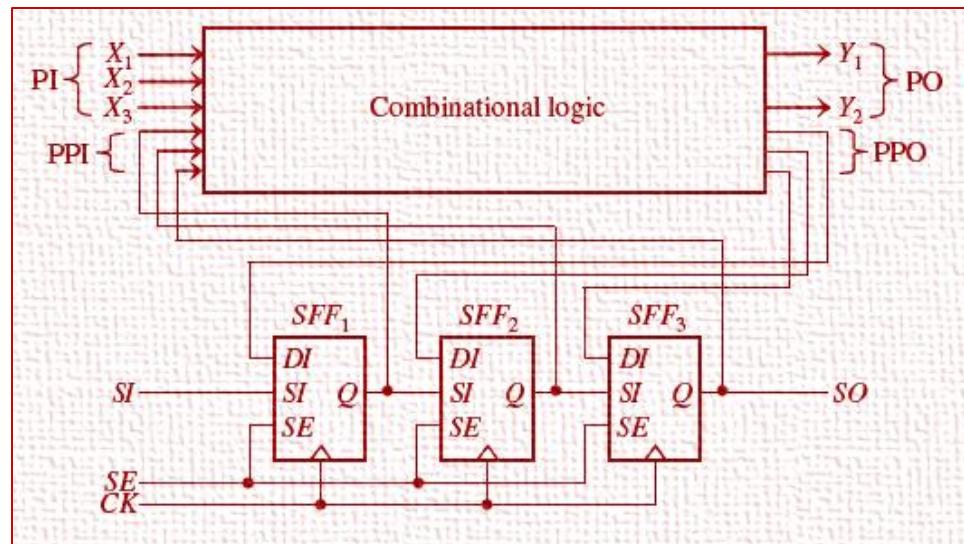
- **Always SE = 0**
- **Same as original circuit**

	operation
SE=0	**Capture (DI→Q)**
SE=1	Shift (SI→SO)

Test Mode Operation

- **Stuck-at fault testing**
  - ◆ **One pattern per scan**
- **Delay fault testing**
  - ◆ **Two-patterns per scan**
    - ∗ **Launch-on-Shift**
    - ∗ **Lunch-on-Capture**

SAF Operation

load	capture	unload

apply   PI (same for all cycles)   PI (next pattern)

apply   SI (cycle by cycle)   SI (next pattern)

observe   PO   SO

CK   ⊓⊓ ··· ⊓   ⊓   ⊓⊓ ··· ⊓

SE

7
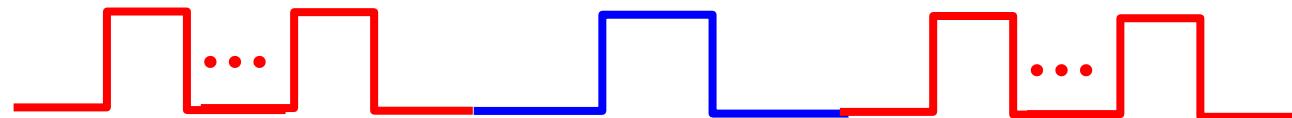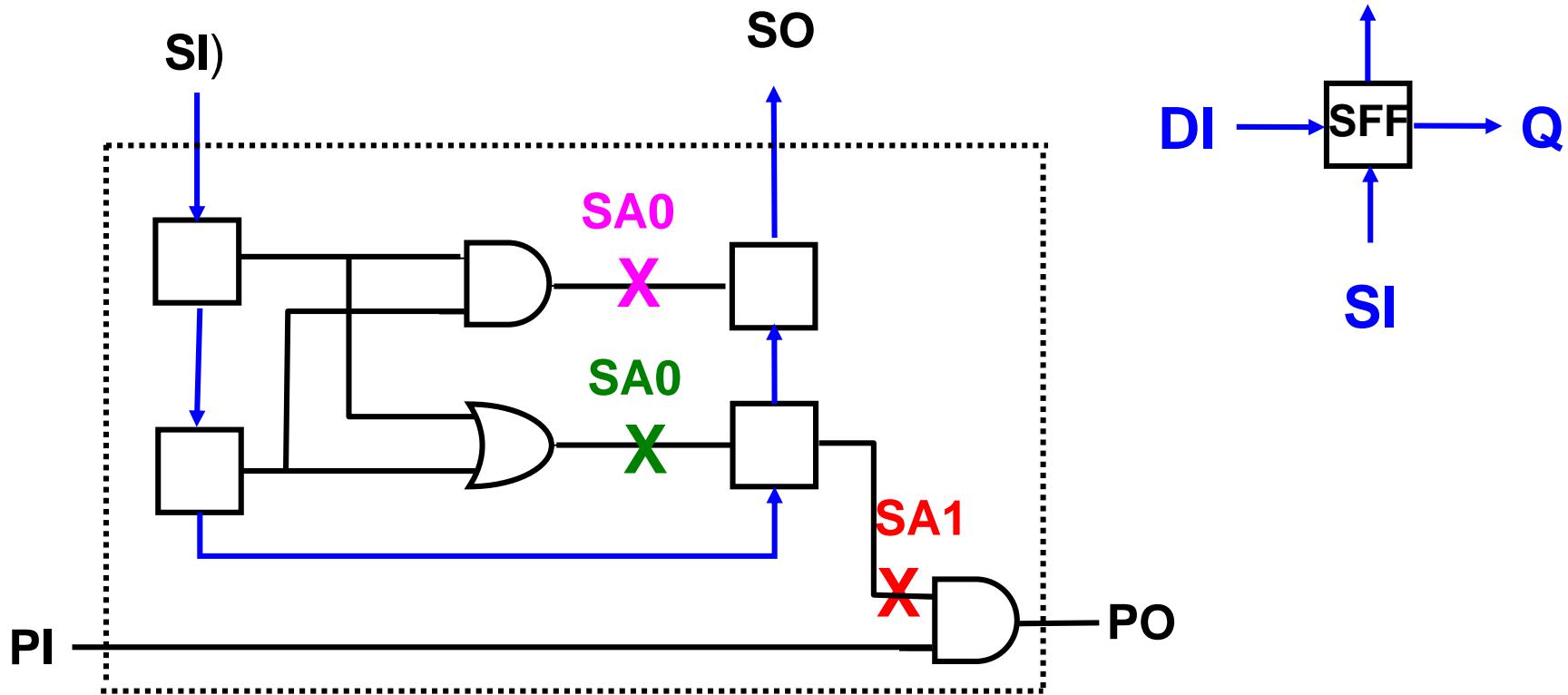
SAF Example

load		capture		unload
CK = PPPP		CK=P		CK = PPPP
SE = 1111	SE 1→0	SE = 0	SE 0→1	SE = 1111
SI = X011				SO = HHXX
PI = 1	PO = L			

P = CK pulse
H=expected 1
L=expected 0
Left bit first in/out

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Test Mode Operation

- **Stuck-at fault testing**
  - ♦ **One pattern per scan in/out**
- <u>**Delay fault testing**</u>
  - ♦ **Two-patterns per scan in/out**
    - ∗ <u>**Launch-on-Shift (aka. Skew load)**</u>
    - ∗ **Lunch-on-Capture (aka. Broad-side load)**

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LOS Operation

Load V$_1$	V$_2$	capture	unload

apply PI$_1$ | PI$_2$ | | PI (next pattern)

apply SI$_1$ | SI$_2$ | | SI (next pattern)
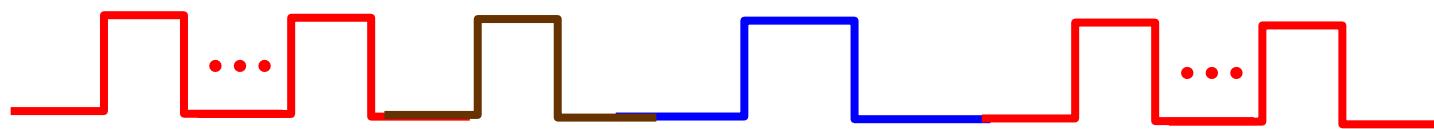
observe PO | SO
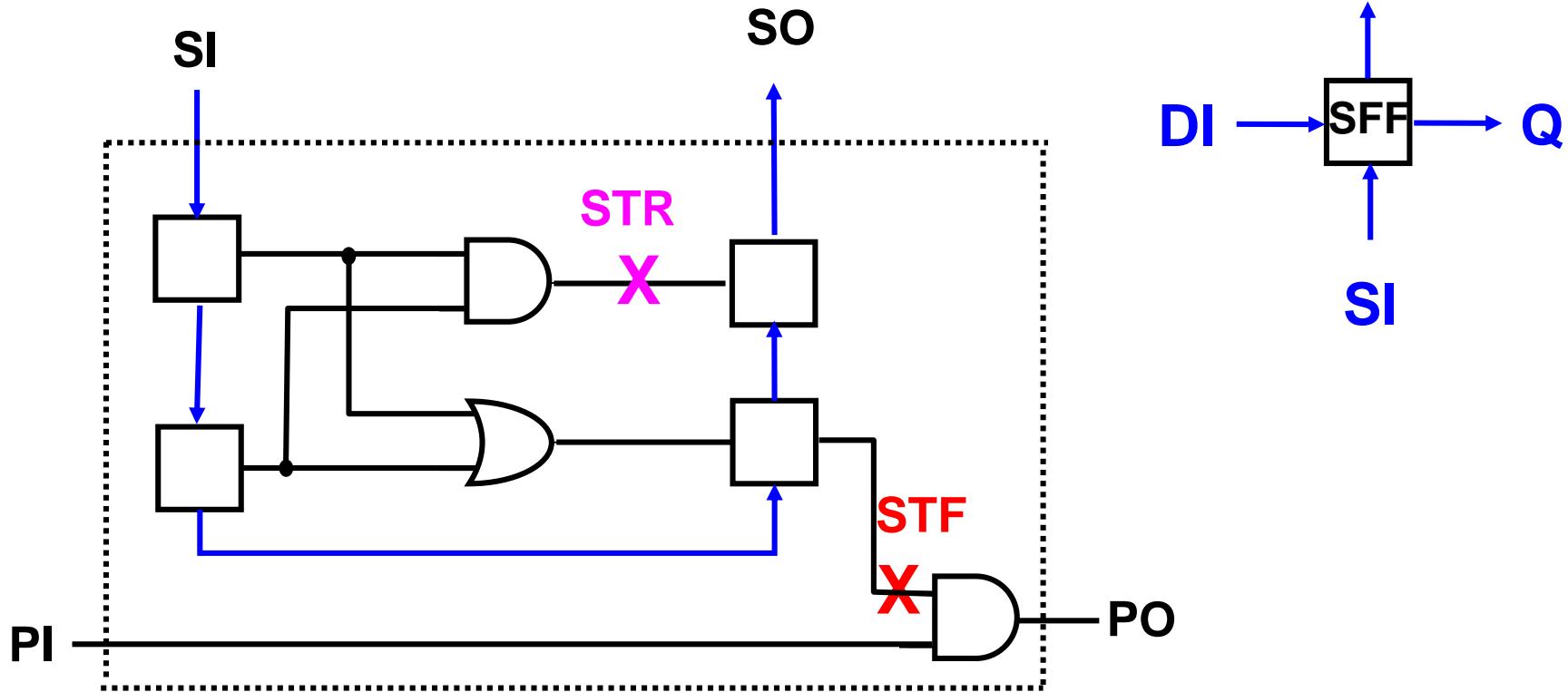
CK

SE
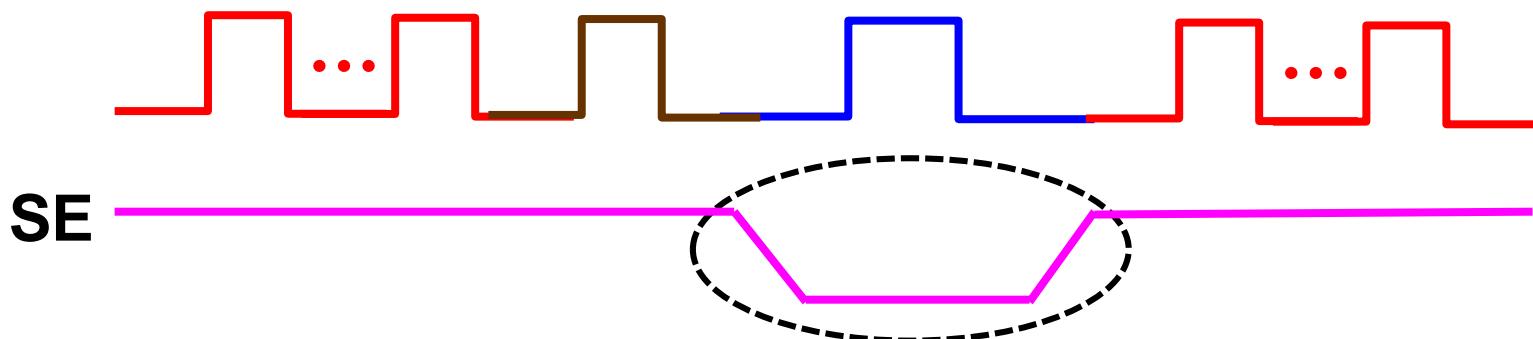
LOS Example

| load V$_1$	V$_2$		Capture		unload
CK = PPPP	CK=P		CK=P		CK = PPPP
SE = 1111	SE=1	SE 1→0	SE = 0	SE 0→1	SE = 1111
SI = X101	SI=1				SO = HXXX
PI = X	PI=1	PO=L			
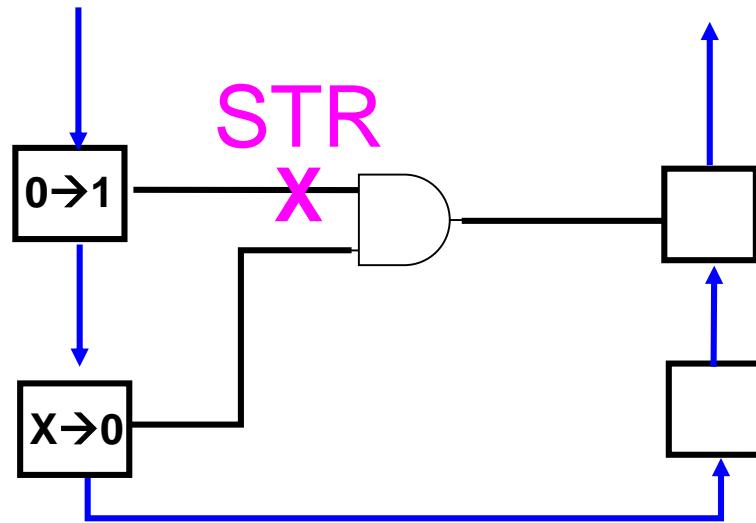
LOS -- Pro and Cons

- **Advantages**
  - **+ Easier for combinational ATPG**

- **Disadvantages**
  - **V_2-capture time is not at-speed**
    - » **Scan_enable signal fall time limitation**
    - » **Currently, ~ 5ns minimum**
    - » **Solution: route scan_enable as clock (area overhead)**
  - **Invoke transitions that never happen in normal operation**
  - **Some TDF not testable; *structure dependency problem***
    - » **V_2 is shifted version of V_1**

SE

Structure Dependency

- **STR fault untestable using LOS**
- **This fault can actually happen in normal operation**
 - **This fault needs to be tested, but how?**

**Some faults are untestable by LOS**

Test Mode Operation

- **Stuck-at fault testing**
  - ♦ **One pattern per scan in/out**
- **<u>Delay fault testing</u>**
  - ♦ **Two-patterns per scan in/out**
    - ∗ **Launch-on-Shift (aka. Skew load)**
    - ∗ **<u>Lunch-on-Capture (aka. Broad-side load)</u>**

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LOC Operation

Load V$_1$	V$_2$	cap	unload

apply PI$_1$ PI$_2$ PI (next pattern)

apply SI SI (next pattern)

observe PO SO

CK

SE
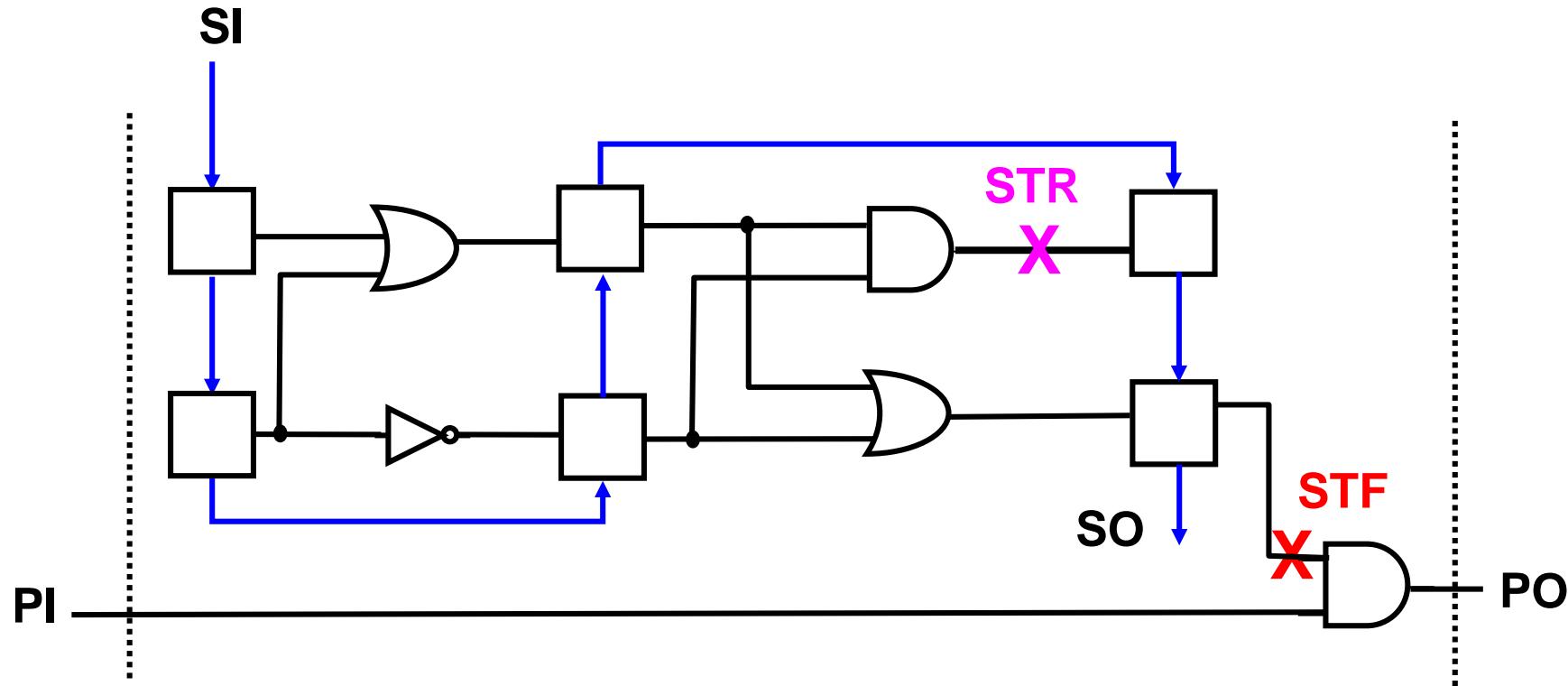
LOC Example

| Load V$_1$		V$_2$		capture		unload
CK=PPPPPP		CK=P		CK=P		CK=PPPPPP
SI=1X0001		SI=X				SO=X**H**XXXX
SE=111111	SE 1→0	SE=0	SE=0	SE=0	SE 0→1	SE=111111
PI=X	PI=1		PO=**L**		SO=X	

16
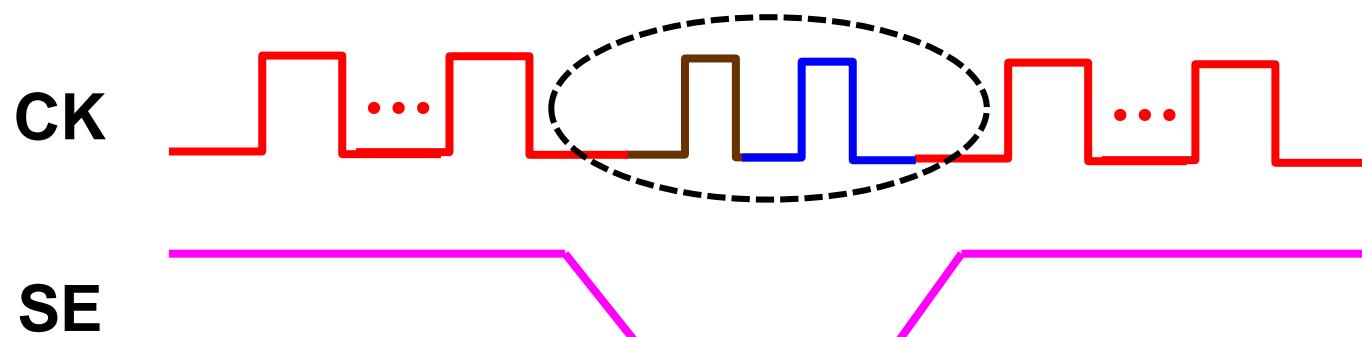
LOC -- Pro and Cons

- **Advantages**
  - V_2-capture can be applied at system clock speed
    - True at-speed testing
  - Avoid structure dependency problem of LOS
  - Minimum work in physical design, SE can be routed as normal signal
- **Disadvantages**
  - ATPG is more complex
    - » Requires two time frames

FFT

- **Q: Are there faults untestable by LOC?**
  - **If so, how should we test them?**