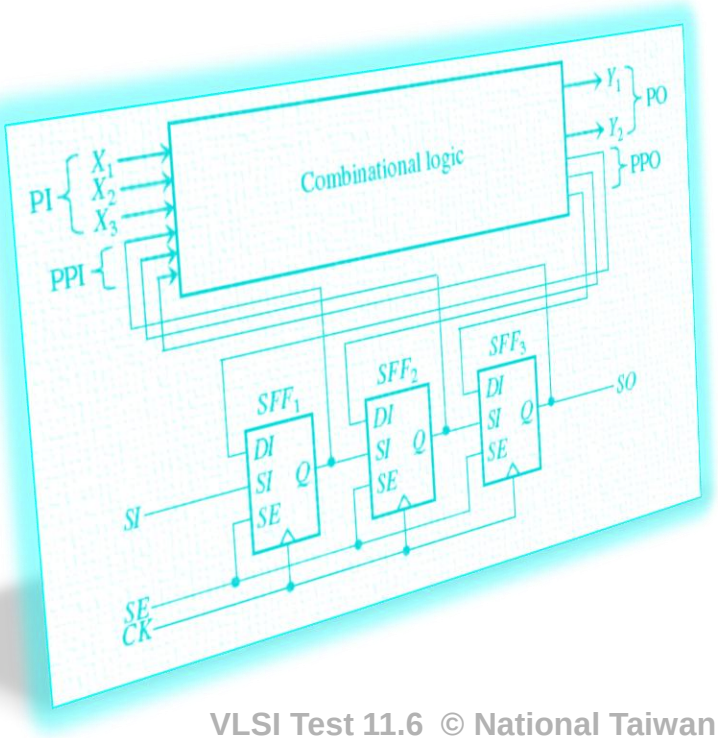
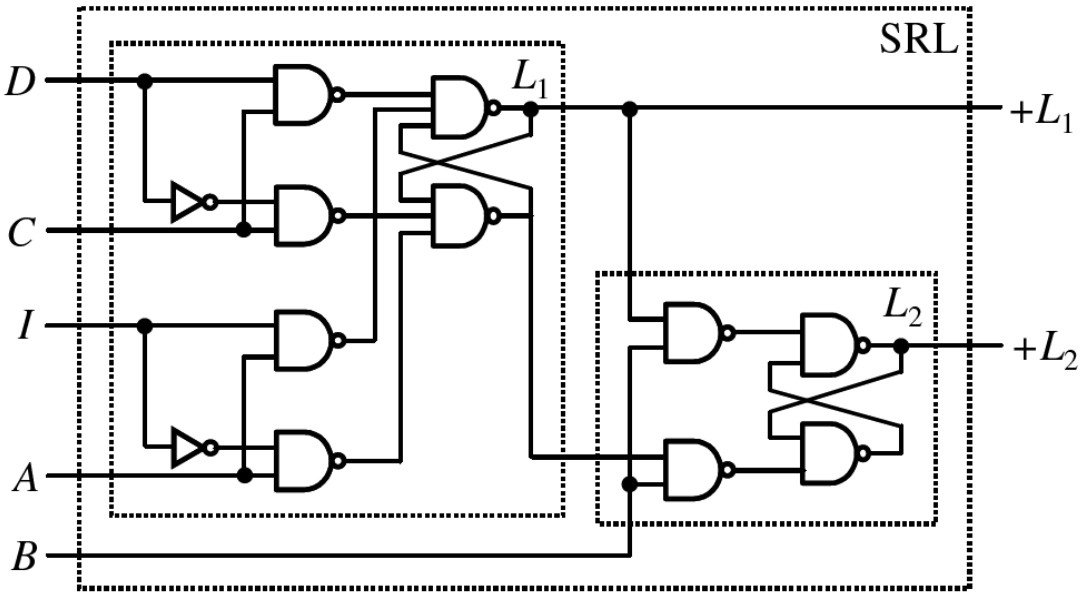
DFT - Part 1

- Introduction
- **Internal Scan**
  - FF-based
    - MUXed-D scan (1973, Stanford)
    - Clocked scan (1968, NEC)
    - Other scan
  - **Latch-based**
    - **LSSD (1977, IBM)**
- Scan Design Flow
- Issues and Solutions
- Conclusion



Level Sensitive Scan Design, LSSD

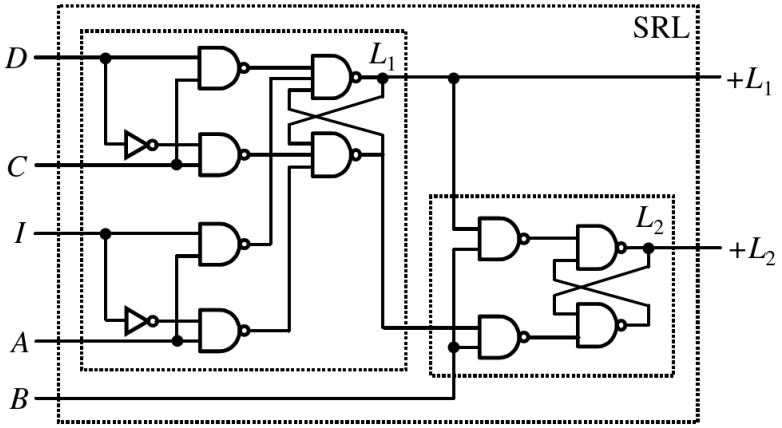
- Invented by IBM [Eichelberger 77]
- Master-slave latch
  - Master L_1: 2-port latch, AC clocks
  - Slave L_2: 1-port latch, B clock
  - 2 inputs: Data input (*D*); Scan input (*I*)
  - 2 outputs: *+L1*, *+L2*



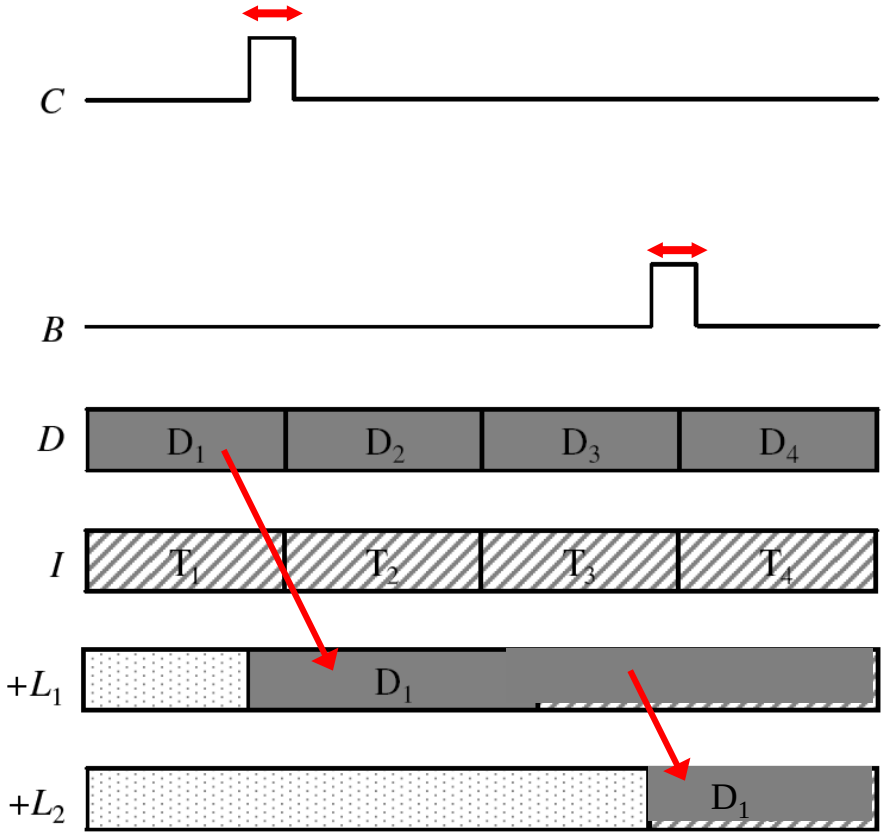
LSSD scan latch is called:
Shift Register Latch (SRL)

Normal Mode Operation

- **Clocking sequence:**
  - **C clock B clock: D → $+L_1$ → $+L_2$**

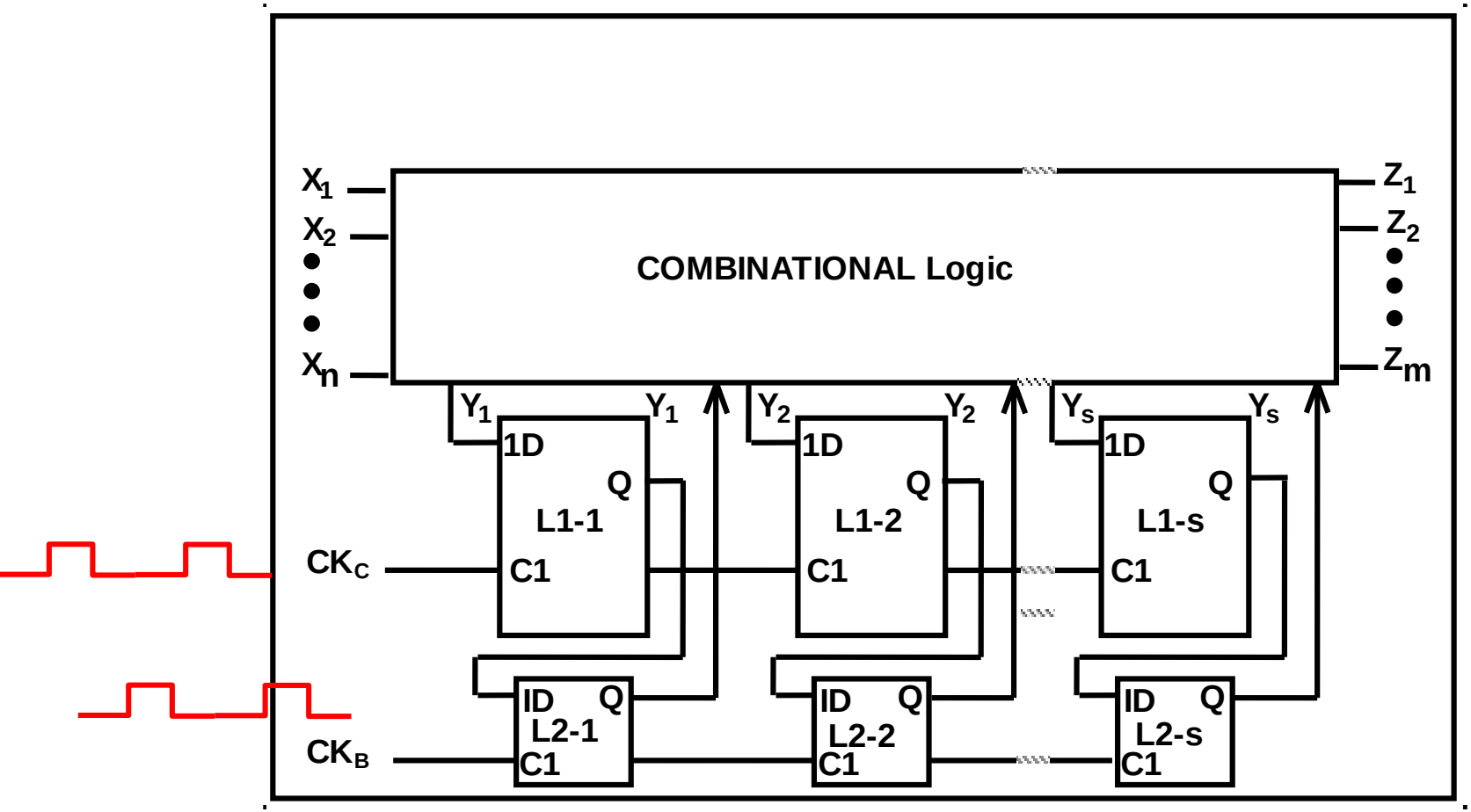


(WWW Fig. 2.12)



Double Latch-based Design (w/o LSSD)

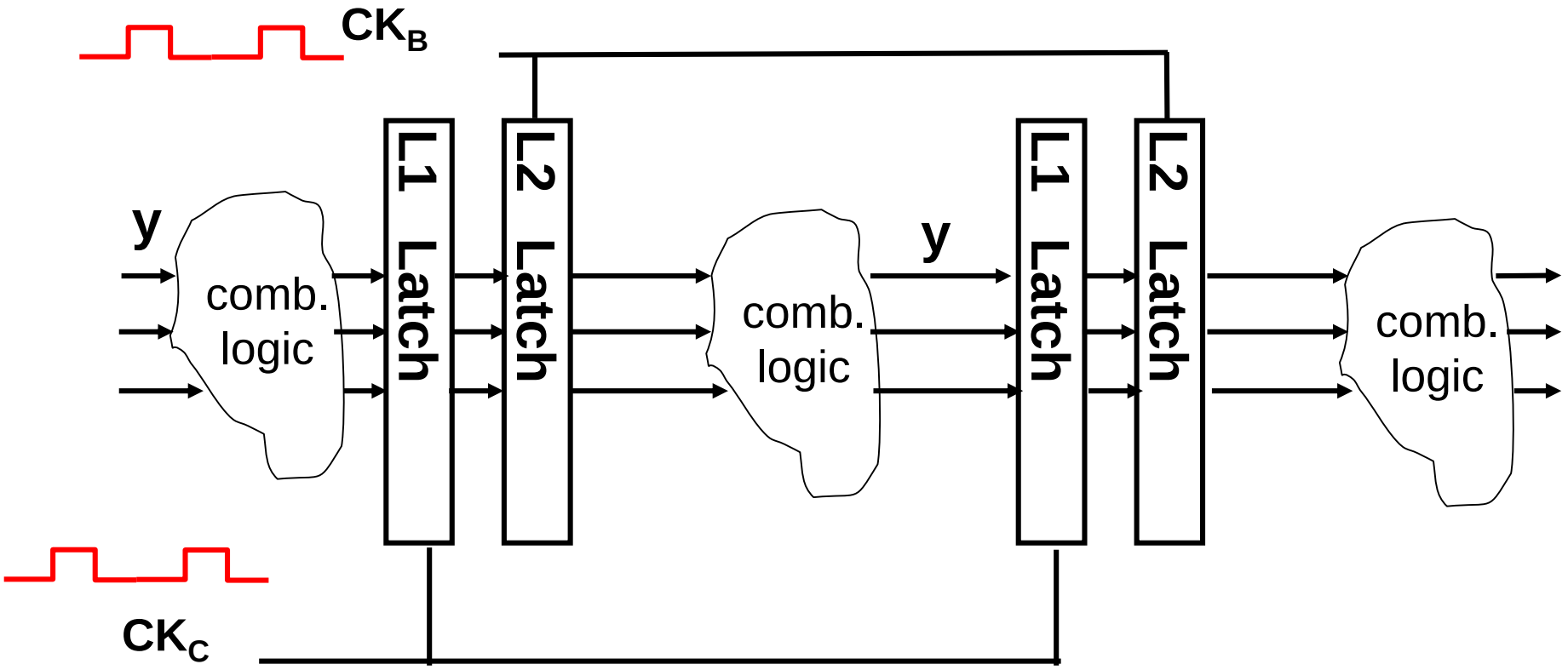
- **Normal operation mode: CK_C CK_B, CK_C CK_B …**
  - **Clock B and C non-overlapping**



(Courtesy of Prof. McCluskey, Stanford)

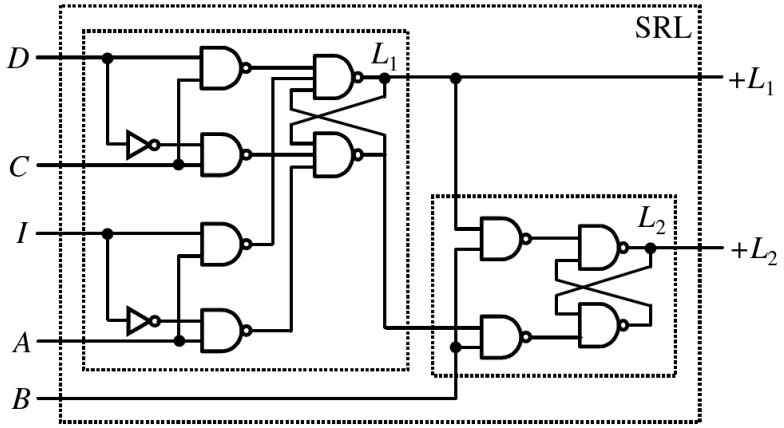
Another Point of View

- 2 latches per stage: L1 and L2
- Normal mode: CK_C CK_B, CK_C CK_B …
  - non-overlapping clocks, avoid clock skew

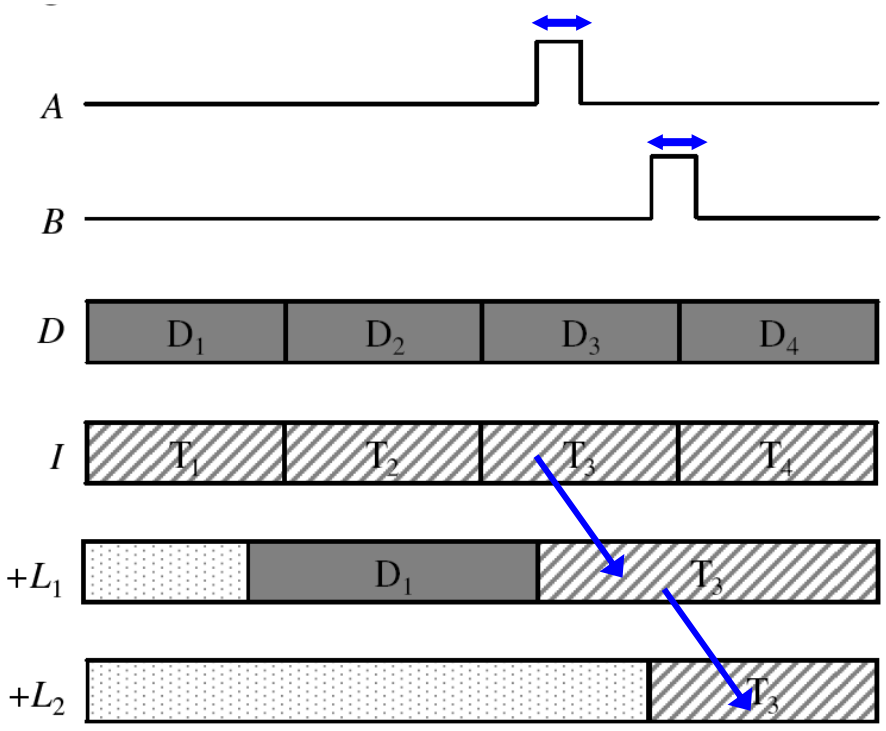


Shift

- **Clocking sequence:**
  - **A clock B clock: I → $+L_1$ → $+L_2$**

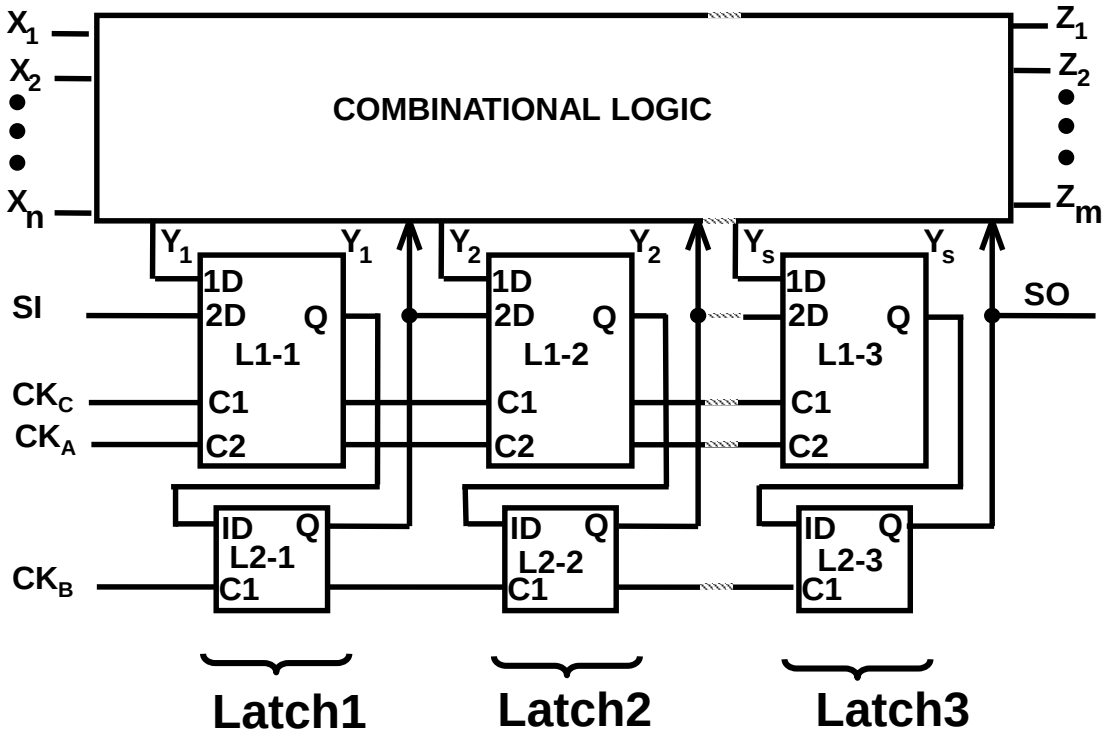


(WWW Fig. 2.12)



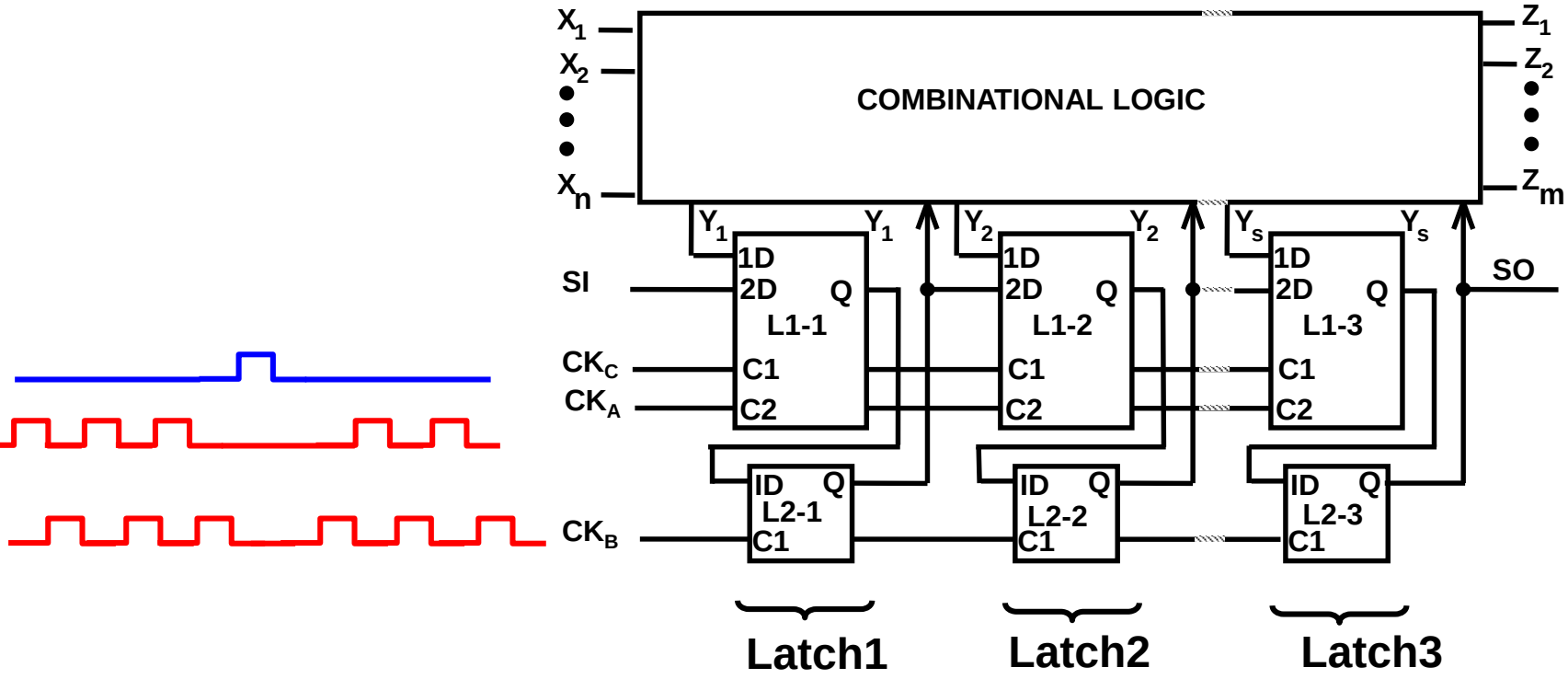
Double Latch-based Design (w/ LSSD)

- Replace L_1 1-port latch by 2-port latch
- Add scan input (SI), scan output (SO)
- Add A clock



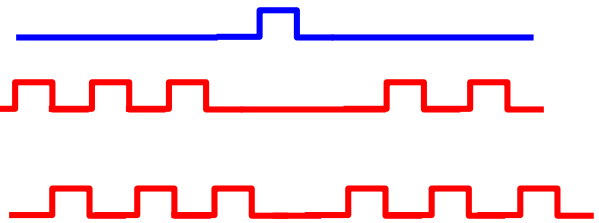
Test Mode Operation (1)

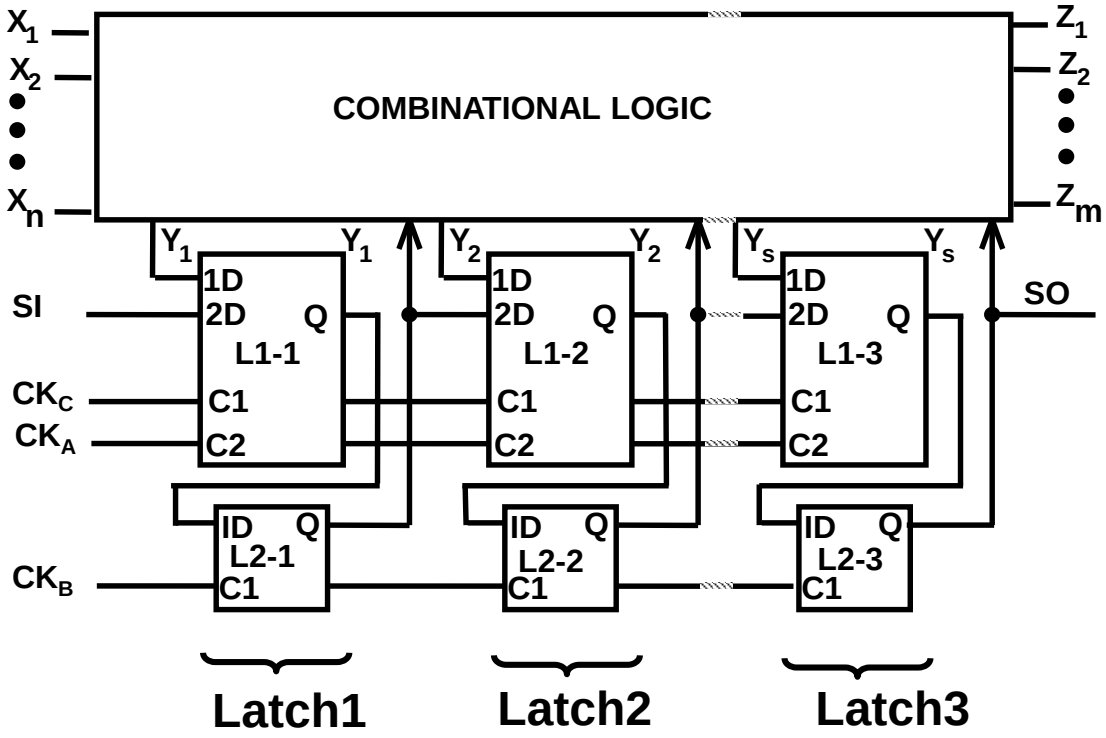
- One-pattern test
  - Shift: CK_A CK_B, CK_A CK_B , CK_A CK_B
  - Capture: CK_C
  - Shift: CK_B CK_A, CK_B CK_A, CK_B



Test Mode Operation (2)

- **One-pattern test**
  - Shift: CK_A CK_B, CK_A CK_B , CK_A CK_B
  - Capture: CK_C
  - Shift: CK_B CK_A, CK_B CK_A, CK_B





Summary of Three Internal Scans

- LSSD
  - ☺ No clock skew
  - popular for latch-based design

- Muxed D-Scan
  - ☺ Very popular for FF-based design
  - ☹ Speed degradation: one MUX delay (about 2 gate delay)
  - Adopted by most ASIC designs
- Clock Scan
  - ☺ Little speed degradation
  - ☹ Need extra clock routing for SCK
  - Adopted by advanced designs

FFT

- Q: how to apply 2-pattern test for LSSD?