VLSI Testing
積體電路測試

Design For Testability
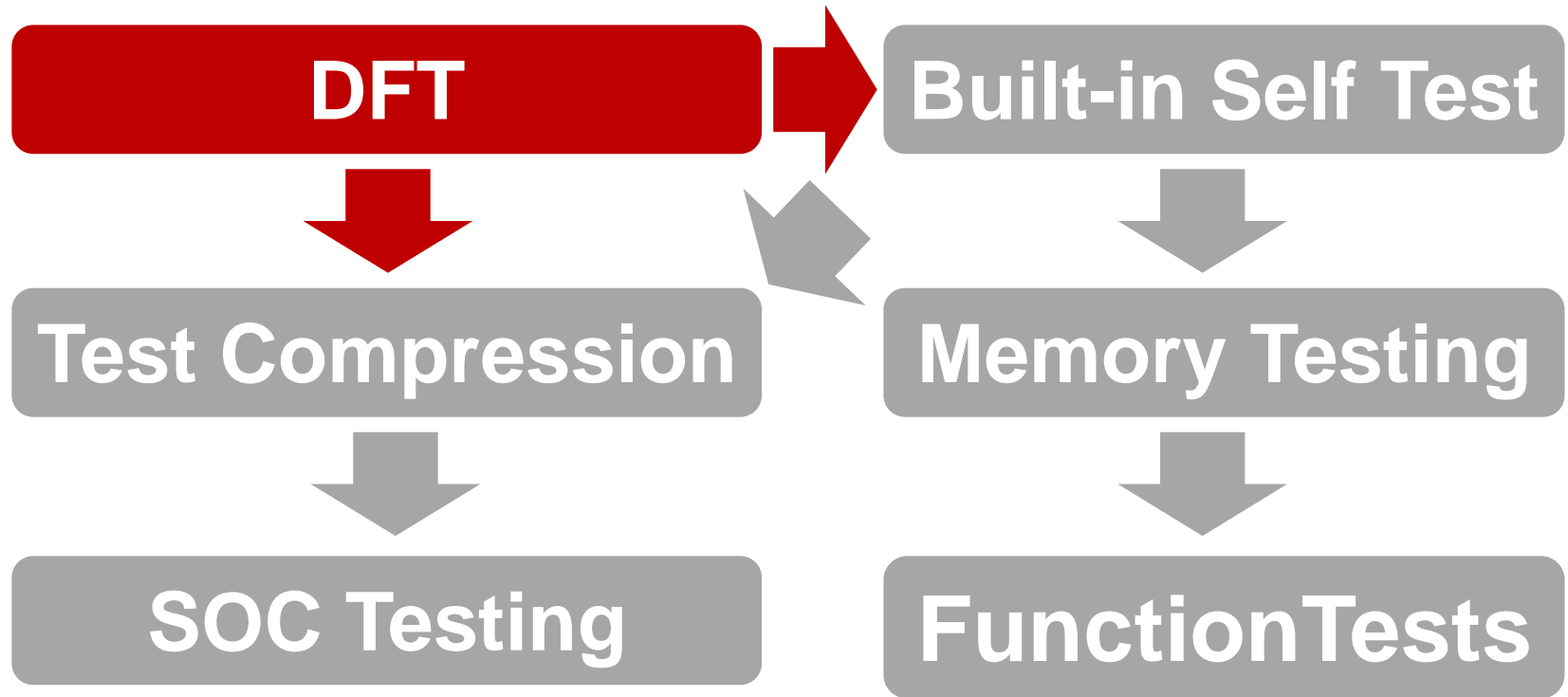## *Part 2: External Scan (JTAG)*

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Lab. of Dependable Systems
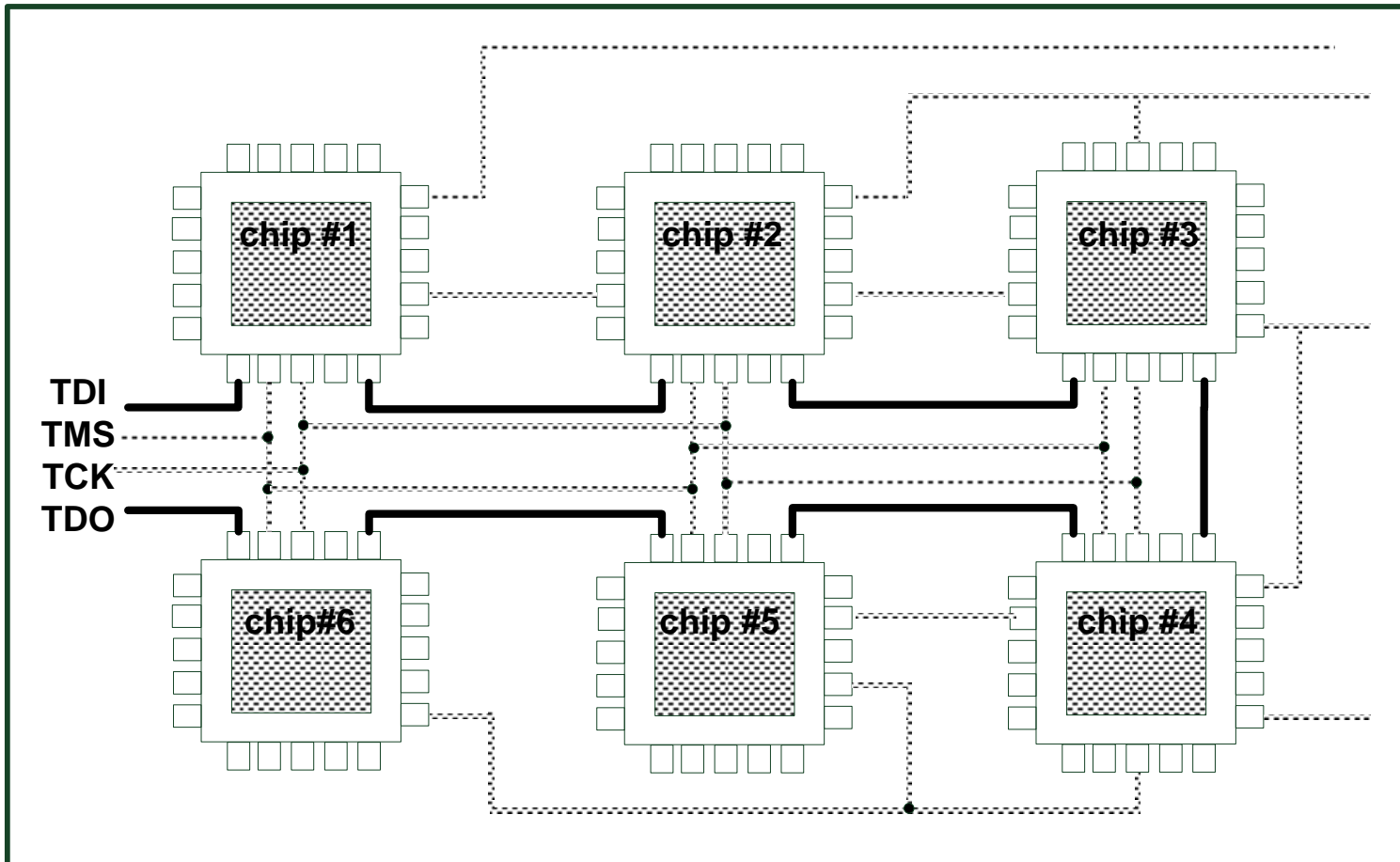
Graduate Institute of Electronics Engineering

National Taiwan University

Course Roadmap (Design Topics)

DFT → **Built-in Self Test**

Test Compression

Memory Testing

SOC Testing

FunctionTests

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Motivating Problem

- **You buy 6 chips and assemble a board**
  - **Your manager asks you to test the board and chips, how?**

Board

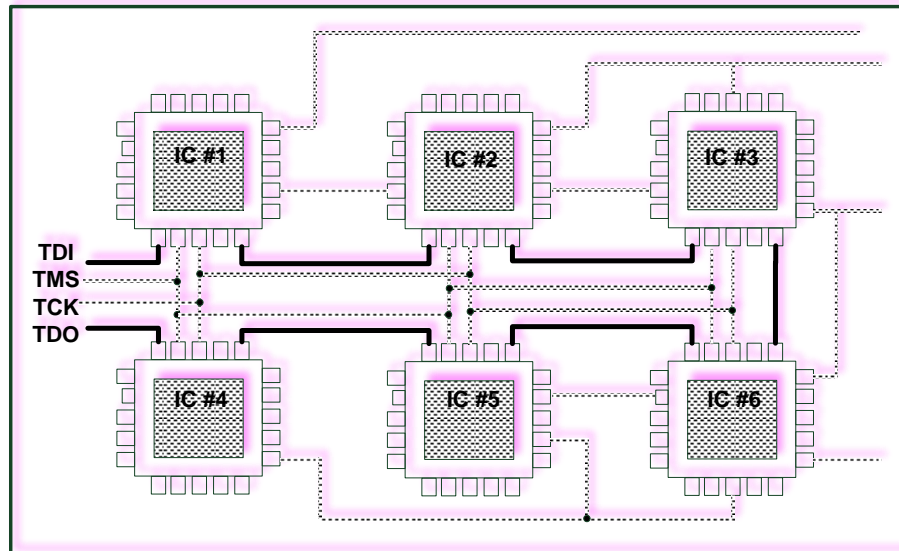University

Why Am I Learning This?

- **This chapter allows us to understand**
  - ♦ **JTAG, IEEE 1149.1 standard**
  - ♦ **board-level testing**

"In school we learn things then take the test, In life we take the test then learn things."
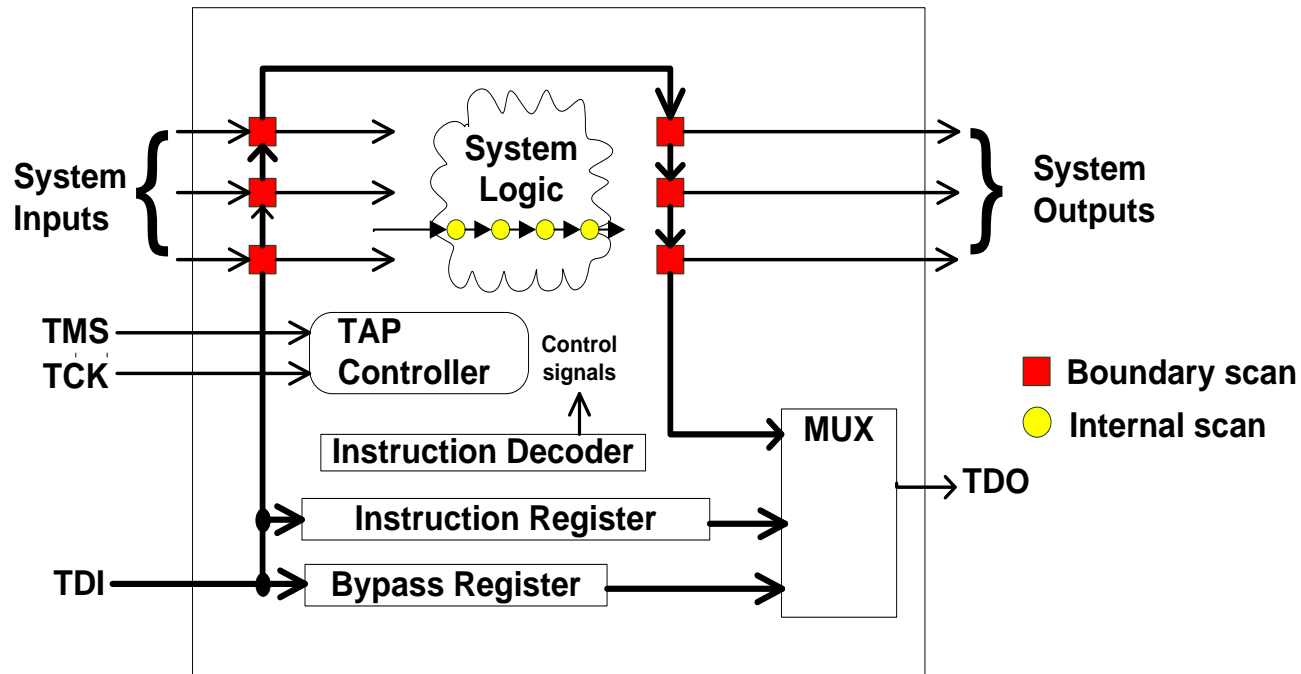
(Admon Israel)

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DFT – Part 2

- **Introduction**
- **JTAG Architecture and Components**
- **JTAG Instructions**
- **Conclusion**

What is External Scan ?

- **External scan**
  - ◆ **Stitch system input/output pins into a shift register**
    - ∗ **as opposed to *internal scan***
 - ◆ **also known as *boundary scan***

Boundary Scan

- **Boundary scan standard is needed**
  - **Allow chips from different vendors to be tested together**
- *IEEE 1149.1-1990*
  - *Boundary scan* **standard**
  - **aka *JTAG***
- **Why use boundary scan?**
  - **1. Board-level test and diagnosis**
  - **2. Test on-board interconnect among chips**
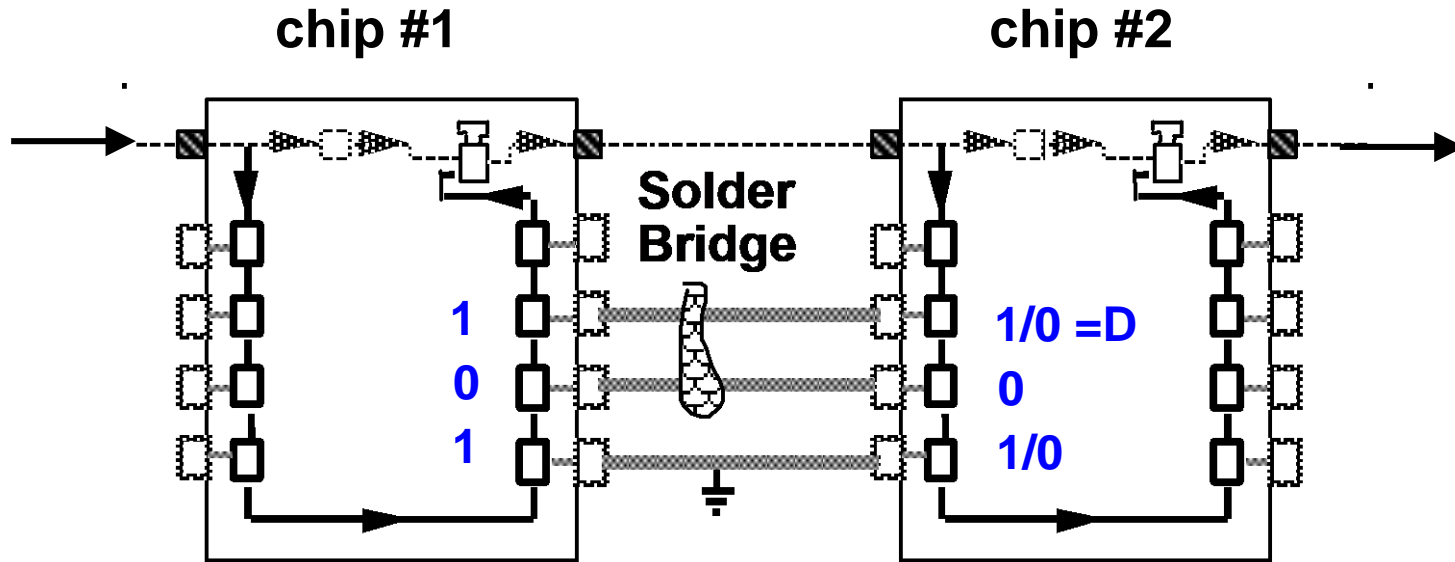 - **3. Test on-chip system logic**

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Board Level Test and Diagnosis

- All chips are stitched into one JTAG scan chain
- Off-line testing and on-line debug are supported

Board

University
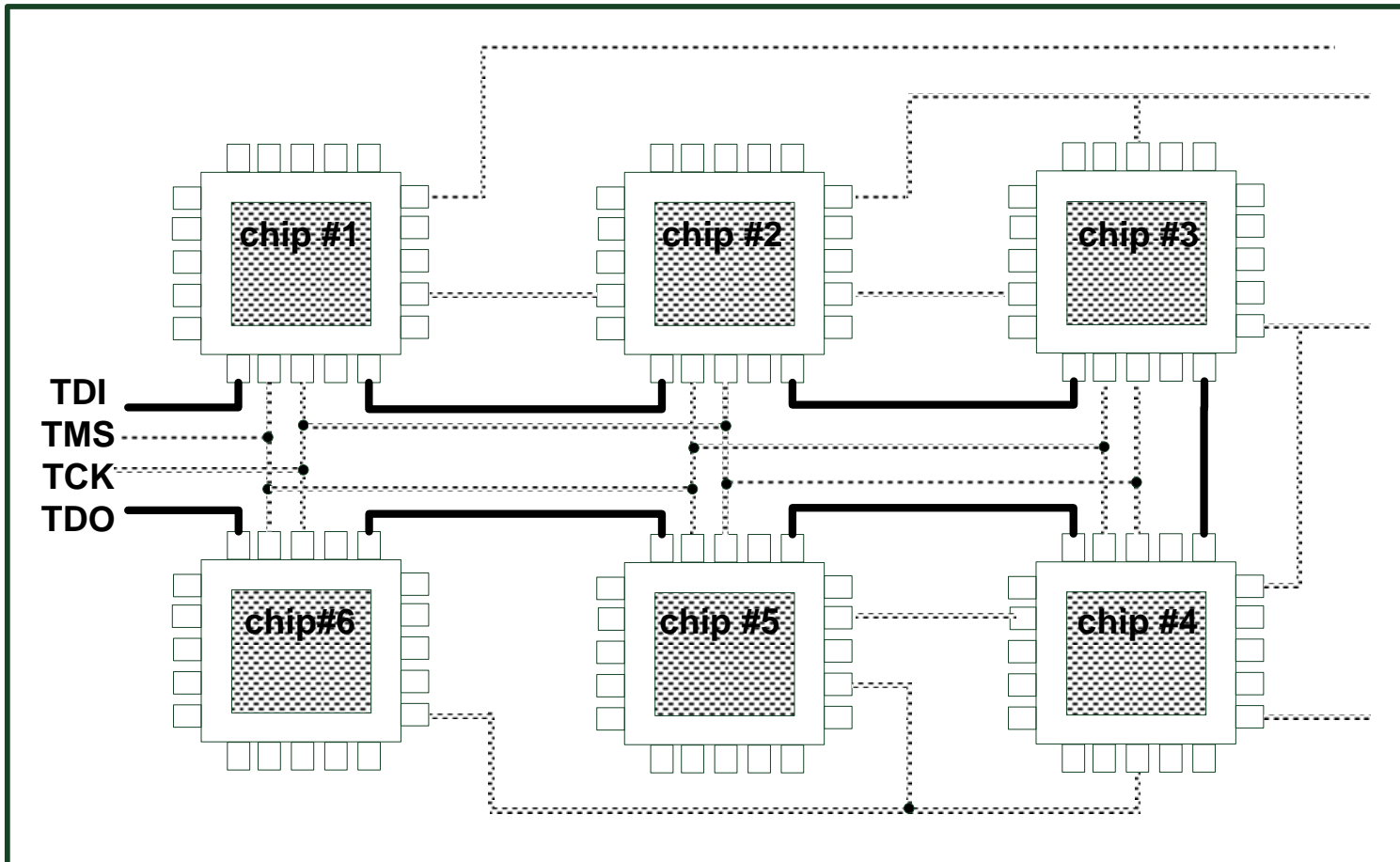
Test On-board Wires Among Chips

chip #1 **chip #2**

Solder Bridge

```
1          1/0 =D
0          0
1          1/0
```
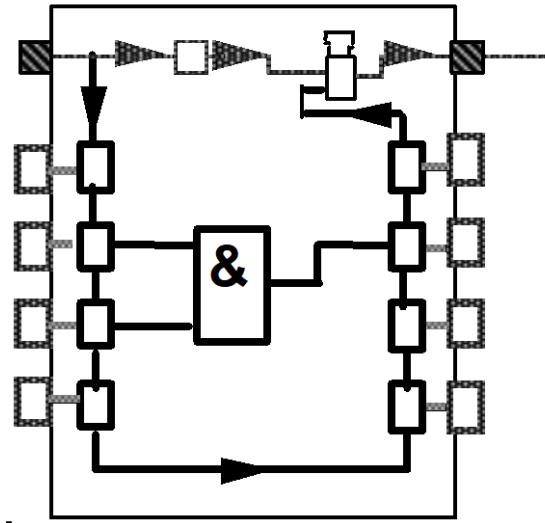
```
Input:    X X X X    1 0 1 X X X X X    X X X X  ← First scan in
Output:   X X X X    X X X X X D 0 D    X X X X  ← First scan out
```

*assume wired-AND fault model

Test On-chip System Logic

- **How to test a chip already assembled on board. Cannot use ATE**

First scan out

First scan in

```
Input:   X 1 1 X   X X X X        Good Output:  X X X X   X X 1 X
Input:   X 0 1 X   X X X X        Good Output:  X X X X   X X 0 X
Input:   X 1 0 X   X X X X        Good Output:  X X X X   X X 0 X
```
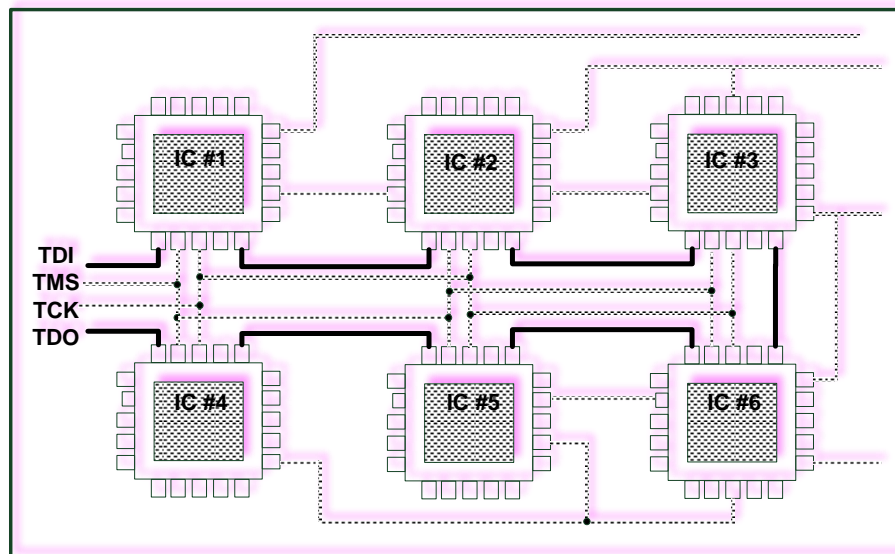
Quiz

Q: Which of the following is NOT true about boundary scan?
   A. Boundary scan enables board-level testing
   B. Requires standard because chips are from different vendors
   C. Boundary scan can replace internal scan

ANS:

DFT – Part 2

- **Introduction**
- **JTAG Architecture and Components**
  - ◆ **TAP**
  - ◆ **TAP controller**
  - ◆ Registers
  - ◆ Instruction Decoder
- JTAG Instructions
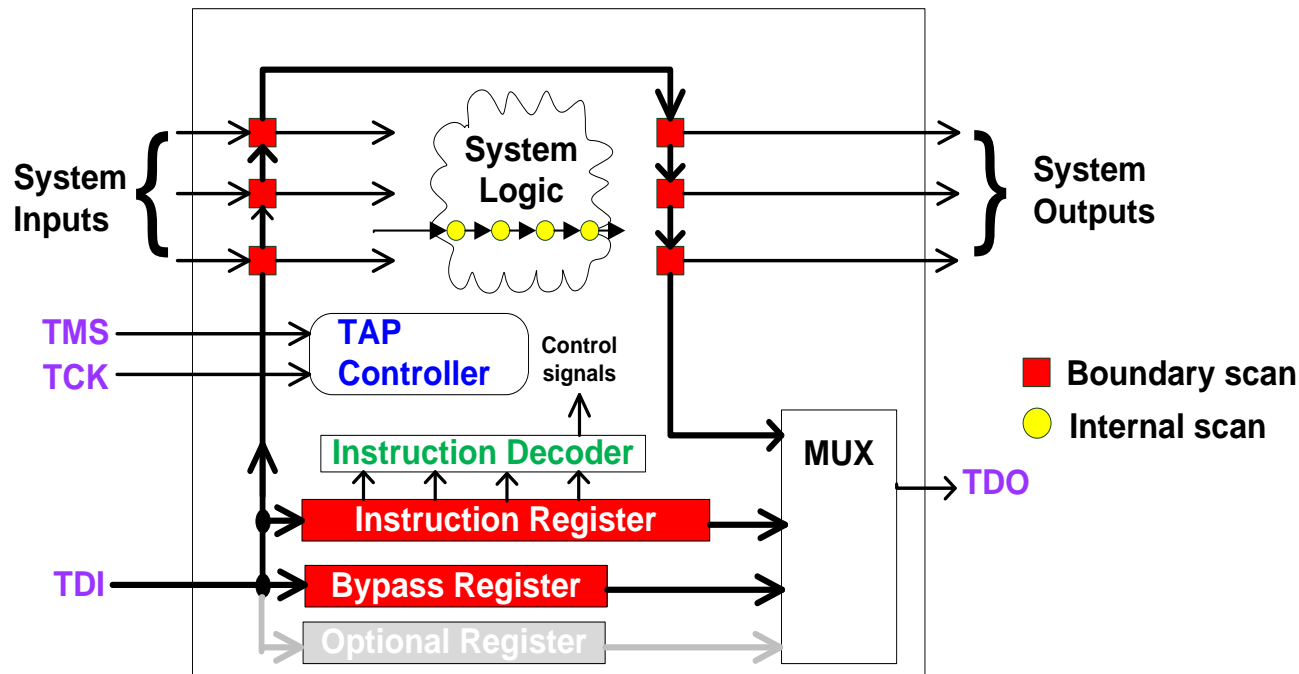- Conclusion

JTAG Architecture

- **JTAG Components**
  - ♦ **1. Test Access Port (TAP)**
  - ♦ **2. TAP controller**
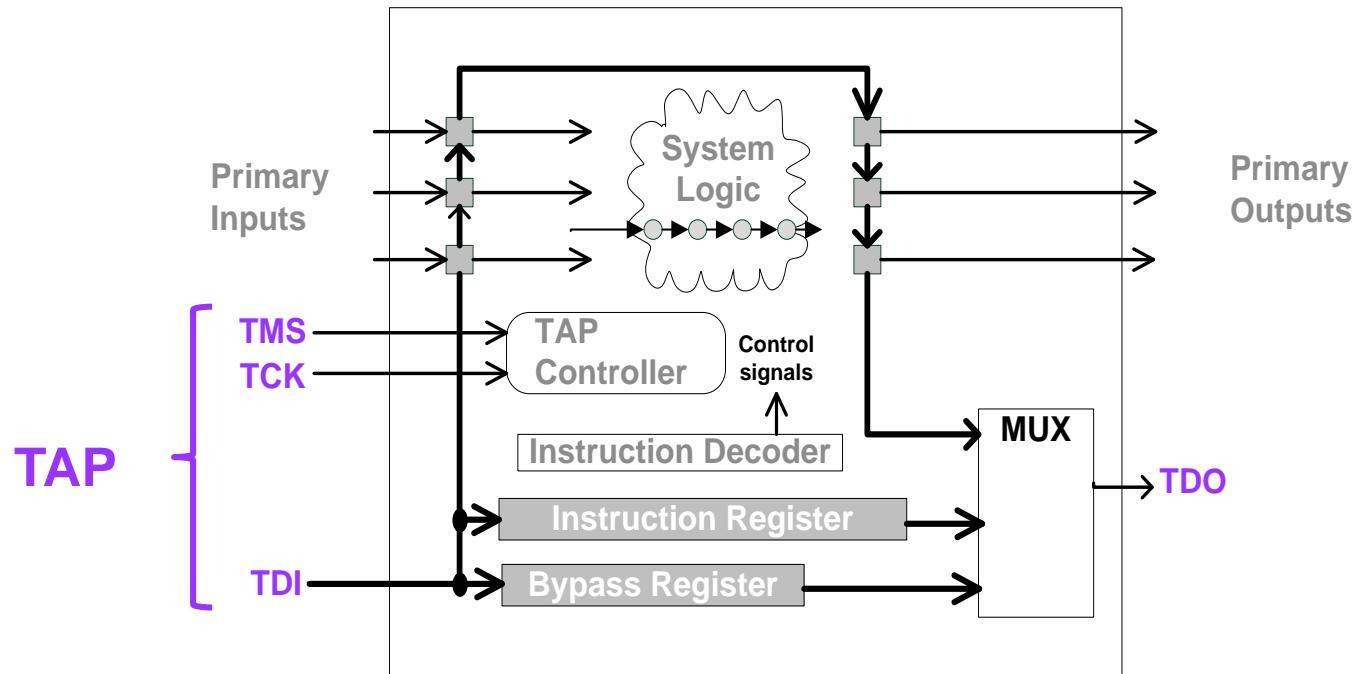 - ♦ **3. Registers**
    - ∗ **Instruction Register, Boundary Scan Register, Bypass Register…**
  - ♦ **4. Instruction Decoder**
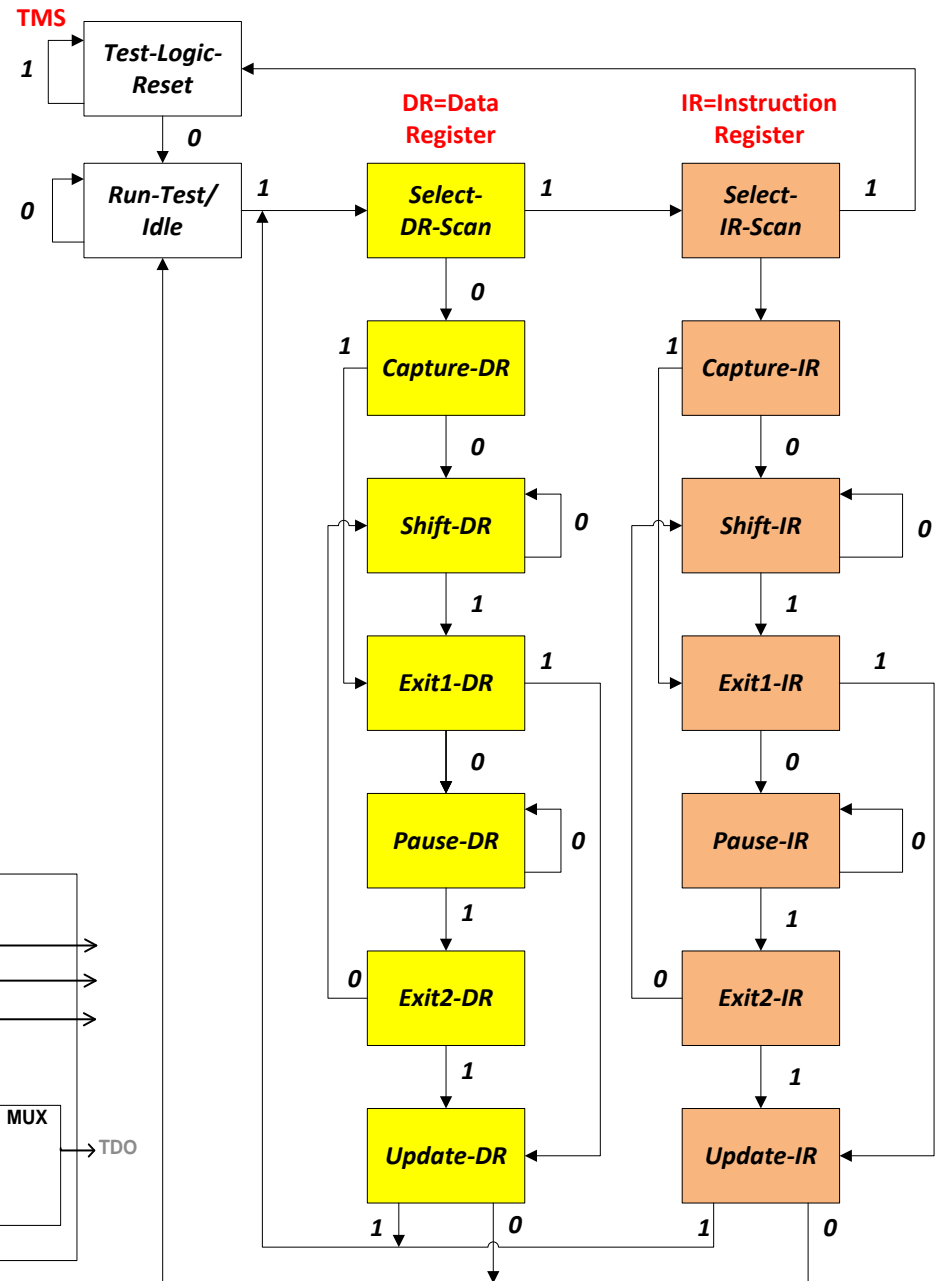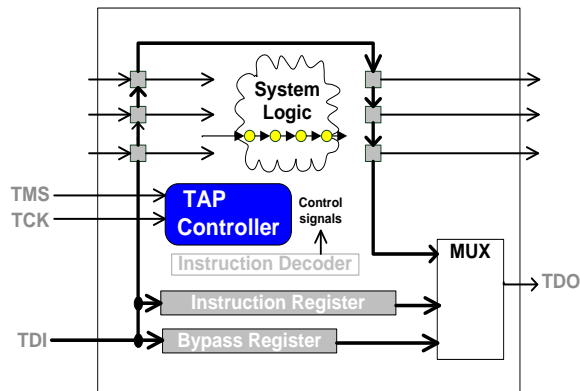
Test Access Port, TAP

- **4 mandatory TAP**
  - ♦ *TDI, Test Data Input*
  - ♦ *TDO, Test Data Output*
  - ♦ *TCK, Test Clock*
  - ♦ *TMS, Test Mode Select*

- **1 optional TAP**
  - ♦ **TRST**, **Reset of Test Logic (Active Low)**

TAP Controller

- **Control JTAG operation**
- **16-state Finite State Machine**
  - ◆ **Clock is TCK**
  - ◆ **Input is TMS**
- **Test-Logic-Reset**
  - ◆ **Reset JTAG Circuits**
  - ◆ **How to reset JTAG?**
    - ∗ **TMS=111..., or**
    - ∗ **TRST = 0**

**Note:
State transition
occurs at rising
edge of TCK**

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Summary

- *IEEE 1149.1-1990*
  - *Boundary scan* standard
  - aka *JTAG (Joint Test Action Group)*
- Why use boundary scan?
  - Board-level, interconnect, system logic
- JTAG components
  - 1. Test Access Port (TAP)
  - 2. TAP controller (16-state FSM)
  - 3. Registers
  - 4. Instruction Decoder

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FFT

- **Q: What is mini number of 1's needed to initialize JTAG? Regardless of initial state.**
  - ◆ **TMS=111…**

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