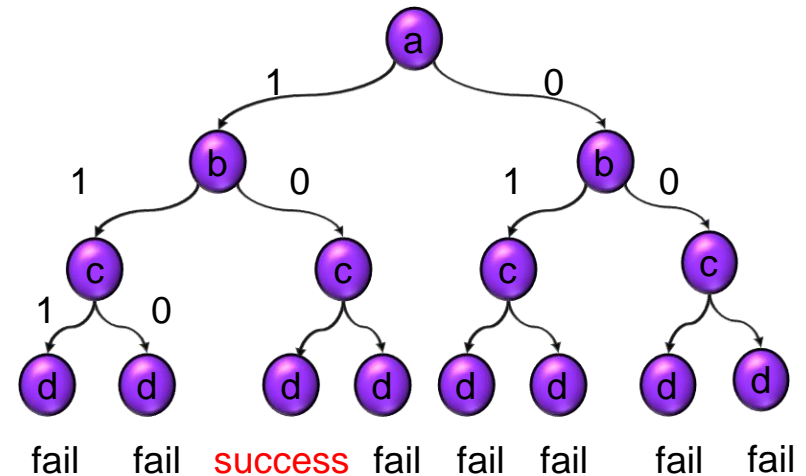# Combinational ATPG

- **Introduction**
- **Deterministic Test Pattern Generation**
  - Boolean difference *
  - Path sensitization **
  - D-Algorithm [Roth 1966]**
  - PODEM [Goel 1981]**
  - FAN [Fujuwara 1985]**
  - **SAT-based [Larrabee 92] ***
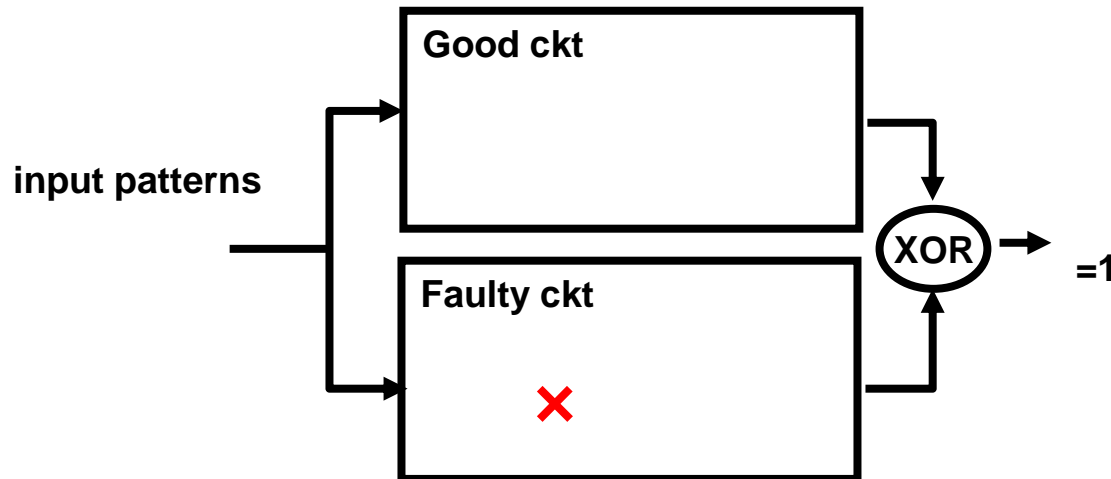- Acceleration techniques
- Concluding Remarks

*Boolean-based methods
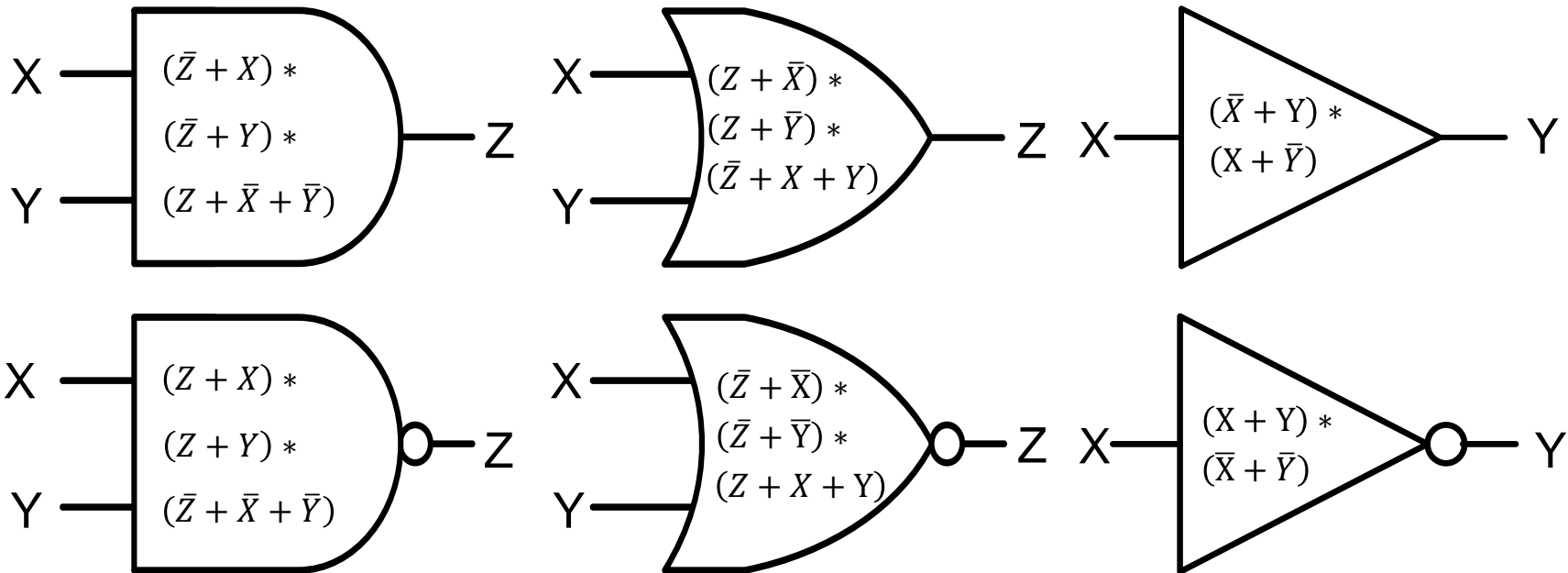**path-based methods

SAT-based ATPG

- **Idea: convert test generation problem into *satisfiability problem***
    - **Solve for a set of inputs such that**
    - **(good output) XOR (faulty output) = 1**

this is called a *miter*

Tseitin Transformation [Tseitin 66]

- **Converts circuit into *Conjunctive Normal Form (CNF)***
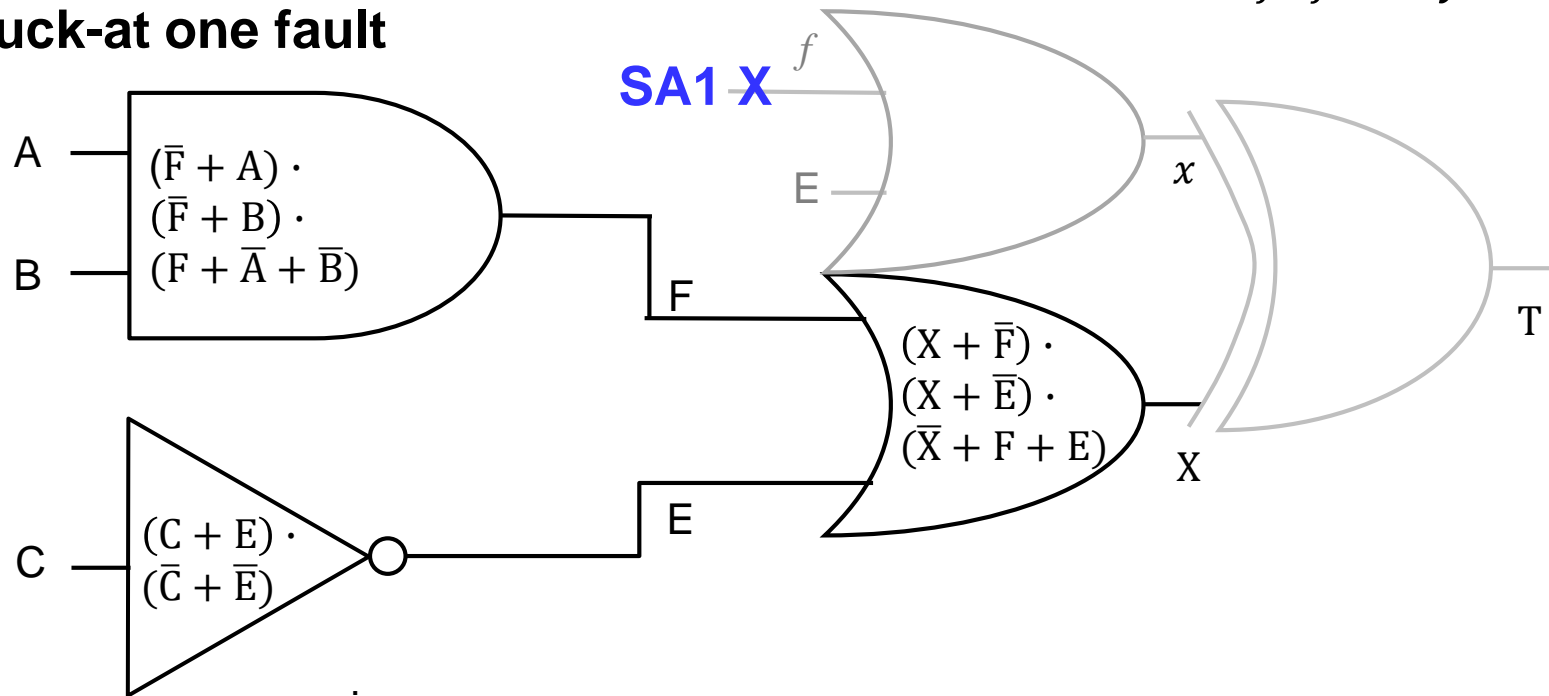 - ♦ **linear time, linear number of clauses and literals**

X —
$(\bar{Z} + X) *$
$(\bar{Z} + Y) *$
$(Z + \bar{X} + \bar{Y})$
Y — — Z

X —
$(Z + \bar{X}) *$
$(Z + \bar{Y}) *$
$(\bar{Z} + X + Y)$
Y — — Z

X —
$(\bar{X} + Y) *$
$(X + \bar{Y})$
— Y

X —
$(Z + X) *$
$(Z + Y) *$
$(\bar{Z} + \bar{X} + \bar{Y})$
Y — — Z

X —
$(\bar{Z} + \bar{X}) *$
$(\bar{Z} + \bar{Y}) *$
$(Z + X + Y)$
Y — — Z

X —
$(X + Y) *$
$(\bar{X} + \bar{Y})$
— Y

CNF for basic gates

3

Example (cont'd)

F good
f faulty

- **F stuck-at one fault**

SA1 X

A — $(\bar{F} + A) \cdot$
$(\bar{F} + B) \cdot$
B — $(F + \bar{A} + \bar{B})$

F

f

E

x

$(X + \bar{F}) \cdot$
$(X + \bar{E}) \cdot$
$(\bar{X} + F + E)$

X

T

C — $(C + E) \cdot$
$(\bar{C} + \bar{E})$

E

faulty $\left(x + \bar{f}\right) \cdot (x + \bar{E}) \cdot (\bar{x} + f + E) \cdot (f)$

good
$\cdot (C + E) \cdot (\bar{C} + \bar{E})$
$\cdot (X + \bar{F}) \cdot (X + \bar{E}) \cdot (\bar{X} + F + E)$
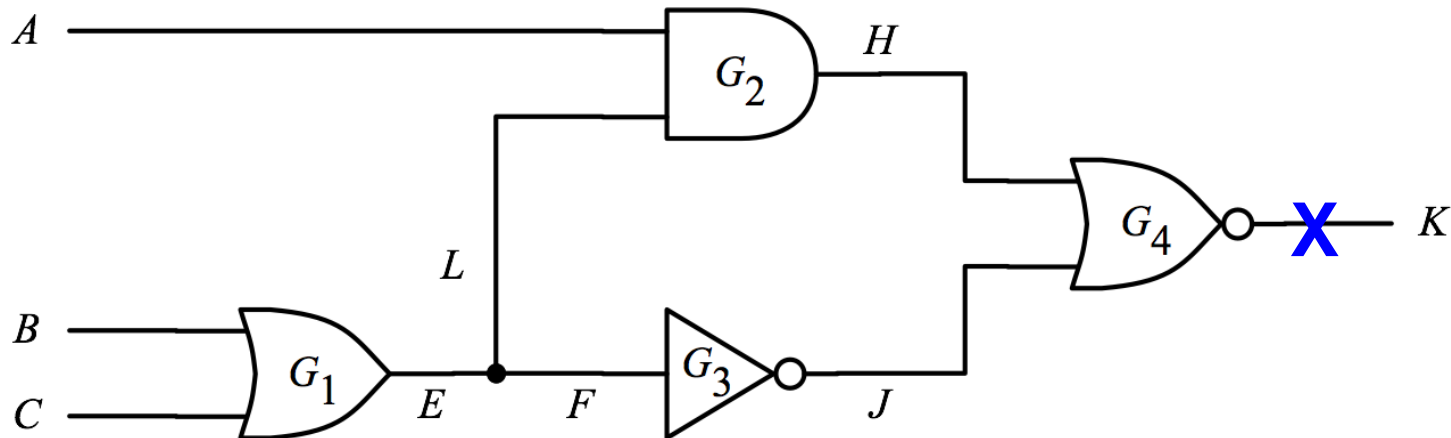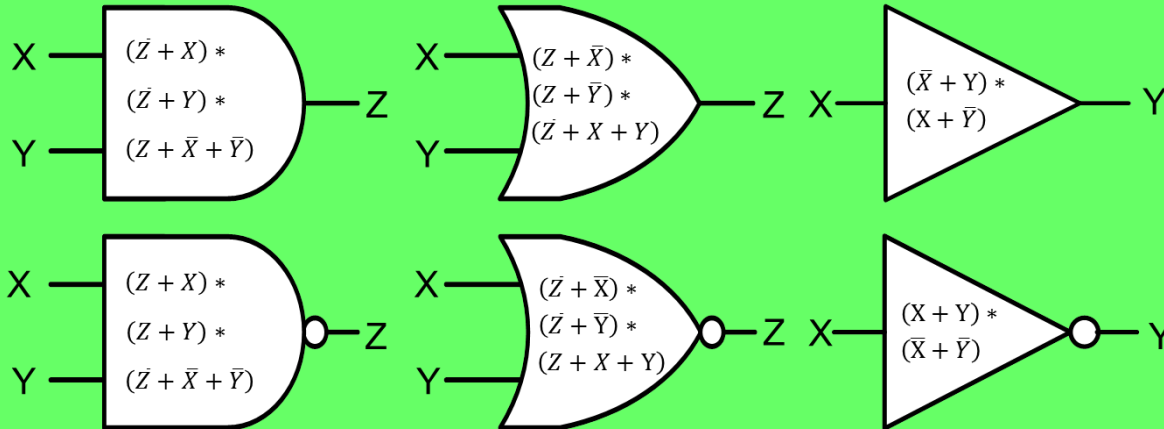$\cdot (\bar{F} + A) \cdot (\bar{F} + B) \cdot (F + \bar{A} + \bar{B})$

=1

XOR
$\cdot (\bar{X} + x + T) \cdot (X + \bar{x} + T)$
$\cdot (\bar{X} + \bar{x} + \bar{T}) \cdot (X + x + \bar{T}) \cdot T$

4

Quiz

Q: Please write CNF to generate a test for K stuck-at one fault

A:

Pros and Cons

- **SAT-based ATPG**
  - + **SAT engine is making big progress recently**
  - + **proves untestable faults if CNF is unsatisfiable**
  - − **does not allow don't cares in input**
  - − **needs to redo CNF every time a target fault is injected**
  - − **does not preserve circuit structure information**
  - − **difficult for multi-valued logic (such as high impedance)**

SAT-based ATPG Not Used in Commercial Tool