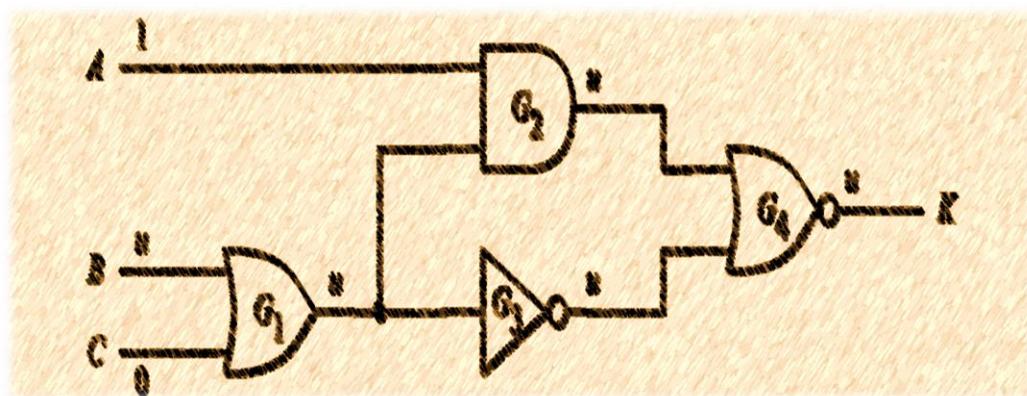
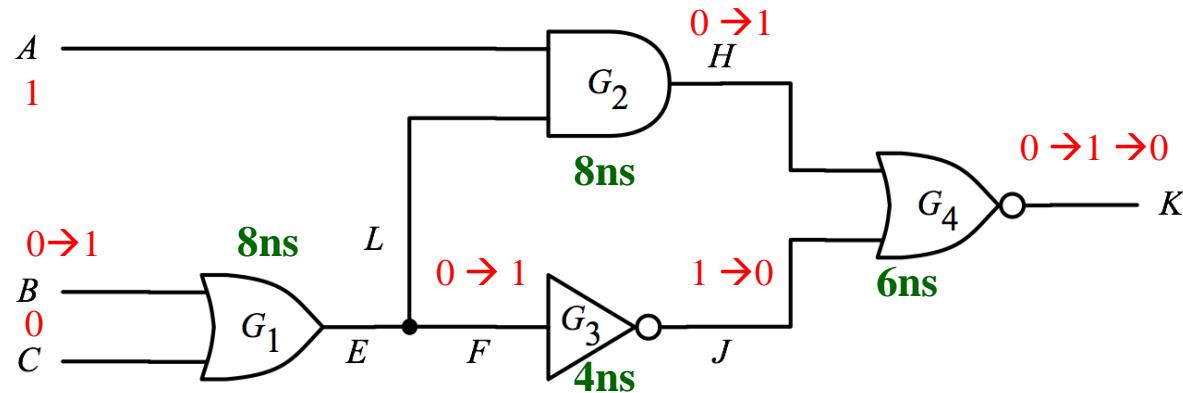


Logic Simulation

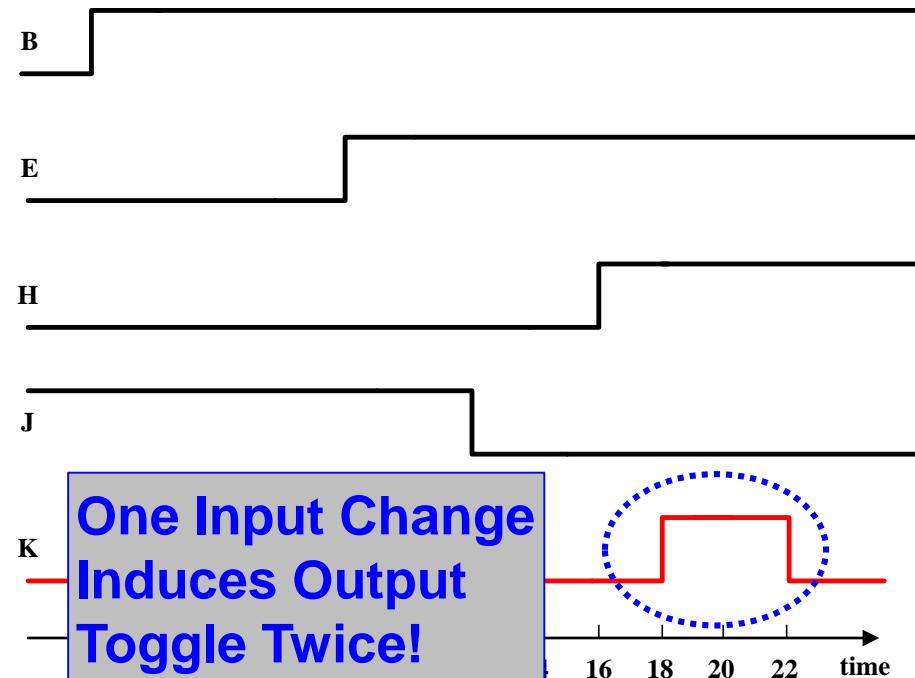
- Introduction
- Simulation Models
- Logic Simulation Techniques
- Issues of Logic Simulations
 - ◆ Hazards
 - ◆ Oscillation
- Conclusions



Quiz Review

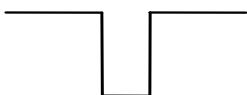


t	L_E	L_A	Scheduled events
0	(B,1)	G_1	(E,1)@8
2			
4			
8	(E,1)	G_2, G_3	(H,1)@16; (J,0)@12
10			
12	(J,0)	G_4	(K,1)@18
14			
16	(H,1)	G_4	(K,0)@22
18	(K,1)		
22	(K,0)		

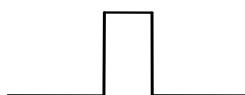


Hazard [Huffman 57] [McCluskey 62]

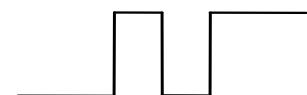
- Hazard : Output signal waveform depends on
 - ◆ (Internal) circuit delay and (external) input signal change
- Two types of hazards:
 - ① **Static hazard:** A momentary change of gate output that does not cause the steady gate output to change
 - ◆ Static-1 hazard: steady output is 1
 - ◆ Static-0 hazard: steady output is 0
 - ② **Dynamic hazard:** A momentary change of gate output during rising or falling transition (no more details in this lecture)



static-1
hasard



static-0
hasard



dynamic-1
hasard

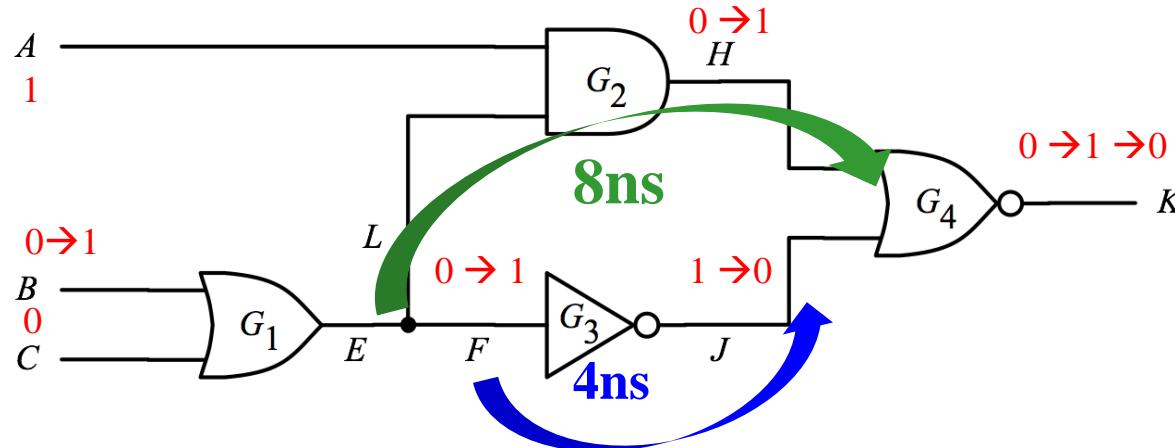


dynamic-0
hasard

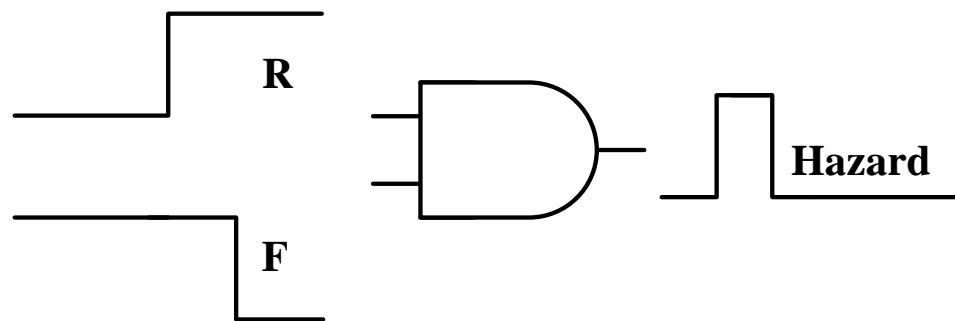
Hazard also called *glitch, spike*

Why Hazard?

- ① **Logic hazard**: signal change reconverge with different timing

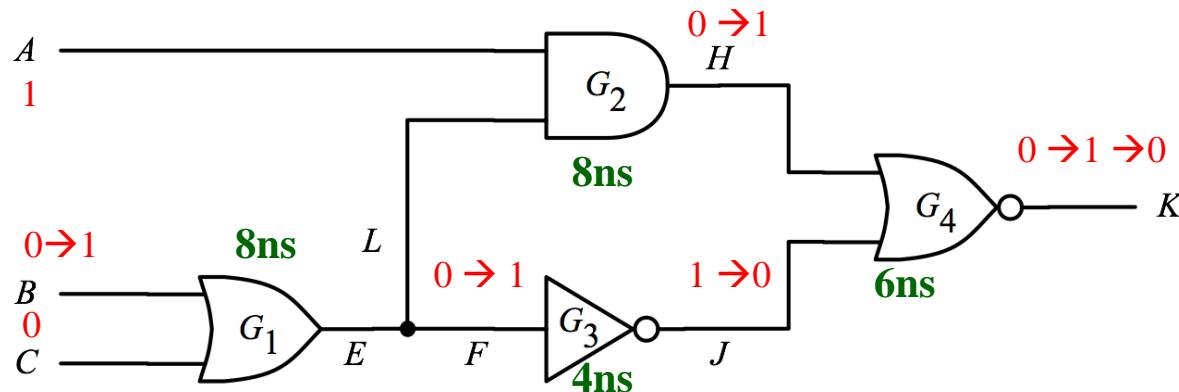


- ② **Function hazard**: more than one input changes



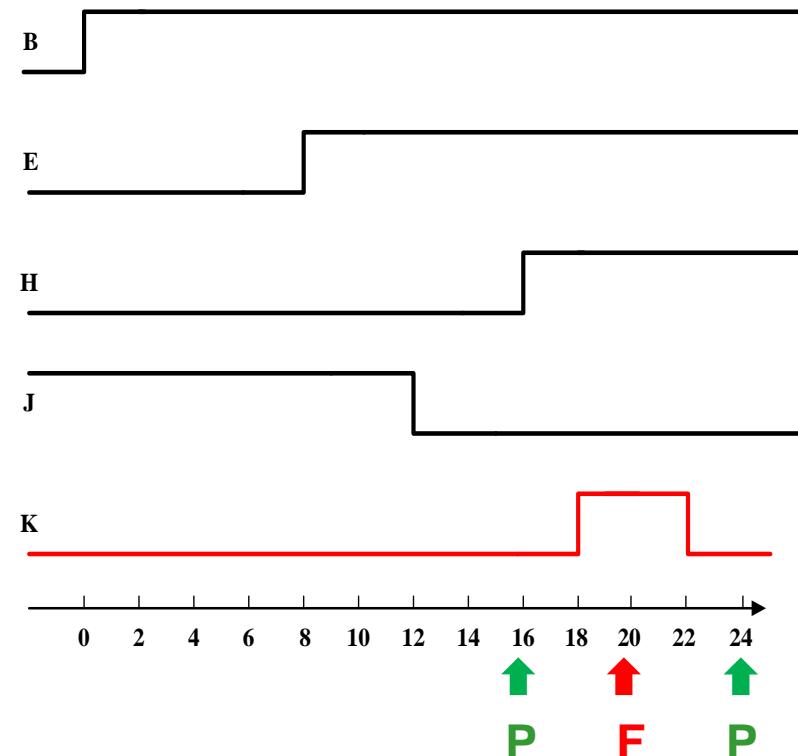
Logic Hazard Can be Improved by Circuit Design;
Function Hazard Cannot.

Test Timing Is Important



- **Strobe time** = time to observe output
- Example: expect output = 0
 - ◆ Strobe time = 16 → pass
 - ◆ Strobe time = 20 → fail
 - ◆ Strobe time = 24 → pass

Need to Consider Hazards
to Decide Test Timing



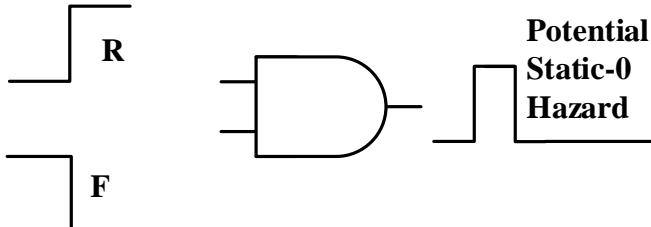
How to Detect Hazard?

- Event-driven simulation is too slow
- **Six-valued Logic** is used to detect potential static hazards

Value	Meaning
0	Static 0
1	Static 1
R	Rising transition, $0 \rightarrow 1$
F	Falling transition, $1 \rightarrow 0$
0^*	Static-0 hazard
1^*	Static-1 hazard

AND	0	1	R	F	0^*	1^*
0	0	0	0	0	0	0
1	0	1	R	F	0^*	1^*
R	0	R	R	0^*	0^*	R
F	0	F	0^*	F	0^*	F
0^*	0	0^*	0^*	0^*	0^*	0^*
1^*	0	1^*	R	F	0^*	1^*

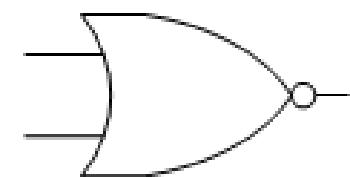
6-valued simulation cannot determine **for sure** if there is a hazard or not.
It can only indicate “potential” hazards.



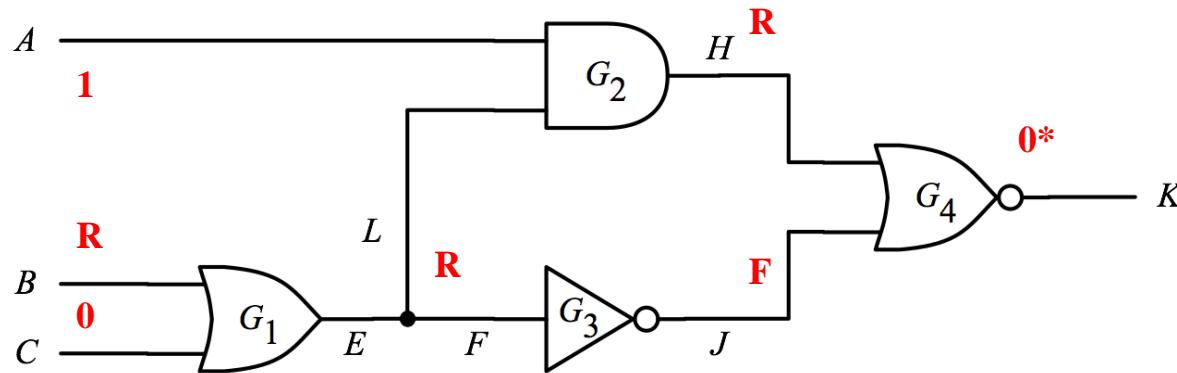
Quiz

Q: Please fill in 6-valued table for NOR gate
A:

NOR	0	1	R	F	0*	1*
0	1	0	F	R	1*	0*
1	0	0	0	0	0	0
R	F	0				0*
F	R	0				0*
0*	1*	0				0*
1*	0*	0	0*	0*	0*	0*



Apply 6-valued Simulation



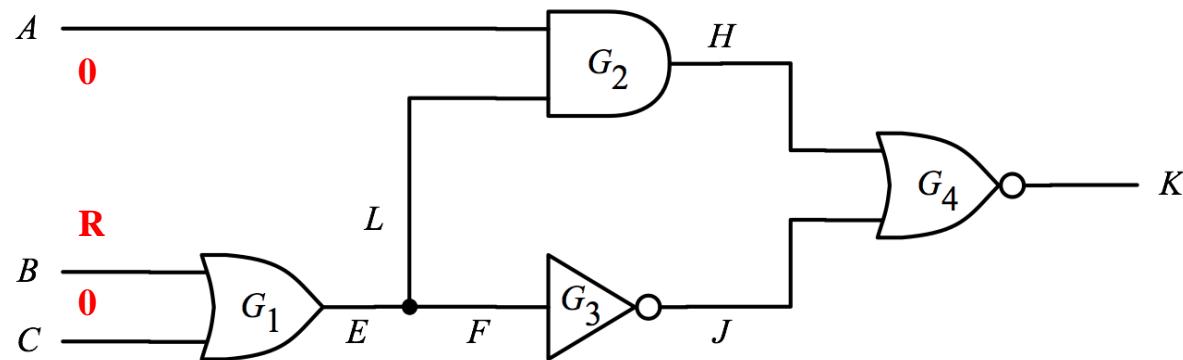
AND	0	1	R	F	0*	1*
0	0	0	0	0	0	0
1	0	1	R	F	0*	1*
R	0	R	R	0*	0*	R
F	0	F	0*	F	0*	F
0*	0	0*	0*	0*	0*	0*
1*	0	1*	R	F	0*	1*

NOR	0	1	R	F	0*	1*
0	1	0	F	R	1*	0*
1	0	0	0	0	0	0
R	F	0	F	0*	F	0*
F	R	0	0*	R	R	0*
0*	1*	0	F	R	1*	0*
1*	0*	0	0*	0*	0*	0*

Quiz

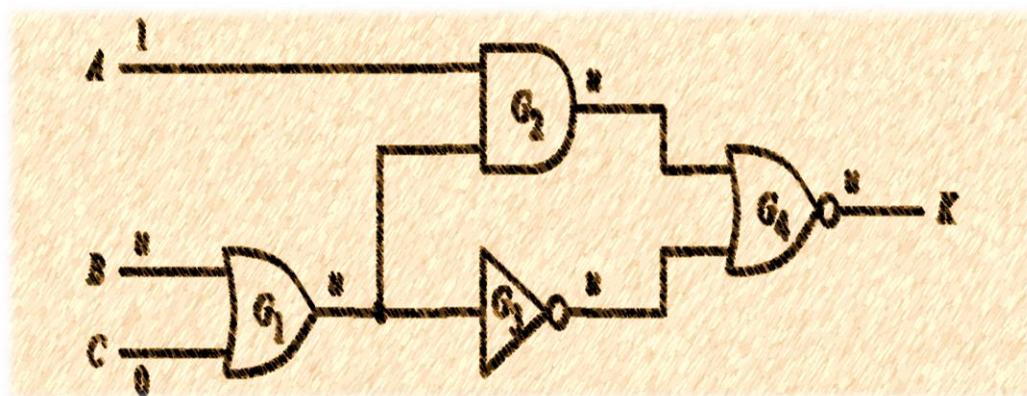
Q: Please run 6-valued simulation to determine whether there is static hazard on output?

A:



Logic Simulation

- Introduction
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- Issues of Logic Simulations
 - ◆ Hazards
 - ◆ Oscillation
- Conclusions

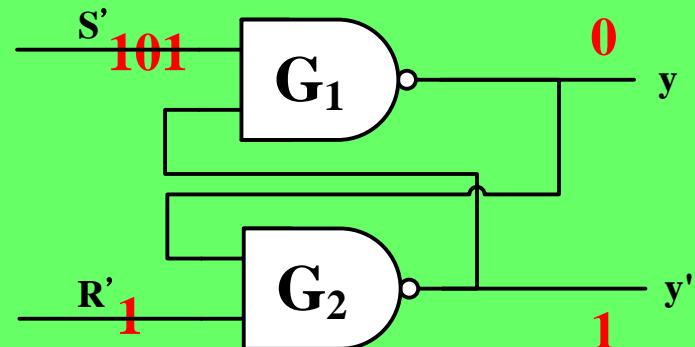


Quiz

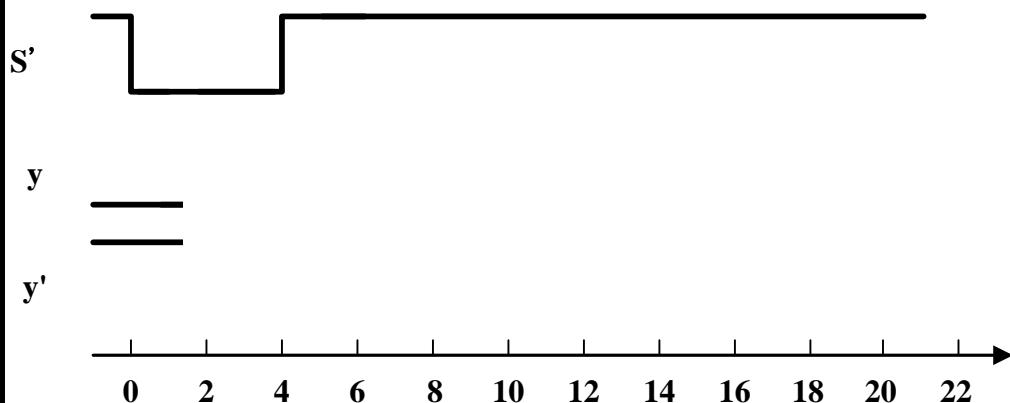
Q: Simulate this circuit with initial values

$$S'=1, R'=1, y=0, y'=1$$

Draw output waveforms.

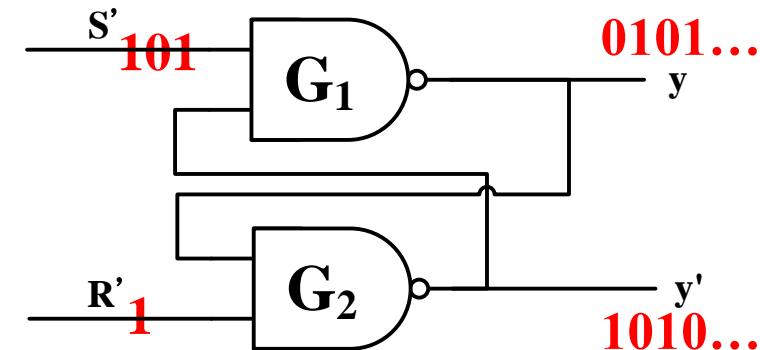


t	L_E	L_A	Scheduled events
0	(S', 0)		
4	(S', 1)		y'
11			

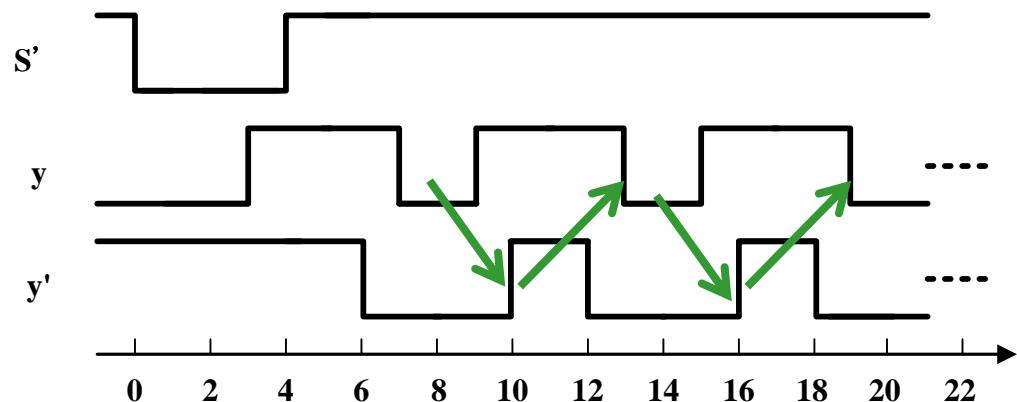


Oscillation

- This is RS-latch with inverted inputs
- RS-latch is oscillating



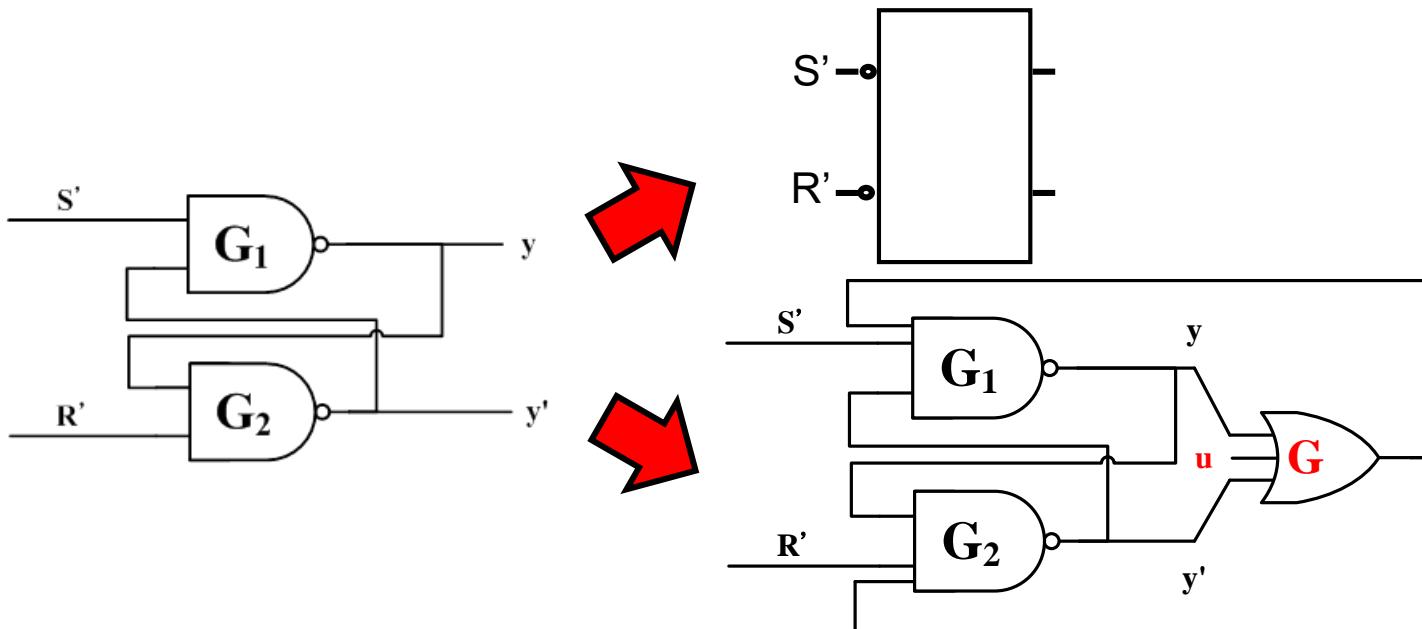
S'	R'	y	y'
0	1	1	0
1	0	0	1
1	1	Last state	Last State
0	0	forbidden	forbidden



Simulator Must Stop Oscillation. How?

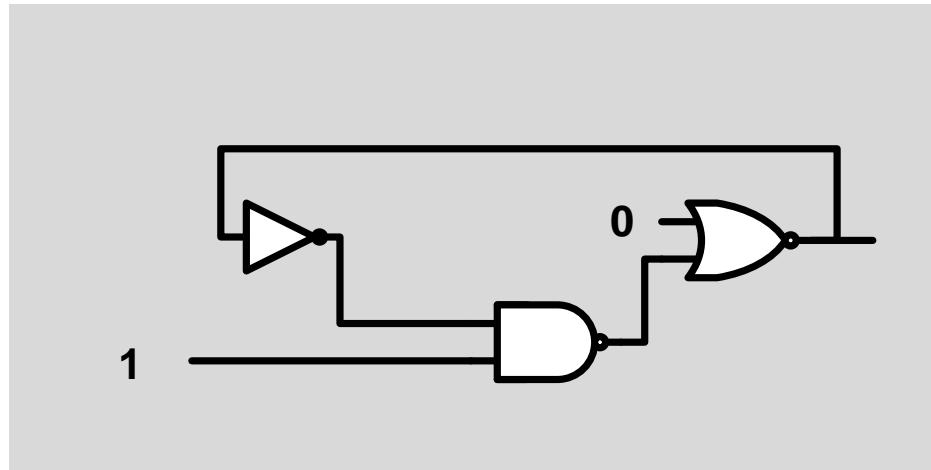
Local Oscillation Control

- Two methods:
 - 1) Monitor user-specified conditions on latches/FF
 - * Example: when $y=y'=0$, simulator forces $y = u$, $y' = u$
 - 2) Oscillation control via modeling
 - * Example: when $y = y' = 0$, $G = u$, $y = y' = u$, oscillation stops
 - * Example: replace it by SR-latch



Global Oscillation Control

- Count events occurring after any primary input change
- If number of events exceeds specified limit
 - ◆ Stop simulation and report warning
- Global feedback loop also cause fault sim./test gen. problem
 - ◆ see fault simulation 5.7



Global Feedback Should be Avoided

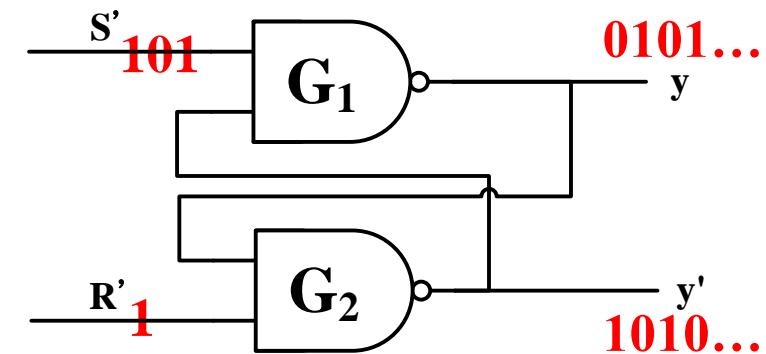
Conclusions

- Types of Hazards
 - ◆ **Static-0 hazard, static-1 hazard**
 - ◆ **Dynamic-0 hazard, dynamic-1 hazard**
- Why hazard?
 - ◆ **Logic hazard:** signal reconverges with differing timing
 - ◆ **Function hazard:** multiple input change
- **6-valued simulation** can detect potential hazard
 - ◆ without event-driven simulation
- Oscillation should be suppressed by simulator
 - ◆ Local/Global oscillation control

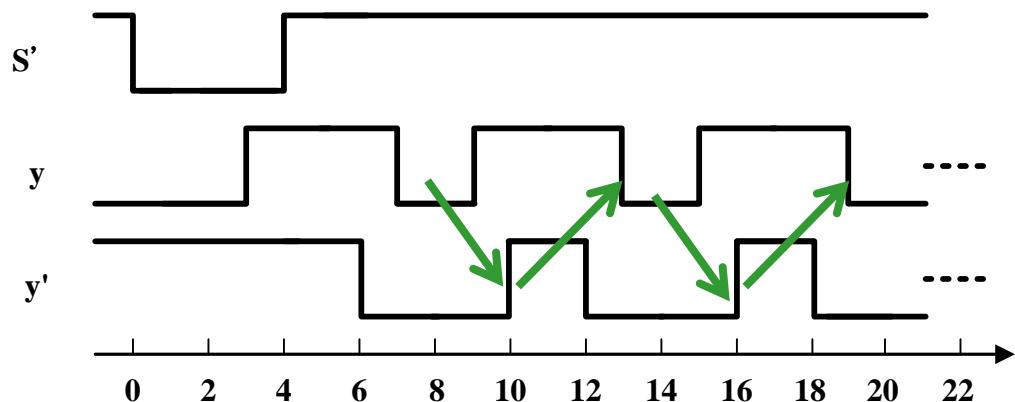
Logic Sim. is Building Block for Many EDA Tools

FFT

- Q: what would happen in real circuits?



S'	R'	y	y'
0	1	1	0
1	0	0	1
1	1	Last state	Last State
0	0	forbidden	forbidden



References

- [Huffman 1957] D. A. Huffman, “Design and Use of Hazard-free Switching Networks,” J. ACM 4, pp.47, 1957.
- [McCluskey 1962] E.J. McCluskey, “Transients in Combinational Logic Circuits,” Redundancy Techniques for Computing Systems, pp.9-46, Spartan Book, 1962.
- [Ulrich 1965] Ulrich, “Time sequenced logical simulation based on circuit delay and selective tracing of active network paths”, ACM Nat'l Conference, pp.437-448, 1965.