VLSI Testing
積體電路測試

Advanced Topics

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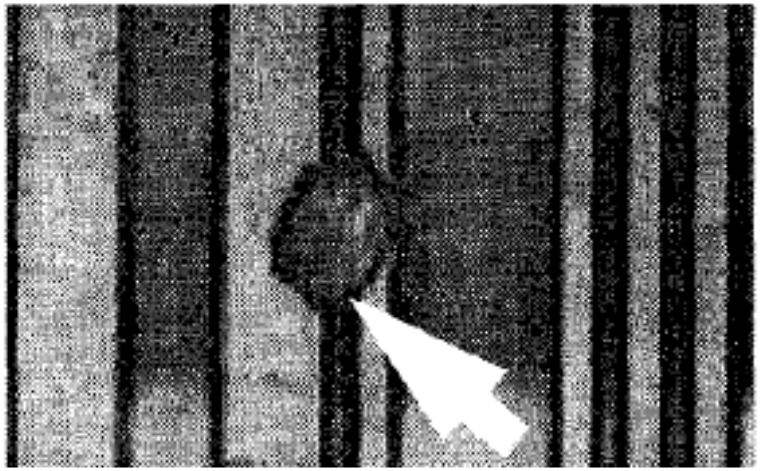
Why Am I Learning This?

- Your manager asks you
  - "We already apply test patterns of 100% fault coverage, why can't we achieve 0 DPM?"
  - "We are entering the automobile market, how to reduce test escapes?"

"When you have faults,
do not fear to abandon them."
過則勿憚改
(Confucius)

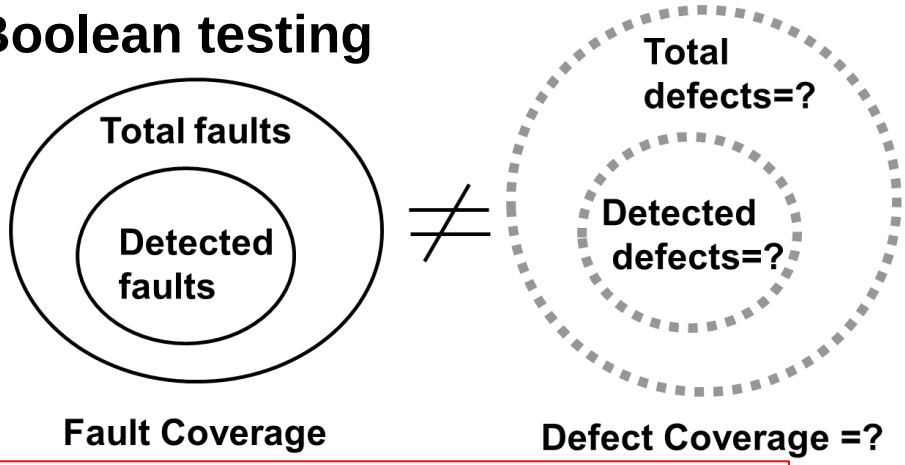
Outline

- Introduction
  - Defect Categories
- Defect-based Testing
- Advanced ATPG
- Conclusion



100% FC ≠ 0 DPM

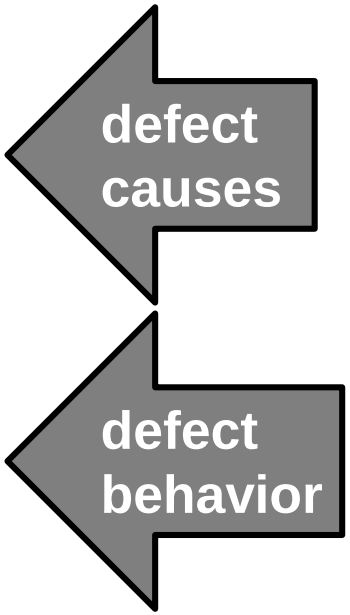
- In theory, DL =1-Y$^{(1-FC)}$
  - but fault coverage does ***NOT*** represent defect coverage
- Experimental results [Stanford CRC]
  - Total 5.5K chips tested by many kinds of test sets
    - 116 defective chips, up to 6 escaped 100% SSF test sets
- Example of test escapes
  - High impedance bridging defect
    - Cause abnormal static current
    - May not detectable by Boolean testing



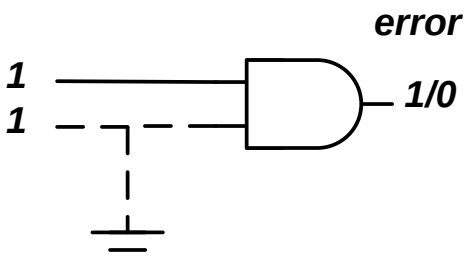
Must Understand Defects Better to Test Them

Defects

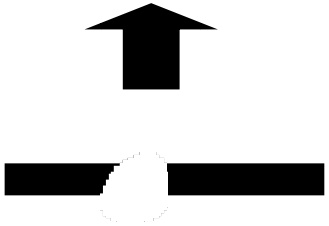
- *Defect*
  - Unintended physical difference between hardware implementation and its intended design
  - Example: unwanted wire (short to ground)
- *Failure Mechanism*
  - *Physical* or *chemical* process that cause defects
  - Examples: Dust particle falling on wafer
- *Failure Mode*
  - Causes or possible ways a device can fail
  - Examples:
    - Opens, Shorts
    - *Parametric*
      - V_t shift
      - Transistor transconductance (R_{on} , R_{off}) changed
      - Contact resistance, wire resistance increased



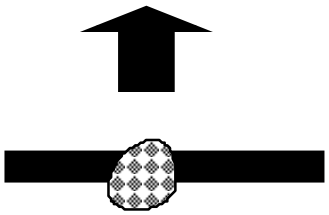
Different Levels of Terminology



SA 0 Fault



Open Metal Wire



Particle on Mask

signal

logic circuit

open/short/parametric

physical/chemical

Error

Fault

Fault modeling

Failure mode

defects

Failure mechanism

Quiz

Q: Which of following is failure mechanism?

A: a metal wire is open

B: a particle dust falling on mask

C: a transistor R_{on} is too high

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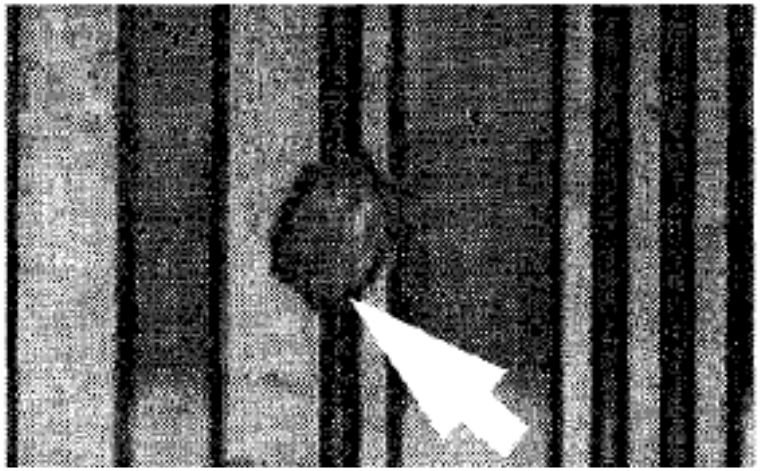
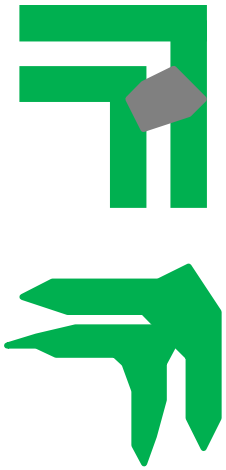
- Introduction
  - Defect Categories
    - Oxidation
    - Metallization
    - Wire Bonding / Packaging
    - Overstress
    - Others: Reliability
- Defect-based Testing
- Advanced ATPG
- Conclusion



Defect Categories

- Classified by occurrence
  - Random defects
    - Caused by random factors such as particles
  - Systematic defects
    - Caused by deterministic factors such masks



- Classified by process
  - Oxidation (*front end process*)
  - Metallization (*back end process*)
  - Wire Bonding / Packaging
  - Overstress
  - Others: Reliability

Briefly Introduce CMOS Process Defects

Oxidation Related Defects

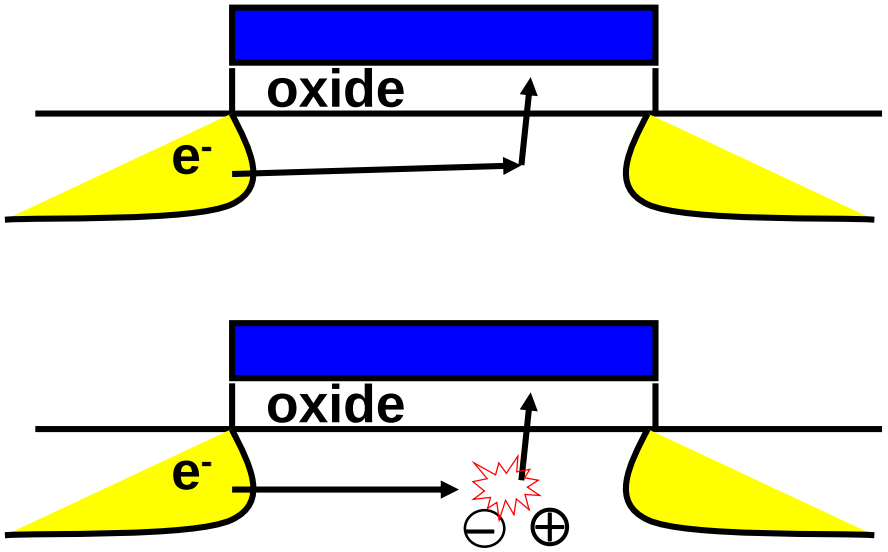
- **Thin oxide (gate oxide)**
  - ***Hot electron injection*** ➔ **V_t shift, Transconductance change**
  - ***Oxide breakdown*** ➔ **gate oxide shorts**
  - ***Ionic contamination*** ➔ **V_t shift**

- **Thick oxide (field oxide)**
  - **Ionic contamination**

Failure Mechanism ➔ Failure Mode

Hot Electron Injection aka Hot Carrier Injection

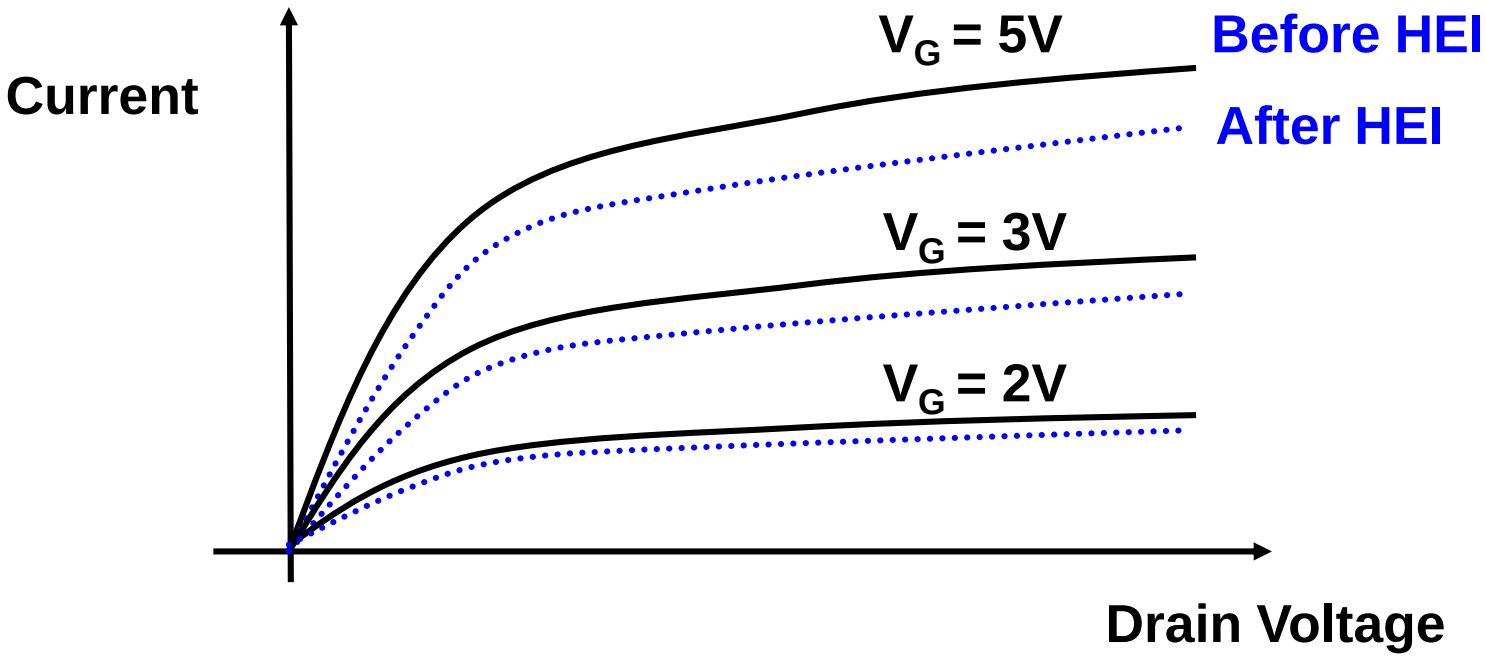
- Failure mechanism
  - Carriers (like electrons) gain high energy from source-drain potential drop
  - Some electrons gain such high energy (called *hot electrons*) that they are able to cross the energy barrier of Si-Oxide interface and trapped in oxide
- More evident in nMOS



Hot Electron Injection 2/2

- **Results (Failure modes) of HEI**
  - **V_t shift**
  - **Transconductance change**

- **Example**

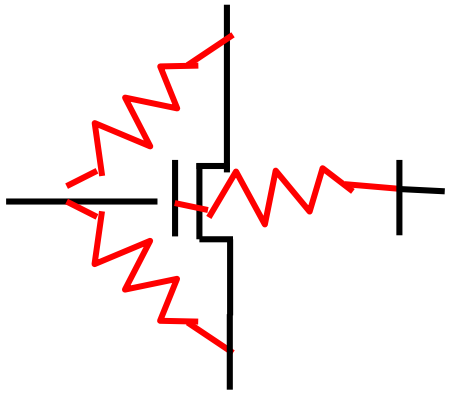


Oxide Breakdown

- What is *Oxide breakdown*?
  - Sudden increase in oxide conductance
  - High current pass through and Joul heating cause oxide damage
- Three frequent failure mechanisms
  1. *Pinholes* or thin spots in oxide
     - Point defects in thin oxide where atom missing from lattice site
  2. *Tunneling effect*
     - Electrons injected into oxide by tunneling and break bonds by collision
     - Can be serious problem in future ultra-thin oxide technology
  3. *Electrical overstress*
     - Wrong design or careless handling
- Results (Failure mode) of oxide breakdown
  - Gate oxide shorts

Gate Oxide Shorts

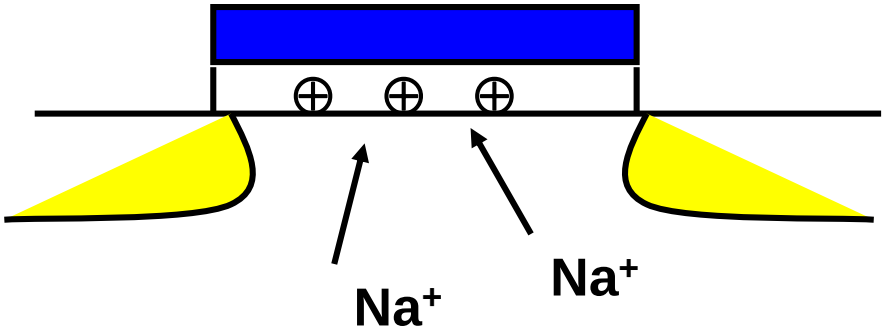
- What are *gate oxide shorts* ?
  - Low impedance path between gate and Si surface
- One of the most frequent failure modes in CMOS technology
- Gate oxide shorts can exist between
  - Gate-drain
  - Gate-source
  - Gate-substrate



- Models
  - if nMOS
    - Simply resistor, 4.7Kohm [Hawkins 85]
    - The number is process dependent
  - If pMOS
    - Complex model with diodes, resistors [Syrzycki 89]

Ionic Contamination

- Failure Mechanism
  - Presence of mobile ions (e.g. Na^+) near surface of oxide can invert the intended doping concentration near surface
  - Can accumulate over time
- Failure modes
  - V_t Shift
  - Leakage current increased
- One major problems in early CMOS process (1930)
  - Took ~10 years to figure out the culprit was ion



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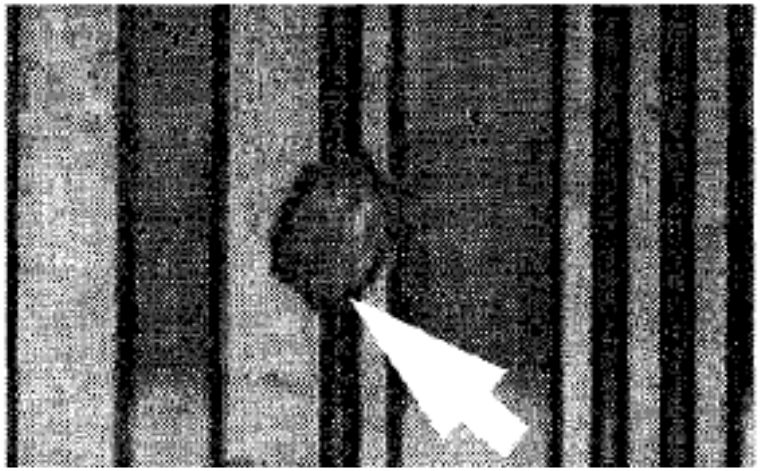


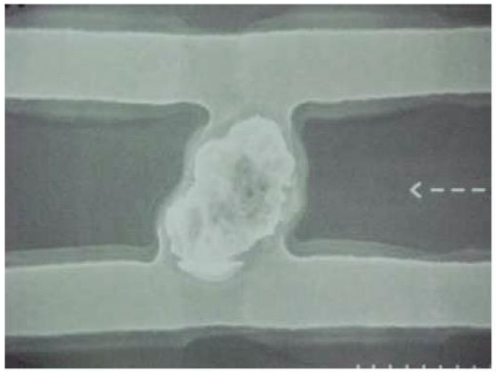
Metallization Related Defects

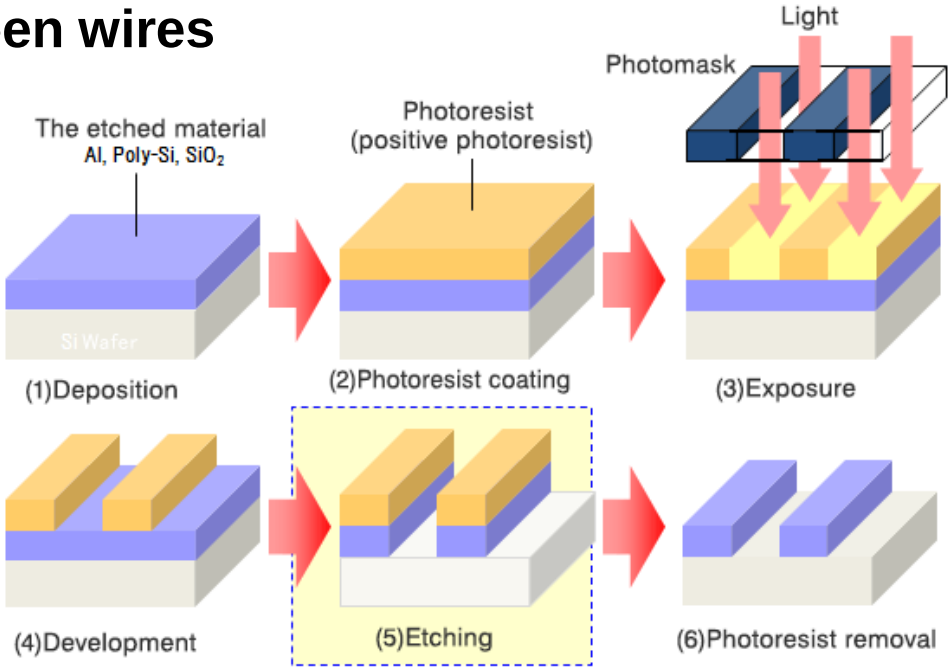
- Poor lithography patterning ➔ open or short
  - mask problem, misalignment, poor step coverage etc
- Bad *Chemical Mechanical Polishing (CMP)* ➔ open or short
- Particle ➔ open or short
- Bad Via or contact ➔ open or increased resistance
- Melting ➔ open
  - Excess current density melt wires
  - can be caused by design error, scratch, mask problem
- Alloy ➔ open or short
  - Si dissolved into Al or Al dissolved into Si
- Scratch ➔ open
  - Caused by careless handling

Failure Mechanism ➔ Failure Mode

Particles Can Cause Shorts

- Aluminum process steps
  - 1. Al deposition
  - 2. Photoresist deposition
  - 3. Expose
  - 4. Etch off photoresist between wires
    - Particles fall on die
  - 5. Etch off Al between wires
    - Particles cause shorts

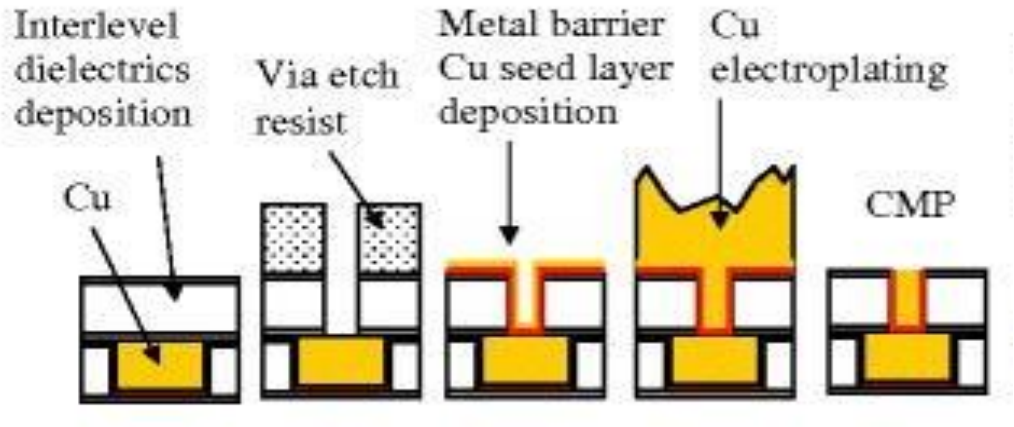




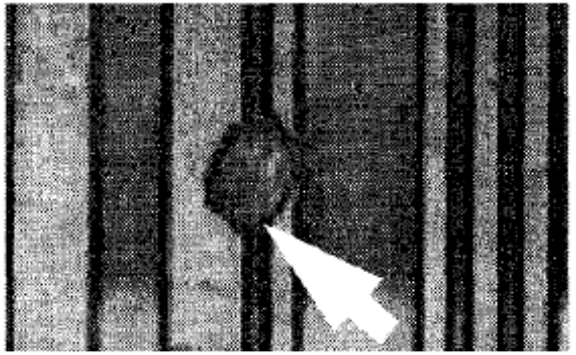
"What is an Etch System"
https://www.hitachi-hightech.com/

Particles Also Cause Opens

- Copper Process (*Damascene process*)
  - 1. Oxide deposition
  - 2. Photoresist deposition
  - Expose
  - Etching
  - 3. Copper Seed layer
    - Particles fall on die
  - 4. Copper deposition
    - Particle cause opens
  - 5. Chemical Mechanical Polishing



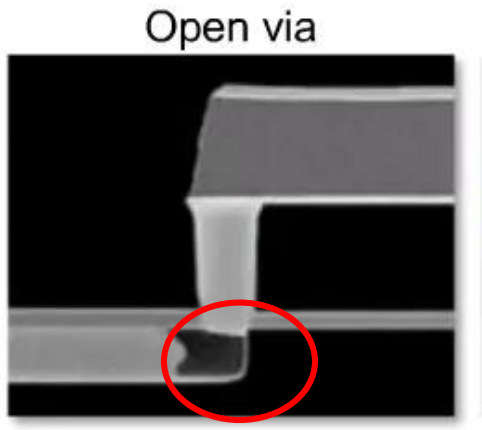
N. Kobayashi, "Damascene Concept and Process Steps," Advanced Nanoscale ULSI Interconnects, 2009



Defects are Process Dependent

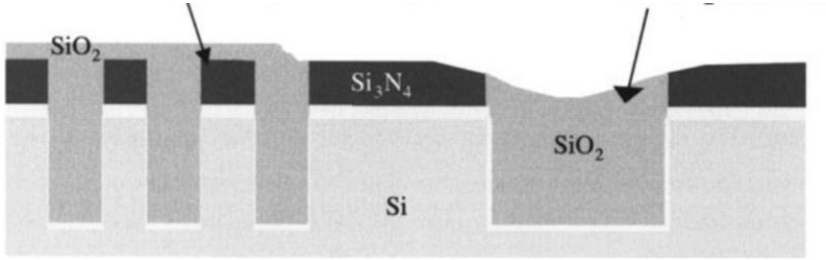
Metallization Defects

- Vias / contact related defects
  - Failure Mechanism
    - Incomplete etching
    - Mask problems
    - Particles
  - Failure modes
    - Open
    - Increased resistance



D. Payne (Synopsys), "Catching IC Manufacturing Defects With Slack-Based Transition Delay Testing", SemiWikli.com, 2014

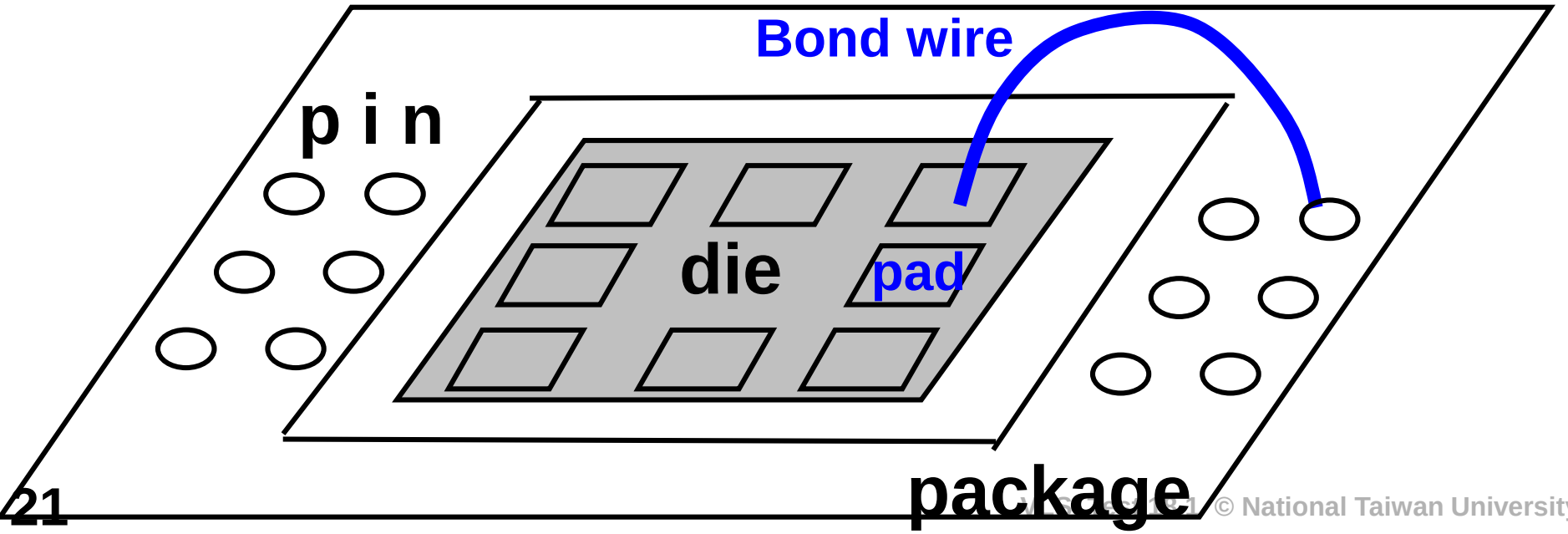
- CMP related defects
  - Failure mechanism
    - Insufficient polish
  - Failure mode
    - shorts



K.M. Robinson, K. DeVriendt, and D.R. Evans, "Integration Issues of CMP," Chemical-Mechanical Planarization of Semiconductor Materials, Springer 2004

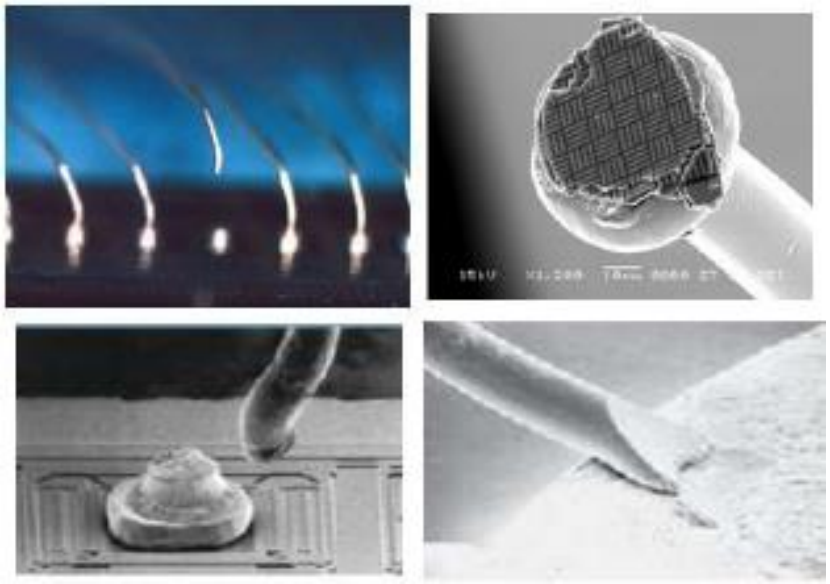
Wire Bonding Related Defects

- Poor pad ➔ open or short
  - Al interact with Si at high temperature, penetrating each other
- Purple plague ➔ open
  - Bonding Au wire to Al pad in the presence of Si forms $AuAl_2$ compound, a purple intermetallic compound which is brittle
- Poor pad-wire contact ➔ open or short
  - Caused by insufficient or excessive pressure/temperature



Package Related Defects

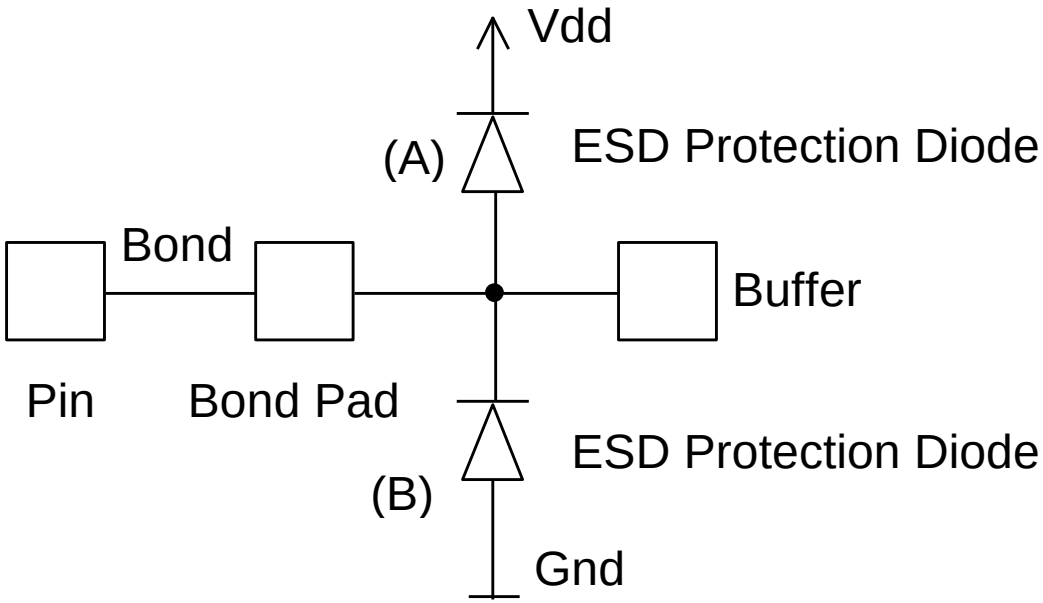
- Moisture penetration
- Mechanical problem
- Poor die-attach
  - Die cannot sit in the package substrate properly
  - Caused by :Solder quantity, temperature, pressure

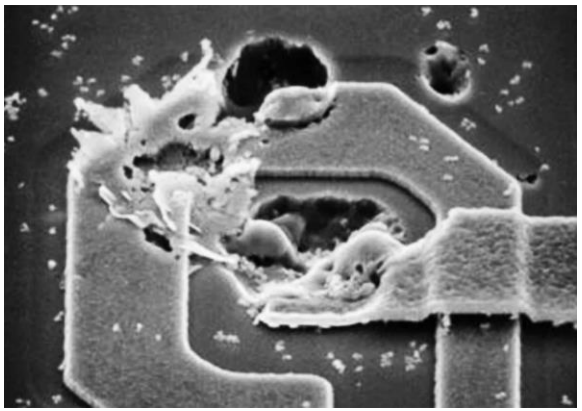


E. Spaan, E. Ooms, “Wire bonding the future: a combined experimental and numerical approach to improve the Cu-wire bonding quality,” EuroSimE, 2010

Overstress

- **Electrical overstress**
  - **Due to design mistake**
- ***Electrostatic discharge (ESD)***
  - **Due to careless handling**
  - **Can be minimized by ESD protection circuitry**





Edvard, "Never underestimate electrostatic discharge (ESD) while working with data networking equipment, " EE Portal 2017

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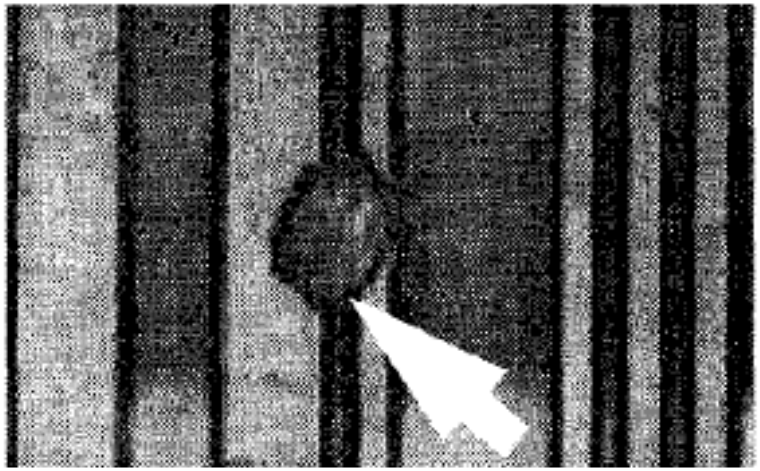
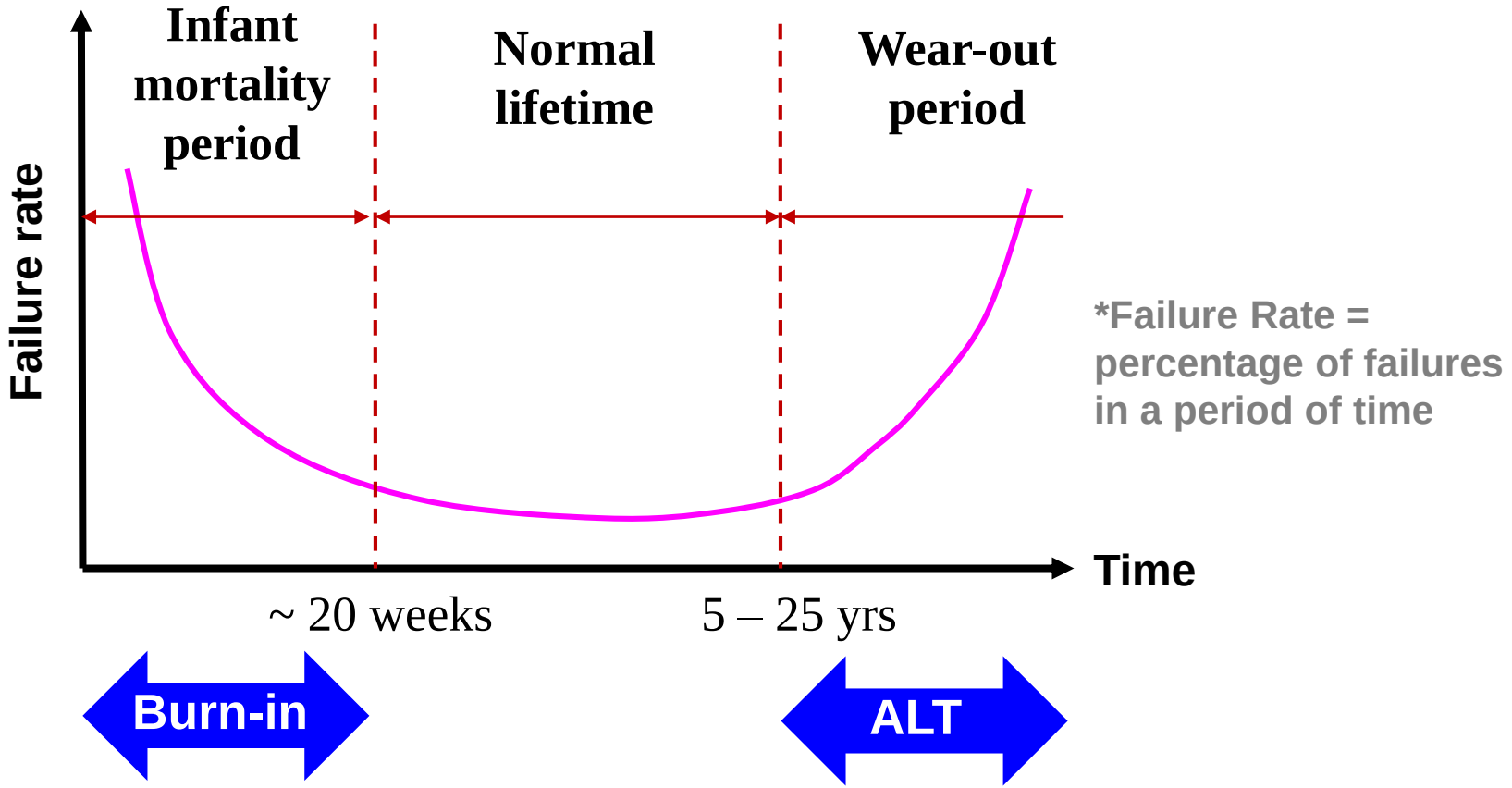


Review: Reliability Curve (CH1)

- IC's *failure rate** resembles a bathtub
  - *Infant mortality*: fail early in life, due to *reliability defects*



*Failure Rate = percentage of failures in a period of time

Reliability Defects

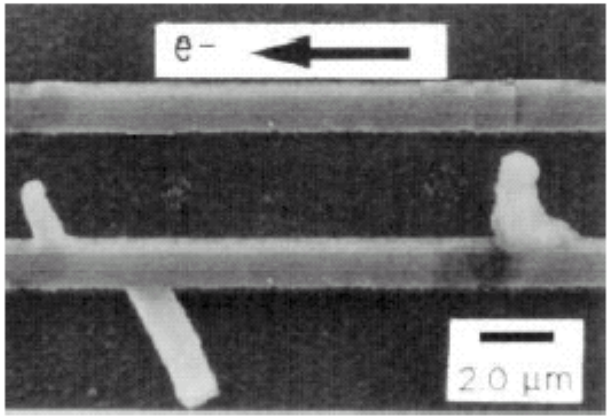
- **Devices**
  - ***Negative bias temperature instability*** **(NBTI) → V_t shift in PMOS**
  - ***Time-dependent gate oxide breakdown*** **(TDDB) → V_t shift, increase leakage current**
  - **Hot electron injection → V_t shift**

- **Wiring**
  - ***Eletronmigration*** **➔ open, short**
  - **Stress-induced voiding ➔ open**
  - **Corrosion ➔ open**

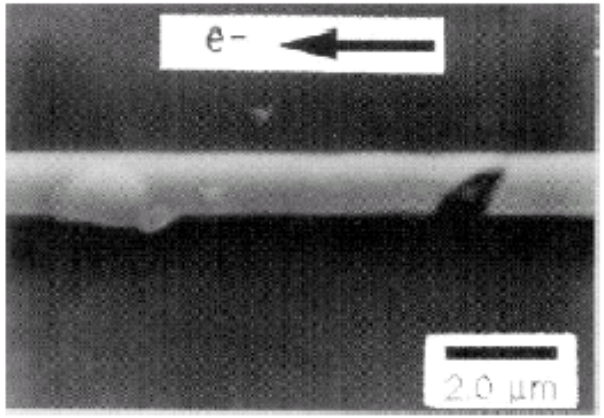
Electromigration

- Atom moved by electron wind when current density J too high
  - Aluminum J > 10^5 A/cm^2 and T > 100ºC
  - Copper is more resistant to electromigration

- Two possible failure modes:
  - Voids ➔ open
  - hillocks ➔short

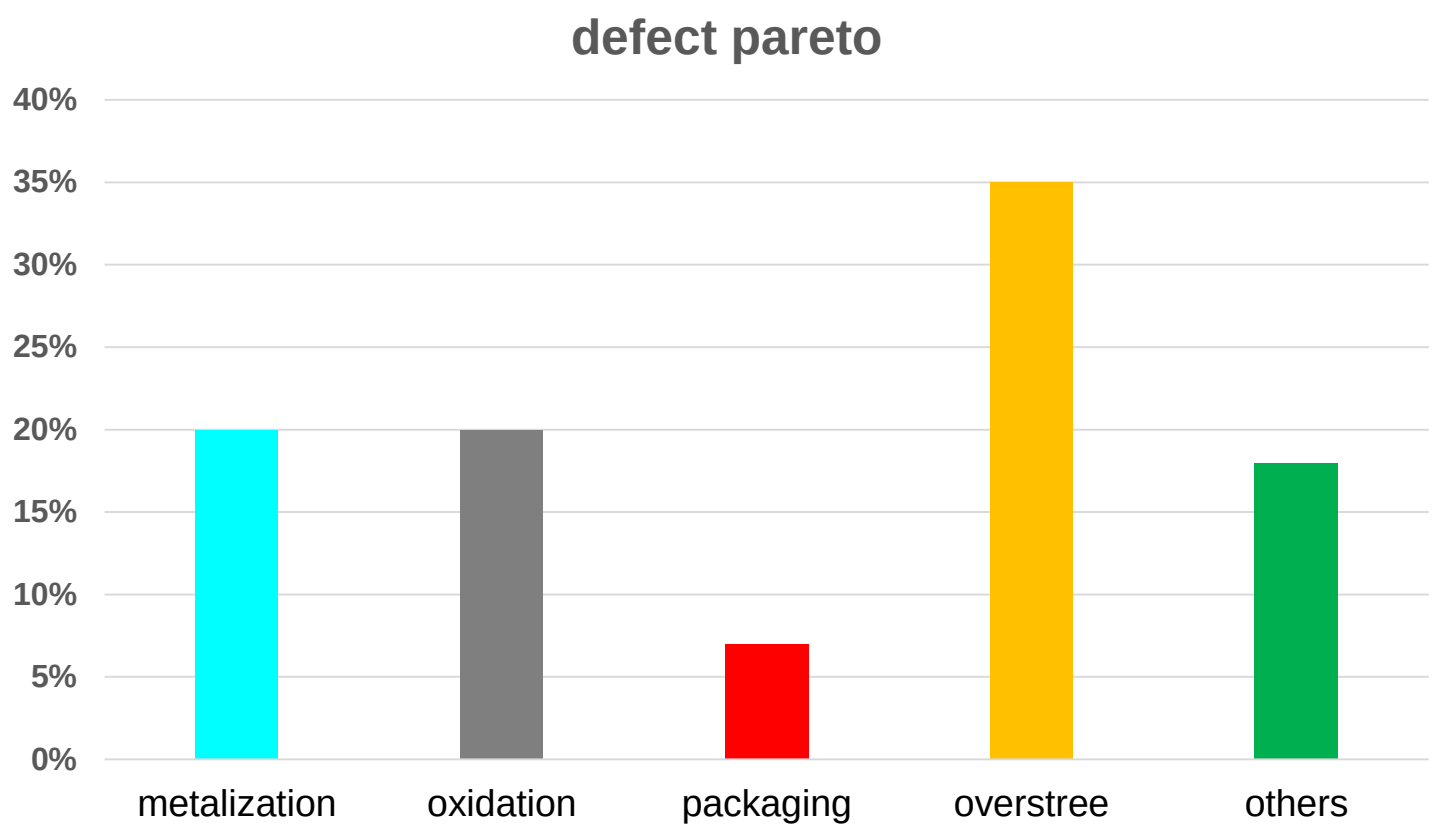


hillocks ➔ Short



Voids ➔ Open

Example Defect Pareto



Defects are Process Dependent

Quiz

Q: Which of following is NOT correct?

A: particle can cause both opens and shorts

B: reliability defects worsen with time

C: SSF can model all kinds of open defects

Conclusion

- 100% FC ≠ 0 DPM
- Failure mechanism: cause of defect
  - Physical or chemical process that cause defects
- Failure mode: behavior of defect
  - Causes or possible ways a device can fail
- Defect Categories (process dependent)
  - Oxidation (*front end process*)
  - Metallization (*backend process*)
  - Wire Bonding / Packaging
  - Overstress
  - Others: Reliability

Impossible To Model All Defects by a Single Fault Model

Corrosion

- Residue of solvents used during process or traces of chemicals in packaging
  - Corrosion in Al in presence of H2O
- Plastic package particularly poor
  - Moisture can penetrate

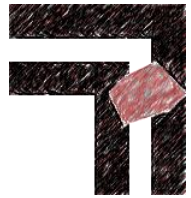
Test Escape vs. Yield Loss

- True pass and true reject are correct decision
- *Test escapes* = defective chips that pass test
  - also known as (aka.) *under-testing*
- *Yield loss* = good chips that fail the tests
  - aka. *overkill*, *over-testing*
- Goal of DBT: reduce both test escape and yield loss
  - Side effects of DBT
  - Sometimes inevitably increases yield loss
  - Trade off between yield loss and test quality

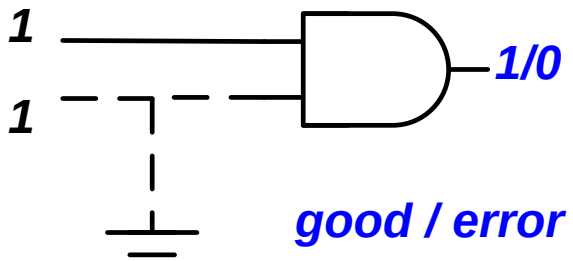
	Good IC	Defective IC
Pass tests	True PASS	Test Escapes (less is better)
Fail tests	Yield Loss (less is better)	True Reject

Definitions

- *Defect*
  - Unintended physical difference between hardware implementation and its intended design
  - Example: unwanted wire (short to ground)



- *Fault*
  - Representation of defects at abstracted logic level
  - Example: b stuck at zero fault
- *Error*
  - Wrong output signal value
  - Example: output = 0, when a=b=1
- *Failure*
  - Deviation from expected behavior
  - Example: computer crash



Defect → Fault → Error → Failure

Introduction

- What is *Defect Based Testing* (DBT)
  - Testing without specific fault model involved

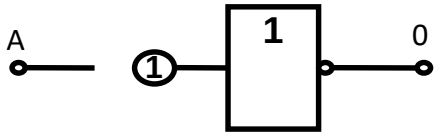
- Why Defect Based Testing?
  - reduce DPM
    - 100% fault coverage is not good enough
    - Defects do not always behave as faults

- Experimental results [Stanford CRC]
  - Total 5.5K chips tested by many kinds of test sets
    - 116 defective found
    - 2 to 6 chips escaped 100% SSF test sets
  - Example : High impedance bridging defect
    - Cause abnormal static current
    - May not detectable by Boolean testing

Example

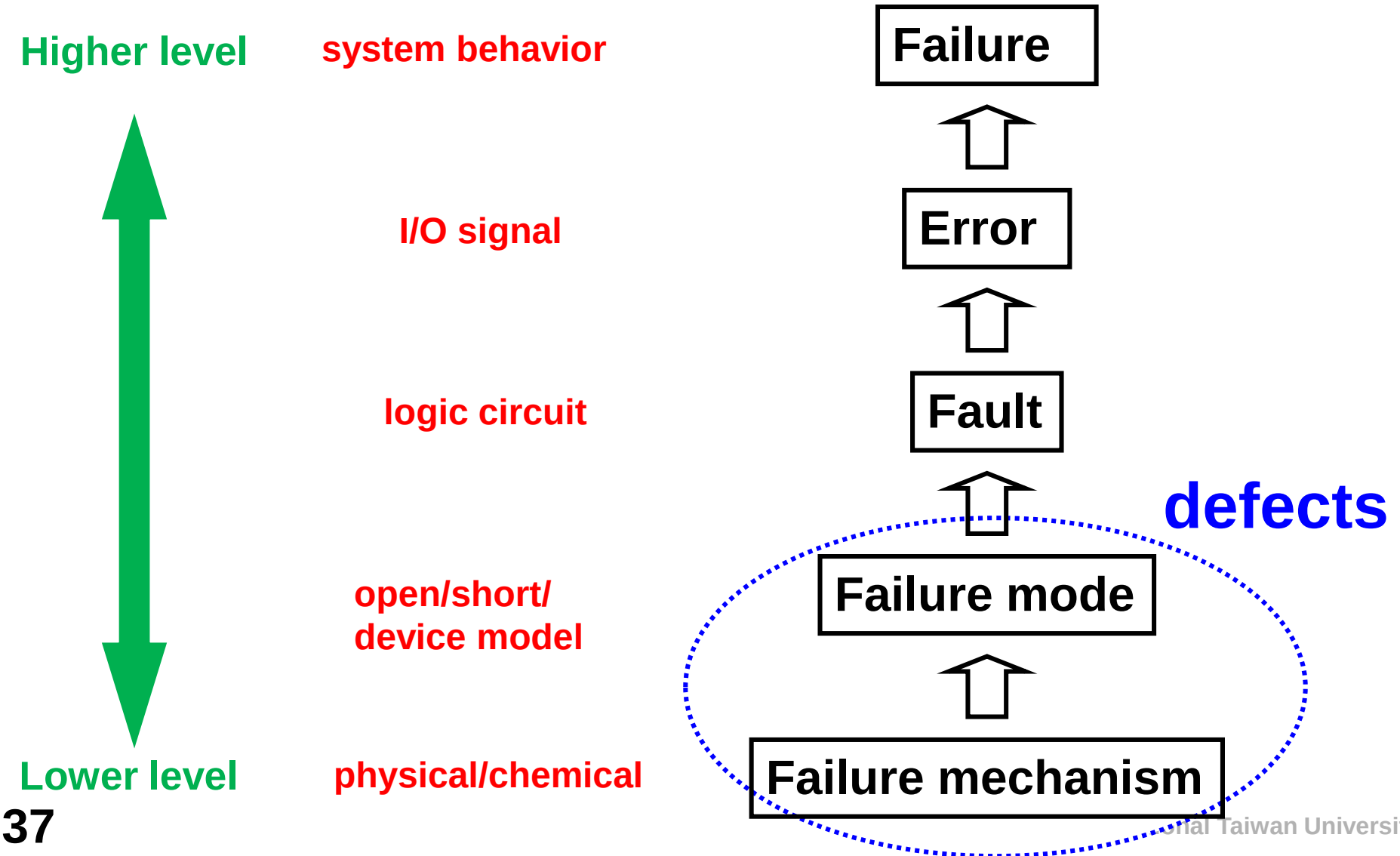
Failure Mechanism: Particle on Mask

Failure Mode: Open Metal Line



Fault Model: Stuck-at-1 Fault

Fail. Mech → Fail. Mode → Fault



Failure Mode Analysis

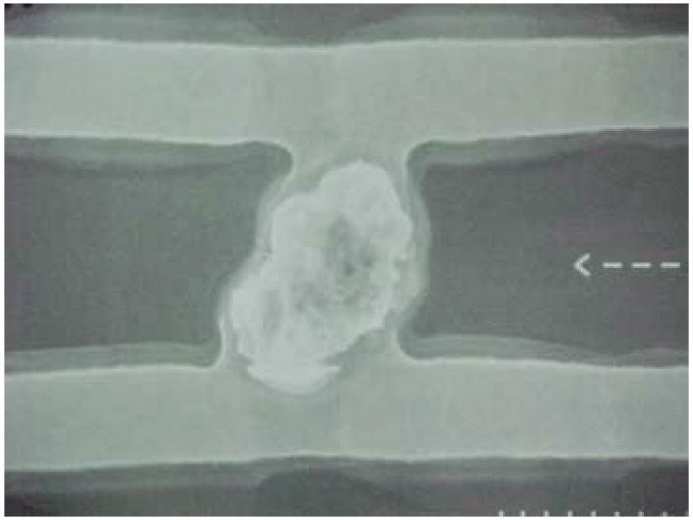
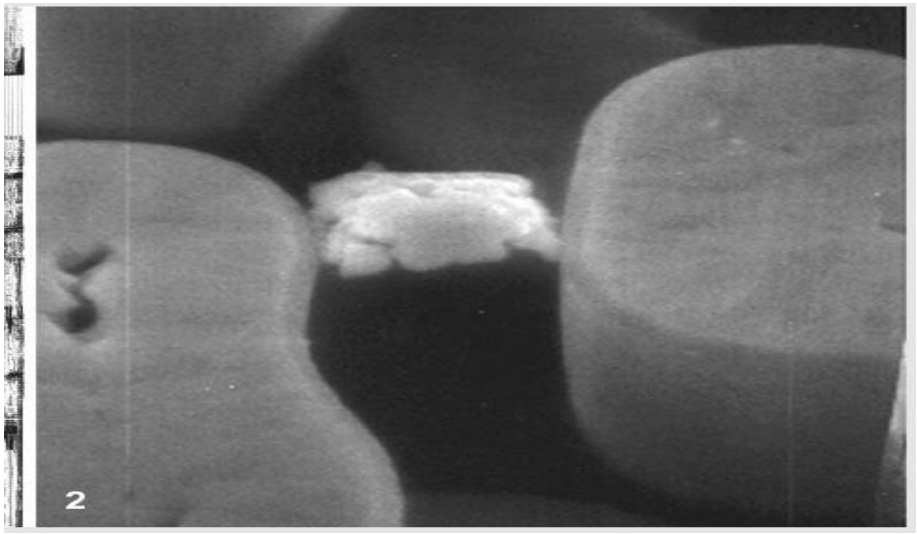
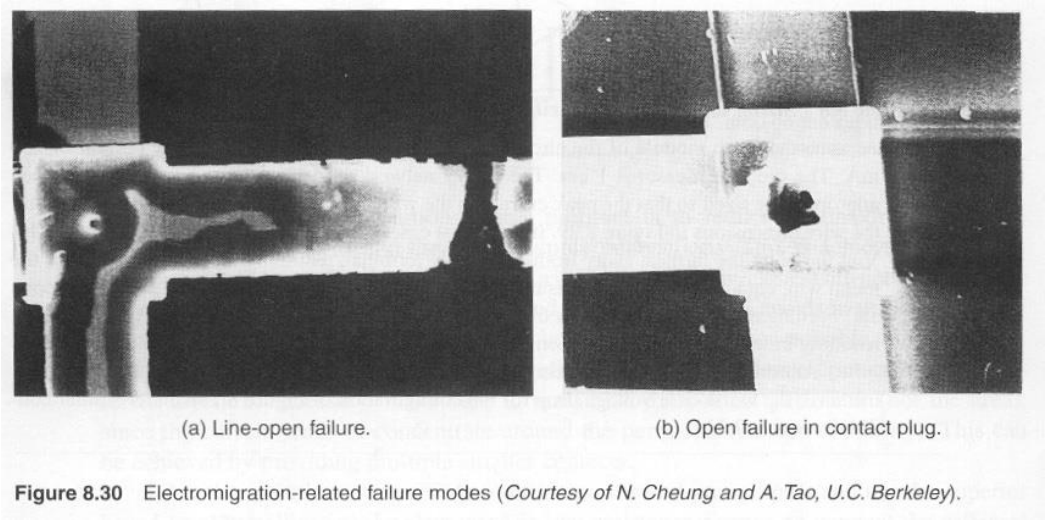


Photo 2-4 Dust-induced Wiring Short

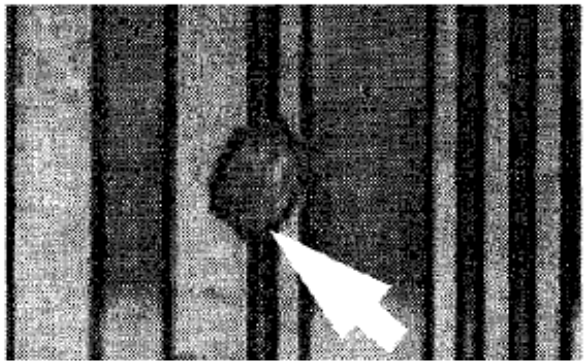


[Vallet IBM 1997]

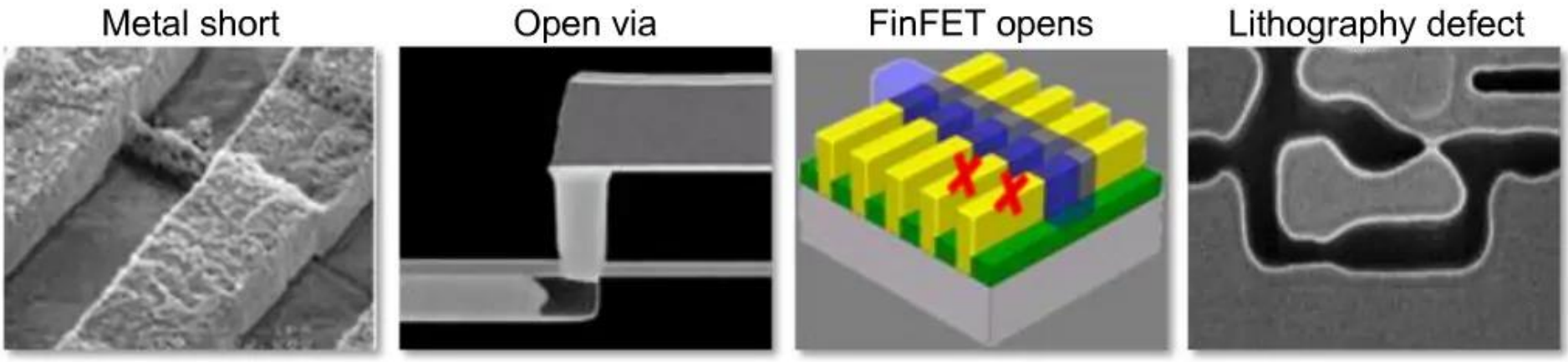


(a) Line-open failure. (b) Open failure in contact plug.

Figure 8.30 Electromigration-related failure modes (*Courtesy of N. Cheung and A. Tao, U.C. Berkeley*).



[Nigh IBM 1998]



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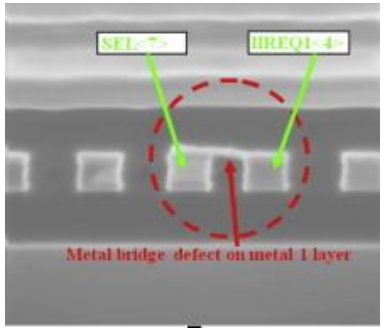

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