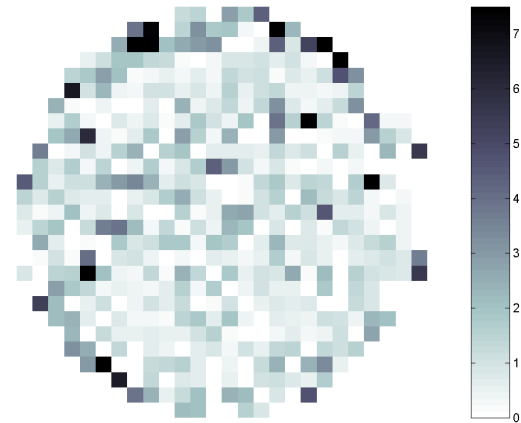


# Advanced Topics: $I_{DDQ}$

- Introduction
- Defect-based Testing
  - ◆ VLV Testing (1982)
  - ◆  $I_{DDQ}$  Testing (1981)
    - \* Introduction
    - \* Fault models and test patterns
    - \*  $I_{DDQ}$  Measurement
    - \* Experimental Results
    - \* Issues & Solutions
- Advanced ATPG
- Conclusion



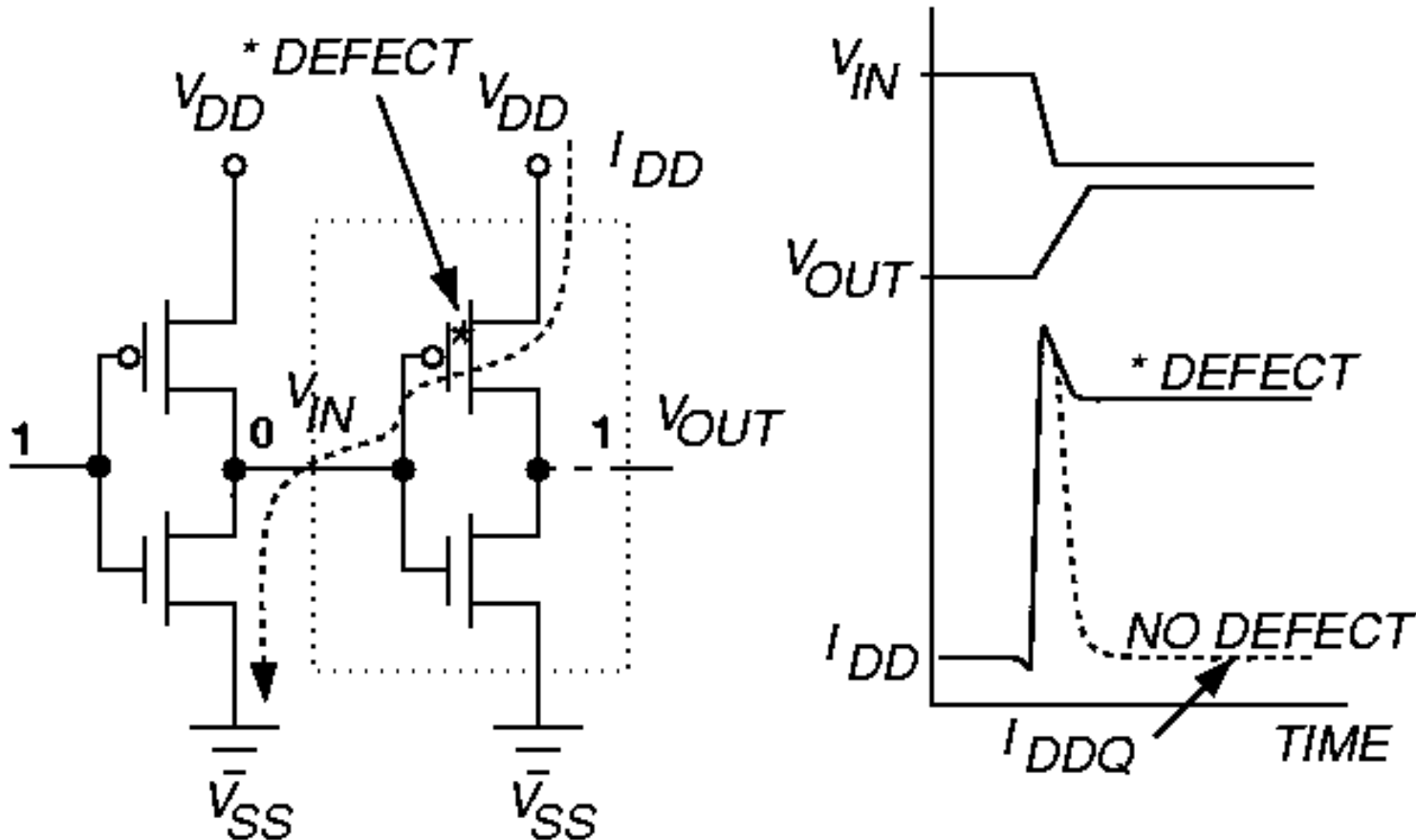
# $I_{DDQ}$ Testing

- What is  $I_{DDQ}$  Testing?
  - ♦ Measure static power supply current, with test patterns applied
  - ♦  $I_{DD}$  = power supply current from  $V_{DD}$
  - ♦ Q = quiescent
- Widely used but first officially presented by [Levi 81]
  - ♦ Still commonly used DBT in CMOS technology so far
- Motivations to use  $I_{DDQ}$ 
  - ♦ Improve DPM
    - \* Targeted 3 DPM in early 1990's
  - ♦ Improve reliability
    - \* Chips pass Boolean test but may fail early in life

**$I_{DDQ}$  is Probably the Most Popular DBT**

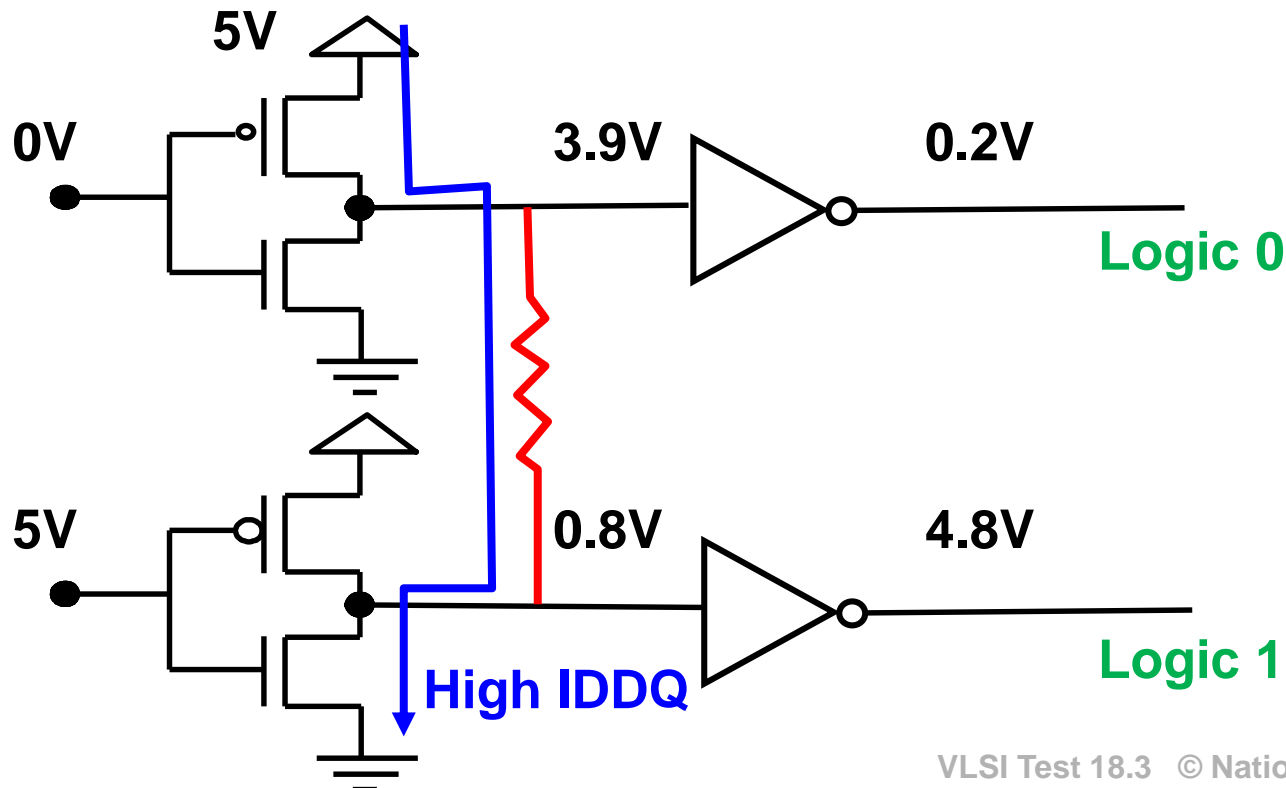
# Idea of $I_{DDQ}$ Testing

- Good CMOS circuit, very low  $I_{DDQ}$
- Defective CMOS circuit, high  $I_{DDQ}$
- Example:
  - ♦ gate oxide short provides a conduction path from  $V_{DD}$  to Gnd



# Why $I_{DDQ}$ Better Than Boolean Testing?

- $I_{DDQ}$  sometimes detects defects missed by Boolean testing
- Example: High impedance bridging defect
  - ♦ may not detectable by SSF test
  - ♦ Could be detected by  $I_{DDQ}$  test
- FFT: Why bother since it passes Boolean test?

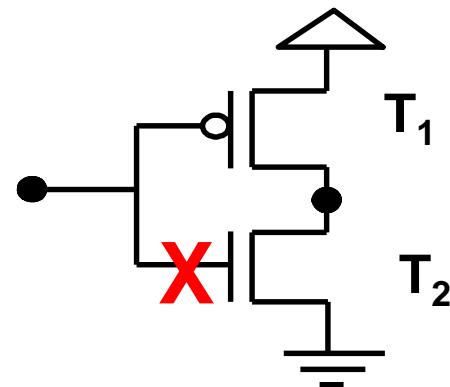
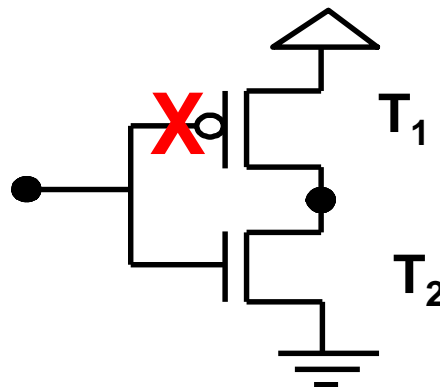
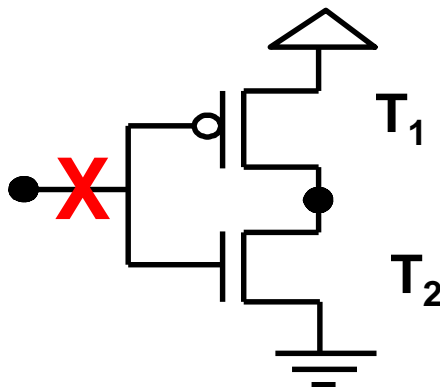


# Defects Could be Detected by $I_{DDQ}$

- **Bridging/shorts**
  - ◆ **Signal to signal bridging**
  - ◆ **Signal to power short**
  - ◆ **Ground to power short**
  - ◆ **Gate oxide shorts**
- **$V_t$  shift**
  - ◆ **Cause increased leakage  $I_{DDQ}$**
- **...Many more**

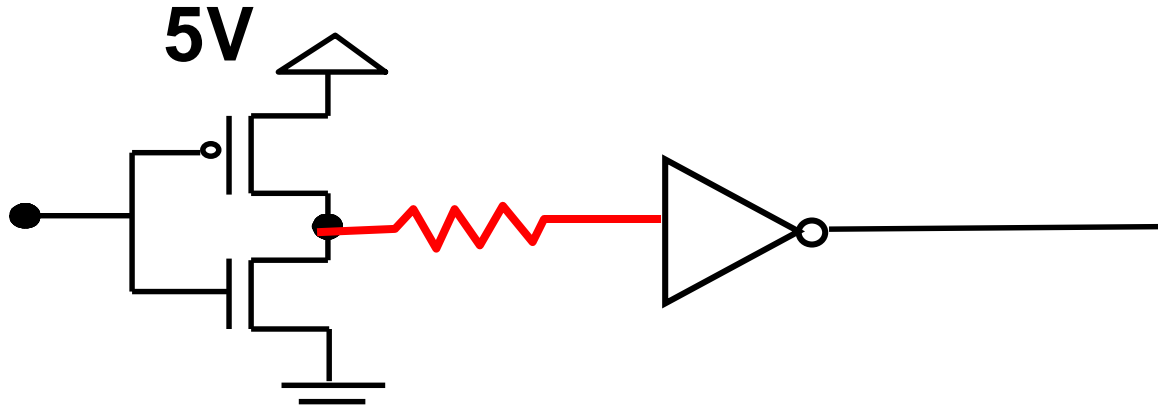
# Opens May (Not) Detected by $I_{DDQ}$

- Open defects:  $I_{DDQ}$  depends on **floating gate voltage**
  - ♦ Floating single transistor gate
  - ♦ Floating nMOS+pMOS transistor pair
- Experimental results [Stanford 00]
  - \* Total 5.5 K chips tested, 116 defective chips
  - \* 7 chips diagnosed to have opens
  - \* 4 high  $I_{DDQ}$ , 3 low  $I_{DDQ}$  [Li 00]

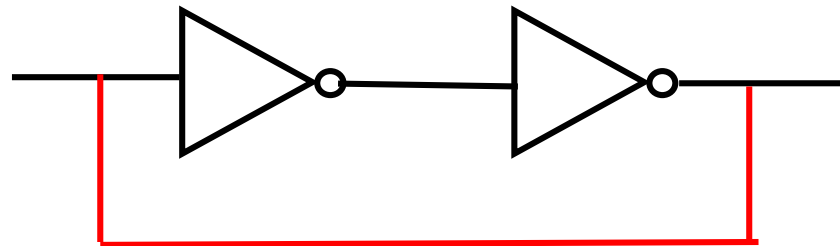


# Defects Not Detected by $I_{DDQ}$

- Resistive open defects
  - ♦ Transient signal **delay** won't cause high  $I_{DDQ}$



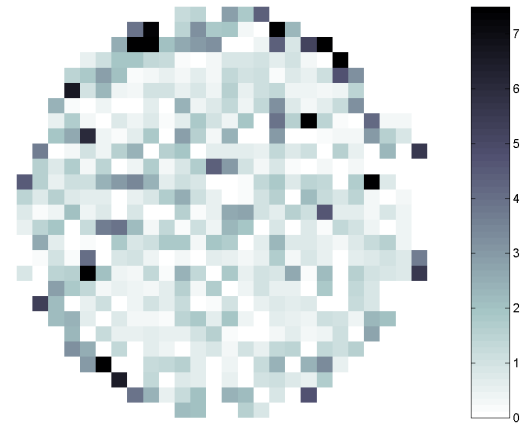
- Feedback bridging fault
  - ♦ Even parity



**$I_{DDQ}$  Cannot Detect ALL Defects**

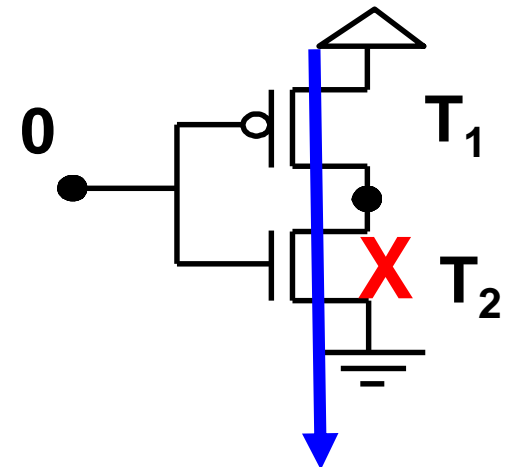
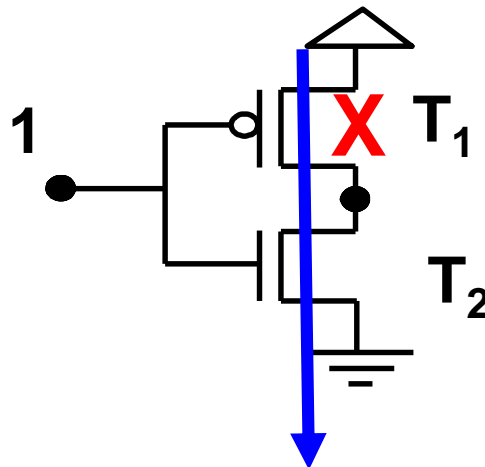
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# Fault Models for $I_{DDQ}$

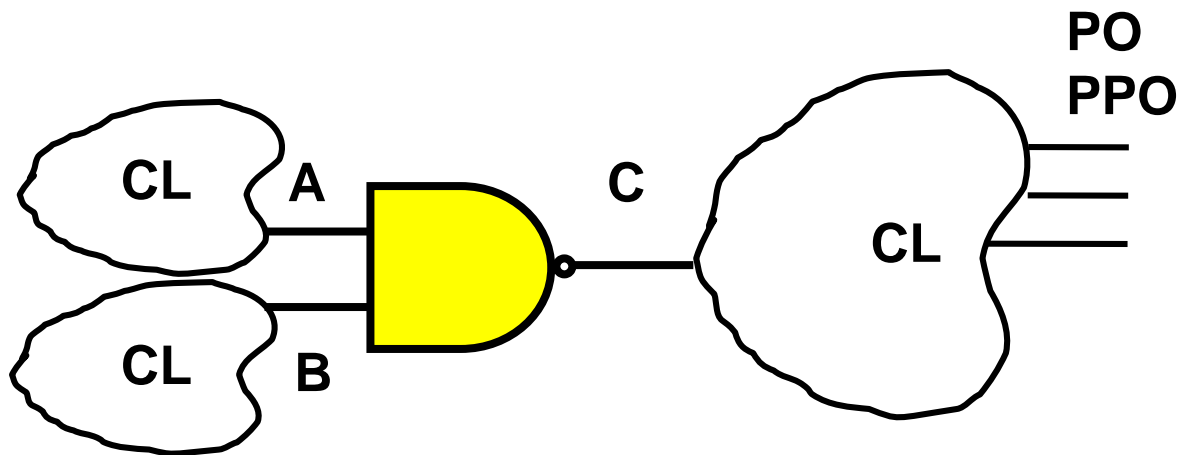
- Test pattern generation requires fault models
  - ♦ However,  $I_{DDQ}$  detects different types of defects
  - ♦ **No universal fault model** good for all defects
- Popular fault models for  $I_{DDQ}$ 
  - ♦ **Transistor stuck-on faults**
  - ♦ Pseudo stuck-at faults
  - ♦ Bridging faults
  - ♦ Leakage faults
  - ♦ ...



# Test Patterns for $I_{DDQ}$

- Test patterns can be either
  - ♦ **generated** by ATPG or
  - ♦ **selected** from existing patterns
- Test length must be **short** because  $I_{DDQ}$  testing is **slow**
- Commercial ATPG tools can support these test sets
  - ♦ *Toggle test set*
  - ♦ *Pseudo Stuck-at (PSA) test set*
- Example: 100% **toggle test set** for NAND gate

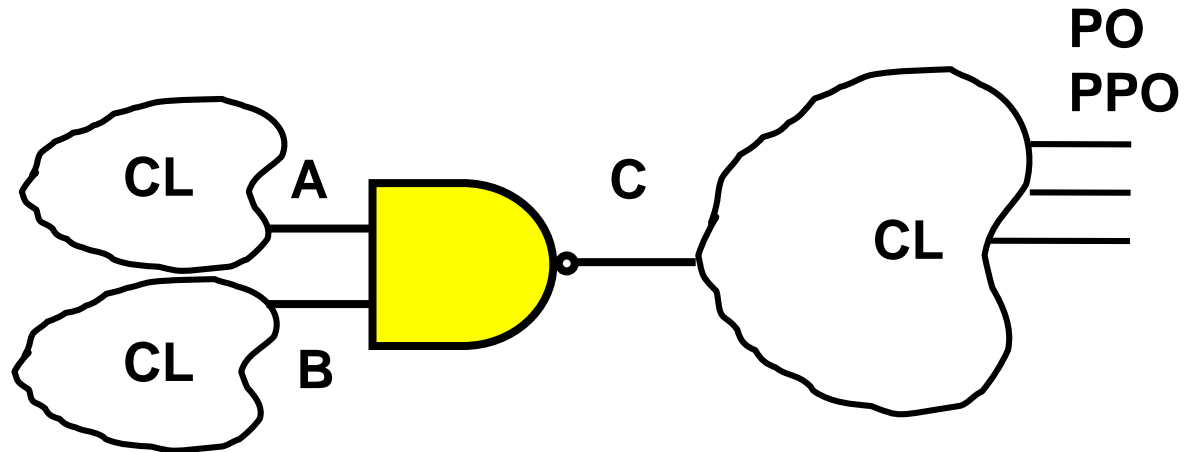
AB	C
00	1
11	0



# Pseudo Stuck-at Test Set

- Definition
  - ♦ Test set that **activate** SSF
  - ♦ but fault effects **need NOT propagate to PO or PPO**
- No propagation because  $I_{DDQ}$  can be measured by current
- Example: 100% pseudo stuck-at test set for NAND gate
  - ♦  $AB = 01, 10, 11$

AB	SSF faults
01	A/1;C/0
10	B/1;C/0
11	A/0; B/0; C/1



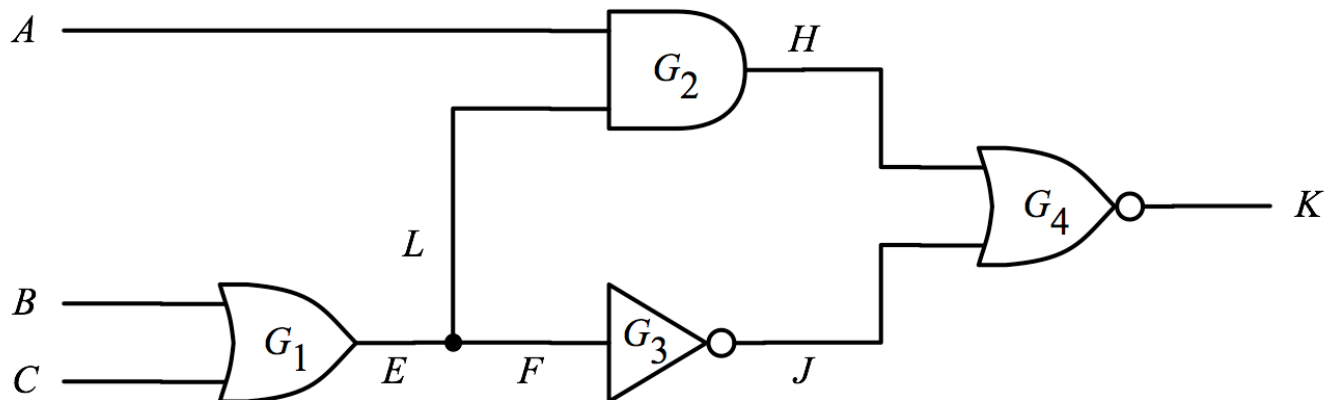
**$I_{DDQ}$  Test Length Must be Short**

# Quiz

Q: Please select three best toggle test patterns for  $I_{DDQ}$

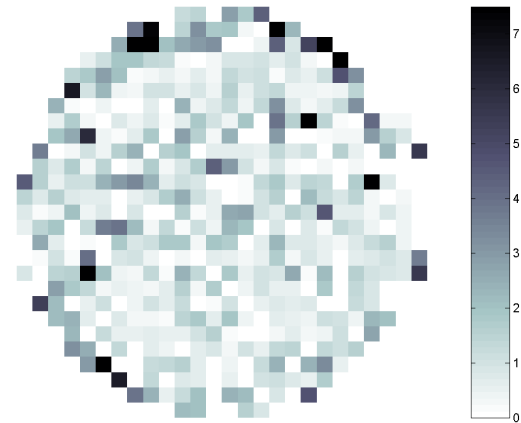
A:

	A	B	C	E	H	J	K
P1	1	1	0	1	1	0	0
P2	0	0	0	0	0	1	0
P3	1	0	1	1	1	0	0
P4	0	0	1	1	0	0	1



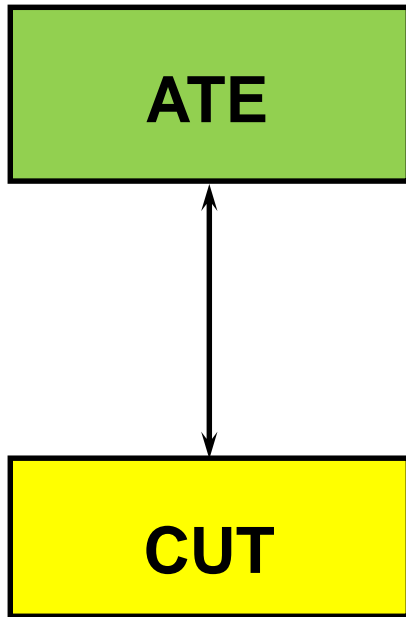
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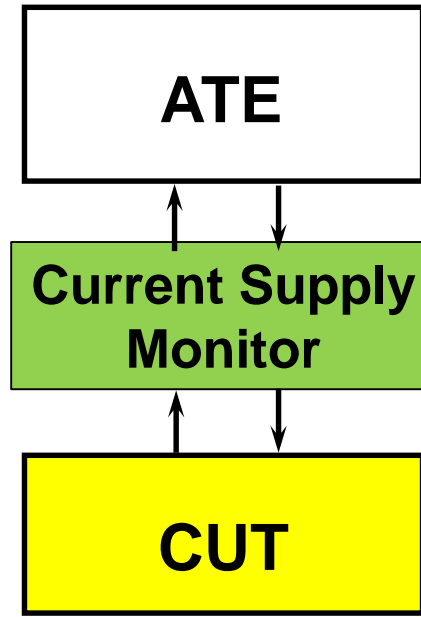


# $I_{DDQ}$ Measurement

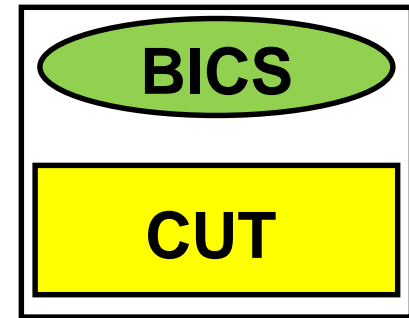
- Three ways to measure  $I_{DDQ}$



I. ATE



II. External device  
on Test Fixture



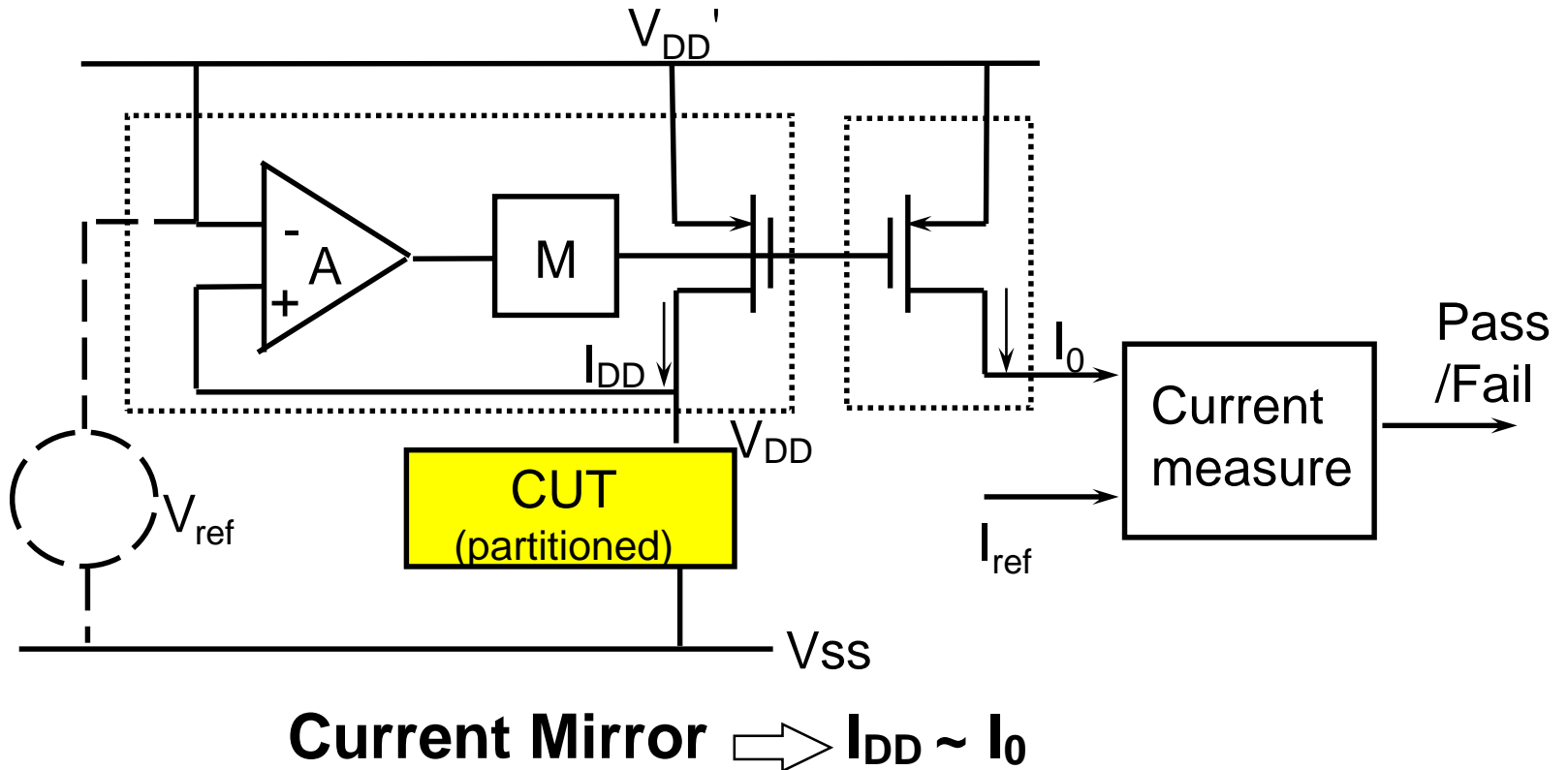
III. On-chip  
Built-In  
Current Sensor

# I. ATE

- Most ATE support  $I_{DDQ}$  measurements
  - ♦ **Precise measurement Unit** (PMU)
- Procedures
  - ♦ 1. apply test pattern
  - ♦ 2. **pause** at pre-selected patterns
  - ♦ 3. **wait about 1~10 ms** until CUT internal nodes stable
  - ♦ 4. measure  $I_{DDQ}$  current
    - \* **FAIL if larger than user defined threshold**
  - ♦ 5. continue applying patterns, loop back to step 2
- 😊 Advantages
  - ♦ No extra equipment needed. No design change
- 😞 Disadvantages
  - ♦ Long test time. Large background leakage current

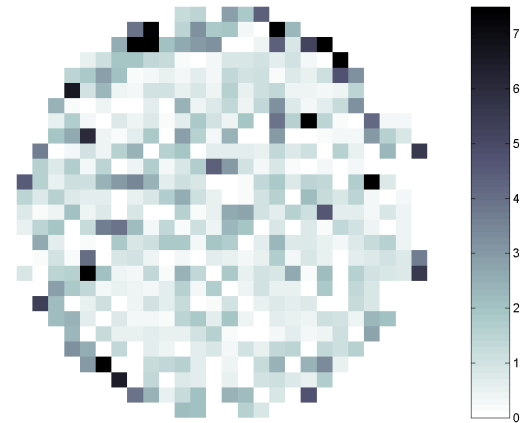
### III. BICS

- 😊 Self testable
- 😊 Easy to Partition CUT
- 😞 Performance degradation
- 😞 Area overhead



# Advanced Topics: $I_{DDQ}$

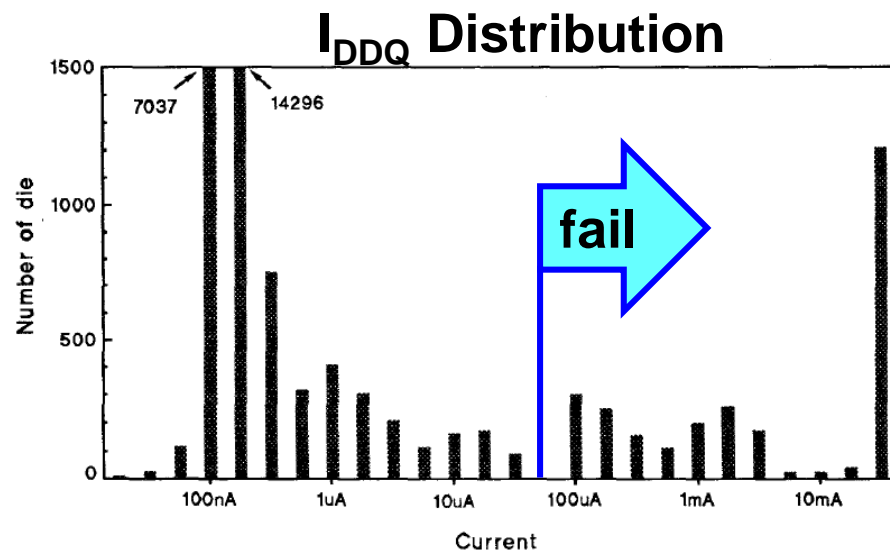
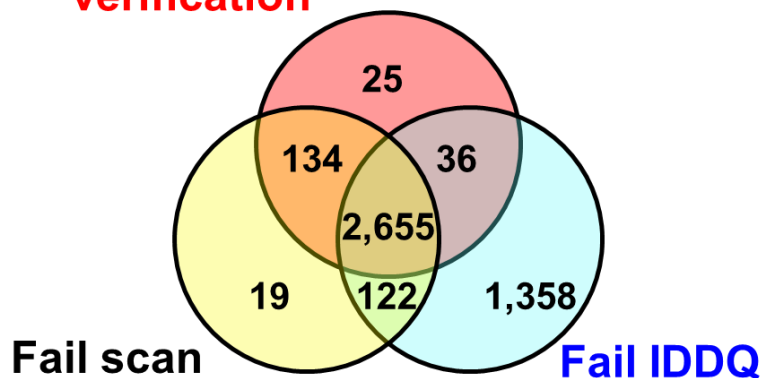
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# Experimental Results

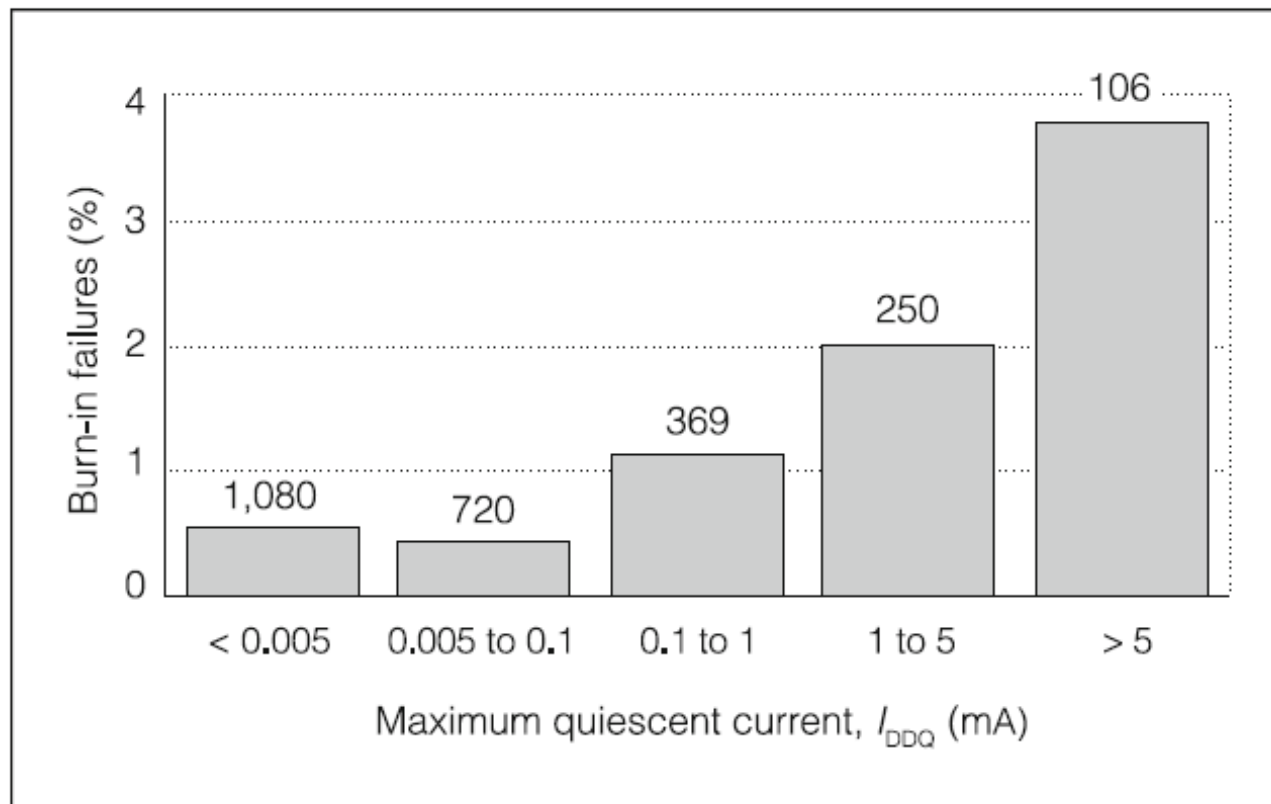
- HP experiment [Maxwell 92]
  - ♦ 26,415 dies, CMOS static logic, 8,577 gates
  - ♦  $I_{DDQ}$  pass/fail threshold =  $30\mu A$
  - ♦ 4,171 (15.8%) failed  $I_{DDQ}$ , 1,358 (5.1%) failed  $I_{DDQ}$  only

Fail functional  
verification



Some Defects Only Detected by  $I_{DDQ}$

# IBM Experiment [Nigh 00] [Mann 08]

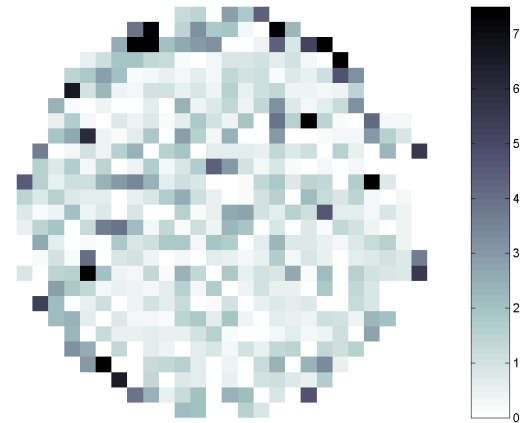


**Figure 2. Percentage of burn-in failure versus maximum  $I_{DDQ}$  for 2,525 devices. (Numbers in boxes refer to the sample size.)**

**Higher  $I_{DDQ}$ , More Unreliable**

# Advanced Topics: $I_{DDQ}$

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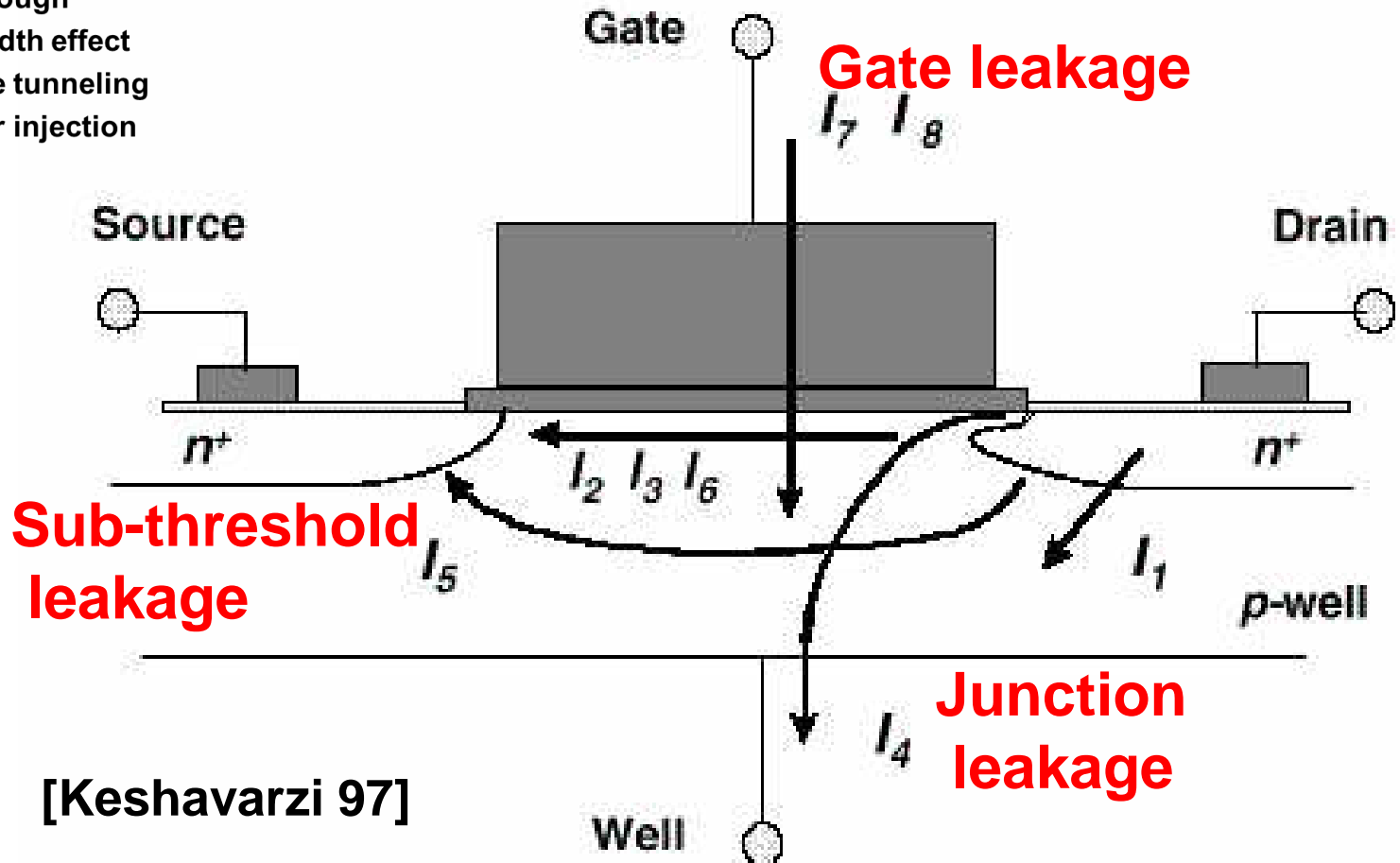


# Issues of $I_{DDQ}$ testing

- Long measurement time
  - ◆ Several **ms** per measurement on a ATE
- Trade off **yield loss** and **reliability**
  - ◆  $I_{DDQ}$  only failure chips
- Not applicable to all designs
  - ◆ Analog, mixed-signal, memory
- Losing effectiveness in advanced technology
  - ◆ Increasing background leakage current
  - ◆ Hard to set **single threshold**

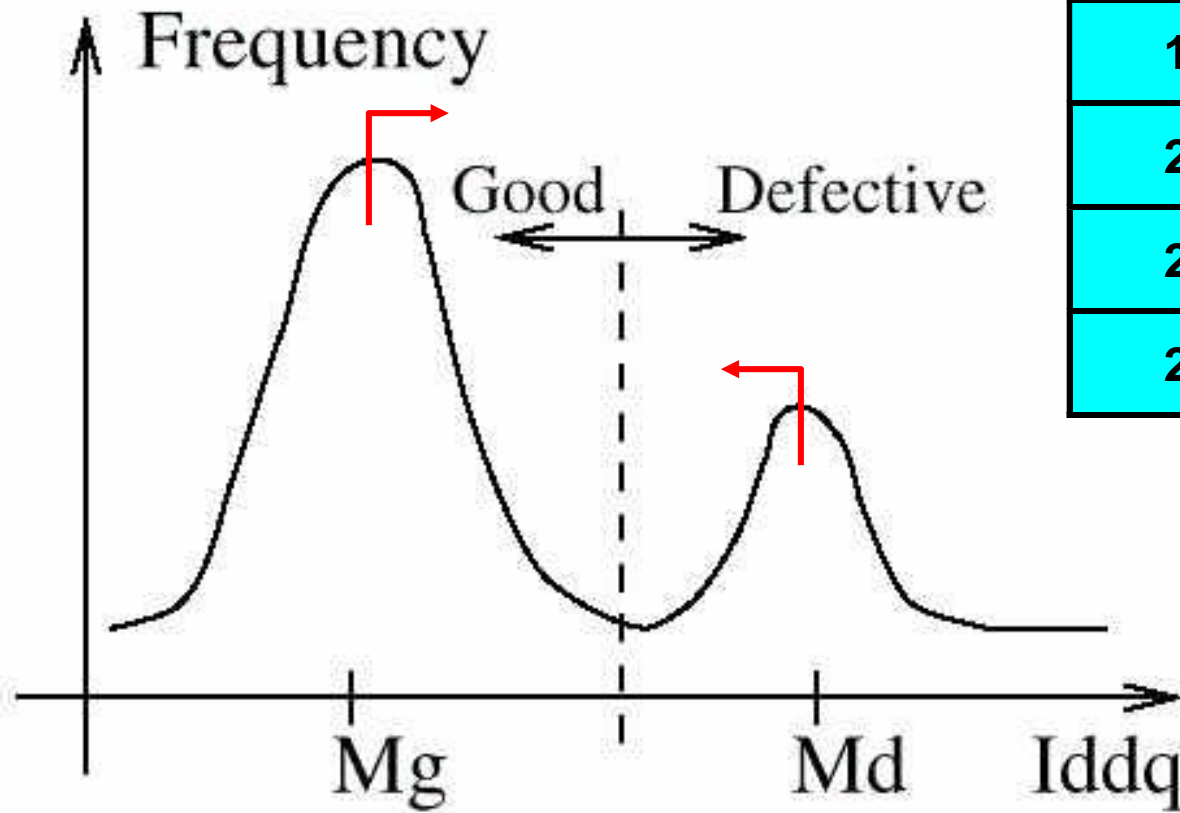
# Where Are Leakage Currents?

- $I_1$  - PN reverse bias
- $I_2$  - weak inversion
- $I_3$  - *drain induced barrier lowering* (DIBL)
- $I_4$  - *gate induced drain leakage* (GIDL)
- $I_5$  - punch through
- $I_6$  - narrow width effect
- $I_7$  - gate oxide tunneling
- $I_8$  - hot carrier injection



# Where is the Threshold?

- $M_g - M_d$  get closer [Williams 96]



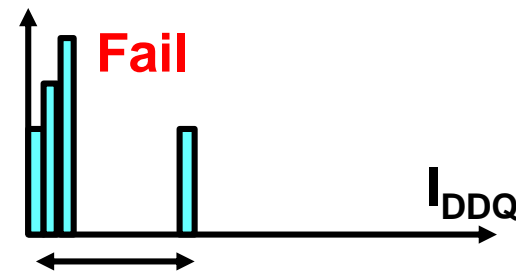
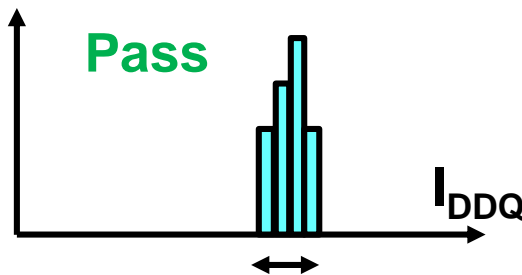
Year	Road map
1995	19.6%
1998	3.15%
2001	1.28%
2004	0.37%
2007	0.07%

# Possible Solutions for $I_{DDQ}$ (1/2)

- Reducing background Leakage
  - ◆ FinFET [Hu '98]
  - ◆ Substrate back-biasing (2500x - 4400x improvement)
  - ◆ Low temperature (350 x improvement)
  - ◆ Multiple  $V_t$ 
    - \* high  $V_t$  (low leakage) logic gates on non-critical paths
  - ◆ Circuit Partition
    - \* Built-In Current Sensor

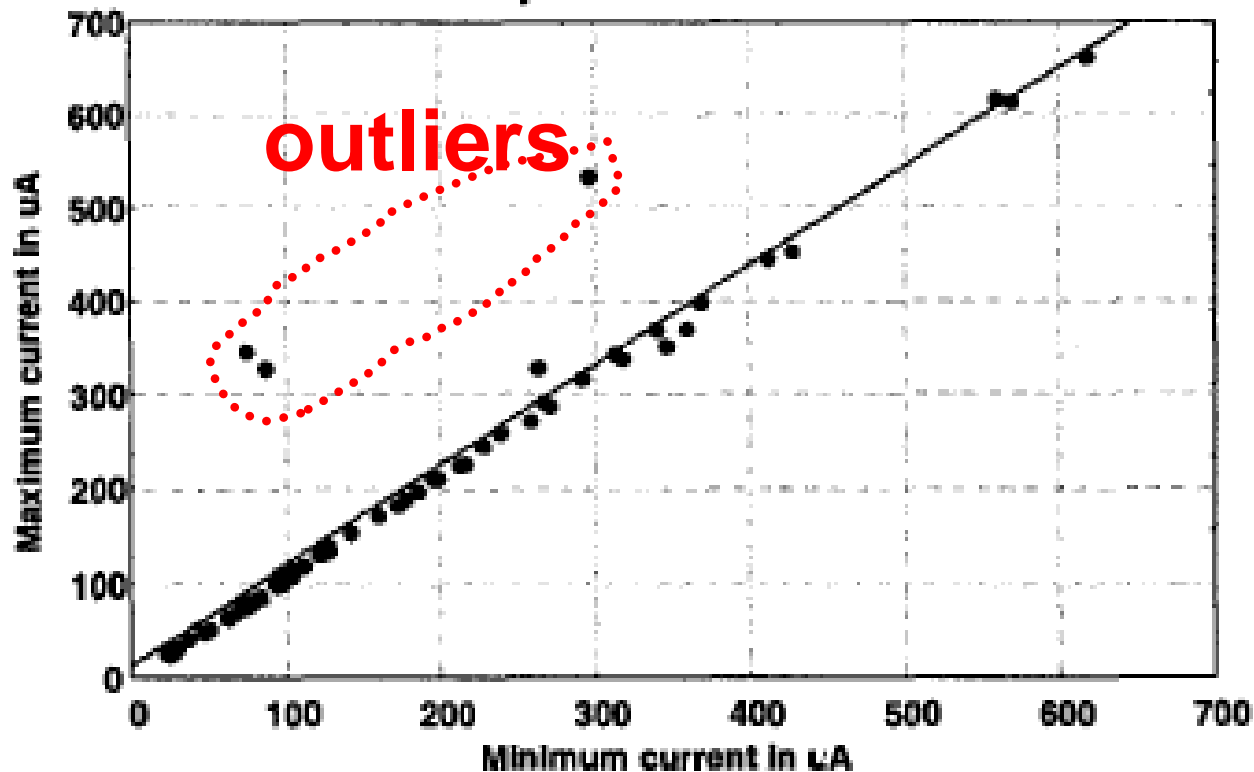
# Possible Solutions for $I_{DDQ}$ (2/2)

- $I_{DDQ}$  data processing. **Avoid single threshold**
  - ♦ Pass/fail decision made by processing collected  $I_{DDQ}$  data
  - ♦ No preset single threshold
- Example data processing techniques
  - ♦  $\Delta I_{DDQ}$  [Powell 00]
    - \*  $\Delta I_{DDQ} = I_{DDQ \max} - I_{DDQ \min}$
    - \* Fail this test if  $\Delta I_{DDQ}$  larger than limit
  - ♦ **Current Ratio** [Maxwell 00]
  - ♦ **Spatial Analysis** [Daasch 00]



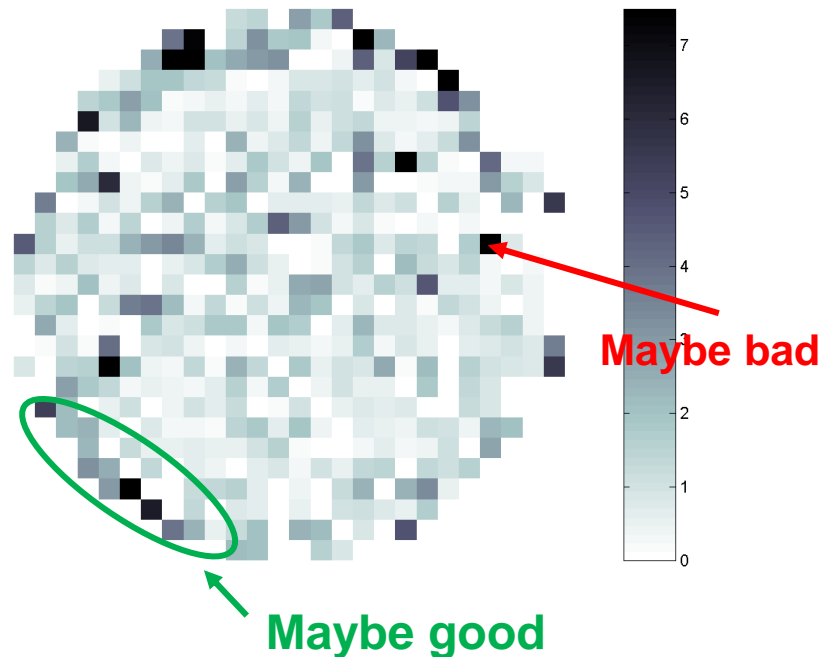
# Current Ratio [Maxwell 00]

- Measure all  $I_{DDQ}$  (without single pass/fail threshold)
- Plot  $I_{DDQ \text{ max}}$  v.s.  $I_{DDQ \text{ min}}$  of many chips
  - ♦  $I_{DDQ \text{ max}} = K I_{DDQ \text{ min}} + \text{Intercept} + 3\sigma$
- **Outliers** fail the test



# Spatial Analysis [Daasch 00]

- Idea:  $I_{DDQ}$  correlates to die neighbors
- *Nearest Neighbor Residue (NNR)* method
  - ♦ Record all  $I_{DDQ}$  data on a whole wafer
  - ♦ Estimate a die's  $I_{DDQ}$  with the  $I_{DDQ}$  of its neighbors
  - ♦ Fail the test if its measured  $I_{DDQ}$  very different from estimated  $I_{DDQ}$



# Quiz

**Q: Which of following is NOT correct ?**

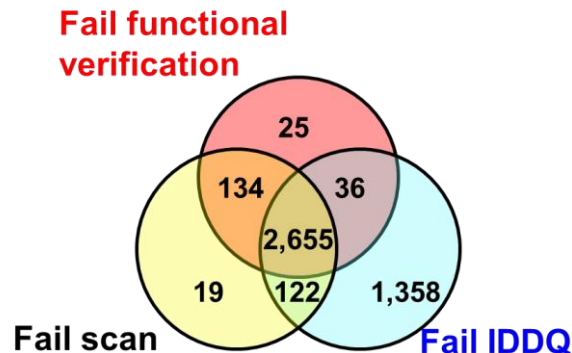
**A:  $I_{DDQ}$  can still be used with careful data analysis**

**B:  $I_{DDQ}$  is lower at lower temperature**

**C: Chips fail  $I_{DDQ}$  are all defective**

# Summary: $I_{DDQ}$ Testing

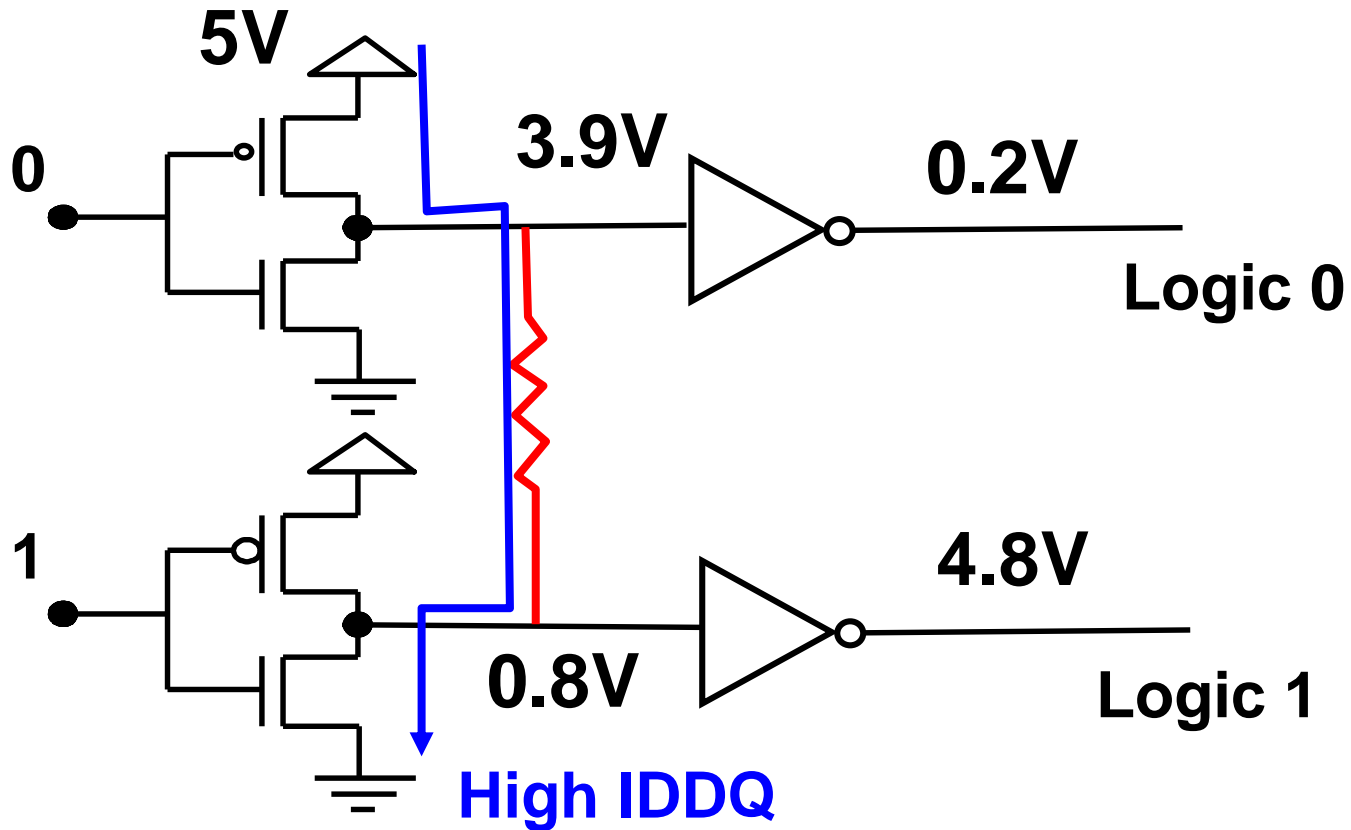
- $I_{DDQ}$  testing improve **reliability** and **DPM**
- $I_{DDQ}$  test patterns
  - ♦ **Toggle test, Pseudo stuck-at test**
- Solutions to enhance effectiveness of  $I_{DDQ}$ 
  - ♦  $\Delta I_{DDQ}$  , **Current Ratios, Spatial Analysis**
- Experimental data
  - ♦ Higher  $I_{DDQ}$  more likely to fail after burn in



**Each Test Detects Unique Defect**

# FFT

- Why bother to detect this defect since it passes Boolean test?



# References

- [Daasch 00] Daasch, “Variance Reduction using Wafer Patterns in IDDQ Data,” ITC pp. 189-198, 2000.
- [Keshavarzi 97] A. Keshavarzi and et. Al., “Intrinsic Leakage in Low Power Deep Submicron CMOS Ics,” ITC, pp.146-155, 1997.
- [Levi 81] M. W. Levi, “CMOS is most testable,” in Int. Test Conf., 1981, pp.217–220
- [Mann 08] W. R. Mann, “Wafer Test Methods to Improve Semiconductor Die Reliability,” IEEE Design & Test of Computers, pp528-537, 2008.
- [Maxwell 00] P. Maxwell et al, “Current Ratios: A self Scaling Technique for Production IDDQ Testing”, ITC 2000
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- [Williams 96] T. Williams and et. al., “ $I_{DDQ}$  Test: Sensitivity Analysis of Scaling,” ITC, 1996.