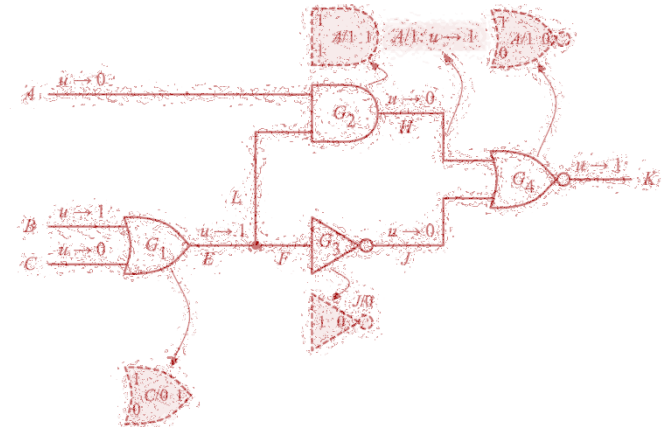


# Fault Simulation

- Introduction
- Fault simulation techniques
- Alternatives to fault simulation
- Issues of fault simulation
- Conclusion

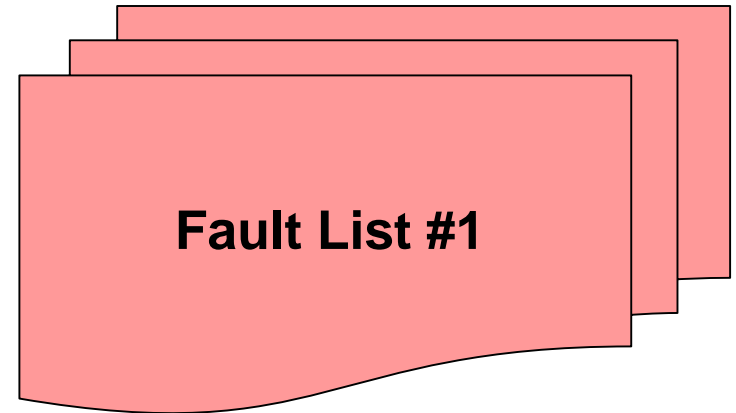


# Issues of Fault Simulations

- Long CPU time
  - ◆ Distributed computing, or Fault sampling
- Large memory requirement
  - ◆ Partition faults into multiple simulation passes
- Potentially detected faults
- Compatibility with logic simulation

# Speed and Memory Solutions

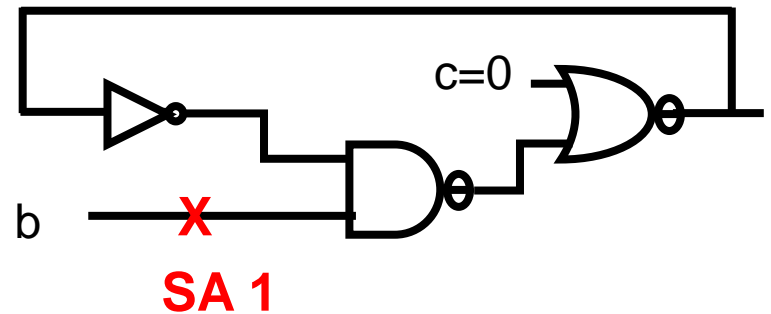
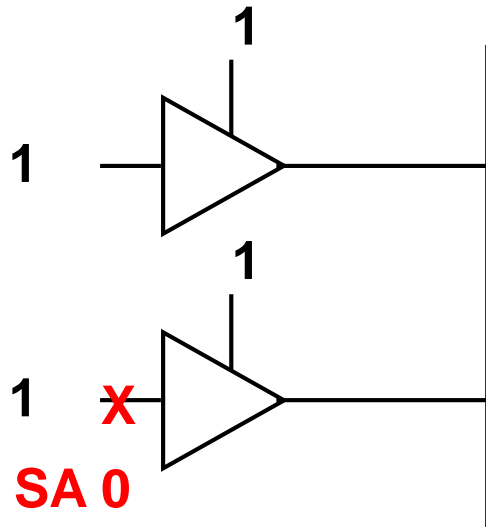
- 1. **Multiple-pass fault simulation**
  - ♦ Run only small portion of faults per pass
- 2. **Distributed fault simulation**
  - ♦ Distribute faults to more than one computers
- 3. **Emulation**
  - ♦ Use hardware emulator, like FPGA



- \*A **simulation pass** is a single simulation run
  - ♦ from beginning to end of test patterns

# Potentially Detected Faults

- DEF: faults that may or may not be detected in practice
  - ♦ Detection cannot be determined by fault simulation
- Possible reasons for potentially detected faults
  - ♦ Bus contention, Oscillation, High impedance, Unknown
- Examples:



**Fault detected?**

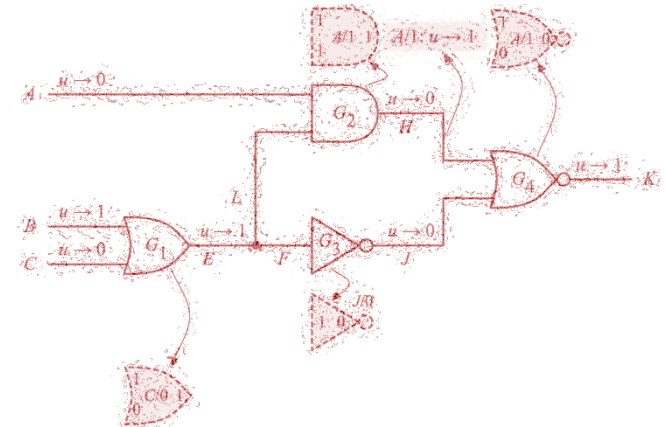
- Different tools have different ways to calculate FC
  - ♦ Please see tool manual for details

# Compatibility with Logic Simulation

- To speed up fault simulation, many tools requires circuits to be represented in a library models pre-defined by tools
- Functional verification logic simulations often involve mixed-level codes, which make such modeling very difficult
  - ◆ Circuit delay
  - ◆ RTL behavior description
  - ◆ *User Defined Primitives* (UDP)
    - \* DFF, MUX

# Fault Simulation

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# Quiz: Comparison of Techniques

| Items               | Serial | PPSFP | Deductive | Concurrent | Differential |
|---------------------|--------|-------|-----------|------------|--------------|
| unknown logic value | 😊      | 😊     | 😞         | 😊          | 😊            |
| Delay model         |        |       |           |            |              |
| Run time            |        |       |           |            |              |
| Sequential circuits |        |       |           |            |              |
| Memory              |        |       |           |            |              |

# Conclusion

- **Usage of fault simulation**
  - ◆ **ATPG, fault grading, diagnosis**
- **Techniques**
  - ◆ **Serial, parallel, PPSFP, deductive, concurrent, differential**
- **Most popular technique in industry now**
  - ◆ **PPSFP is simple for comb. ckt (or seq. ckt with full scan)**
  - ◆ **Concurrent and differential good for both comb./seq. ckt**



# Commercial Tools

- **Cadance**
  - ◆ **Verifault**
- **Mentor Graphic:**
  - ◆ **Fastscan, flextest**
- **Synopsys**
  - ◆ **Tetramax**
- **Syntest**
  - ◆ **Turboscan**
  - ◆ **TurboFault**

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