Fault Modeling

- **Introduction**
- **Fault Models**
  - ♦ Stuck-at fault (1961)
  - ♦ Bridging fault (1973)
  - ♦ Delay fault (1974)
  - ♦ **Transistor-level fault**
    - * **Stuck-open (1978)**
    - * **Stuck-on**
    - * **Cell-aware (2009)**
  - ♦ **Review**
- Fault Detection
- Fault Coverage
- Conclusion

1
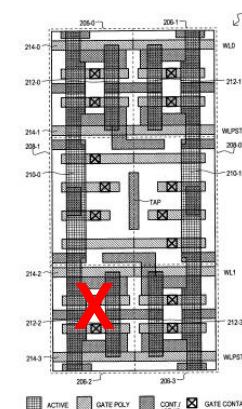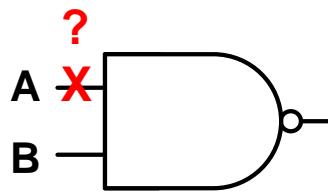
Why Faulty NAND Has Memory ?

- **Stanford Murphy Experiment [Li 01]**
  - ◆ *Sequence Dependency*: **Test result depends on test sequence**
- **Example: NAND gate**
  - ◆ **Same test patterns {11, 01, 00}, but in different sequence**
  - ◆ **Sequence 1 fails; Sequence 2 passes**
  - ◆ **Is it A SA1 or not?**

Sequence 1

A	B	Out$_{good}$	Out$_{faulty}$
1	1	0	0
0	1	1	0
0	0	1	1
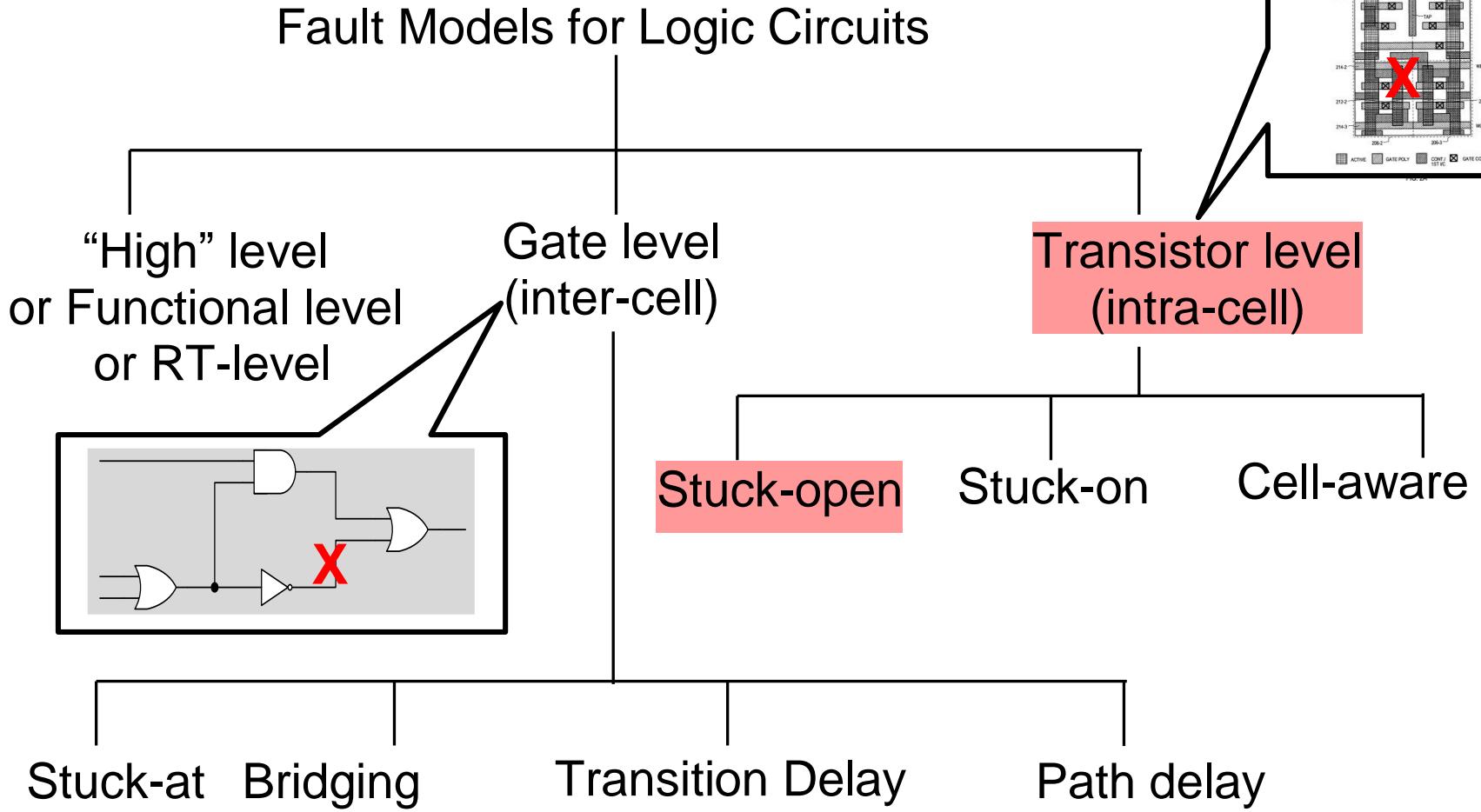
← **A SA1 ?**

Sequence 2

A	B	Out$_{good}$	Out$_{faulty}$
0	0	1	1
0	1	1	1
1	1	0	0

← **Not A SA1 ??**
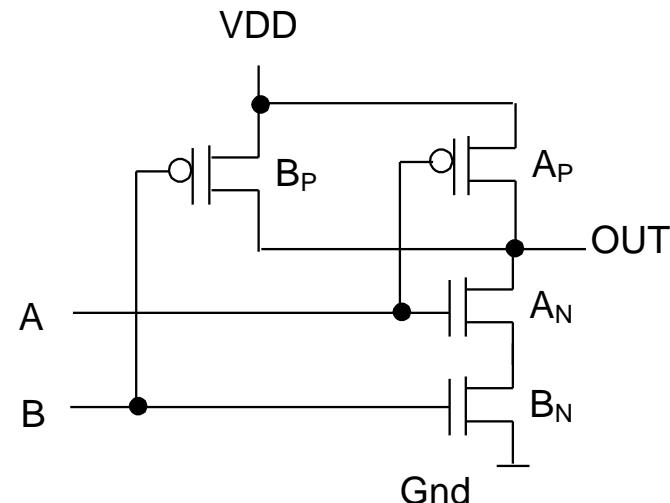
SSF Cannot Explain Seq. Dep.

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Classification of Fault Models

Fault Models for Logic Circuits

"High" level
or Functional level
or RT-level

Gate level
(inter-cell)

Transistor level
(intra-cell)

Stuck-open   Stuck-on   Cell-aware

Stuck-at   Bridging   Transition Delay   Path delay

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Stuck-open Fault [Wadsack 78]

- ***Stuck-open (SOP) fault***
  - ♦ **Faulty transistors is always off**
- **Example: NAND**
  - ♦ **$11 \to 01$ detects A_P SOP**
  - ♦ **Totally 4 faults: A_P B_P A_N B_N**
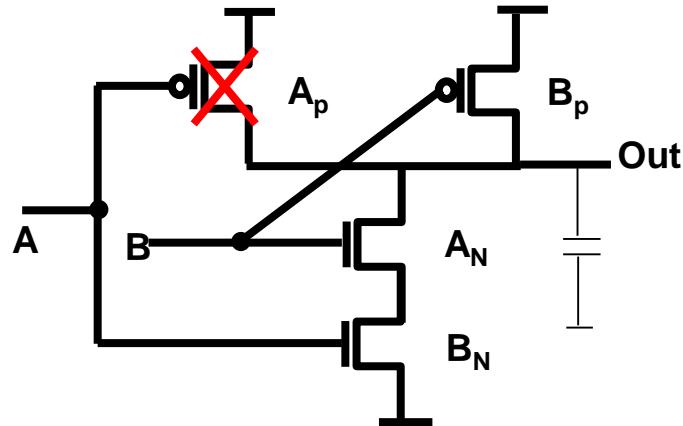
Input A B	Fault-free Output	Faulty Outputs Z = high impedance			
		A_P	A_N	B_P	B_N
0 0	1	1	1	1	1
0 1	1	Z	1	1	1
1 0	1	1	1	Z	1
1 1	0	0	Z	0	Z

SOP Requires 2-pattern Test

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Sequence Dependency

- **SOP Faulty circuit has *memory* (due to parasitic capacitor)**
  - **Test results depend on sequence of test patterns**
- **Example: A_p stuck-open fault,**
  - **Same test patterns{11, 01, 00}, but different sequence**
  - **Sequence 1 fails; Sequence 2 passes (test escape)**


Sequence 1

A	B	Out$_{good}$	Out$_{faulty}$
1	1	0	0
0	1	1	0
0	0	1	1

**FAIL:
Fault detected**

Sequence 2

A	B	Out$_{good}$	Out$_{faulty}$
0	0	1	1
0	1	1	1
1	1	0	0

**PASS:
Fault undetected
(test escape)**

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# Simulation Results [Millman 89]
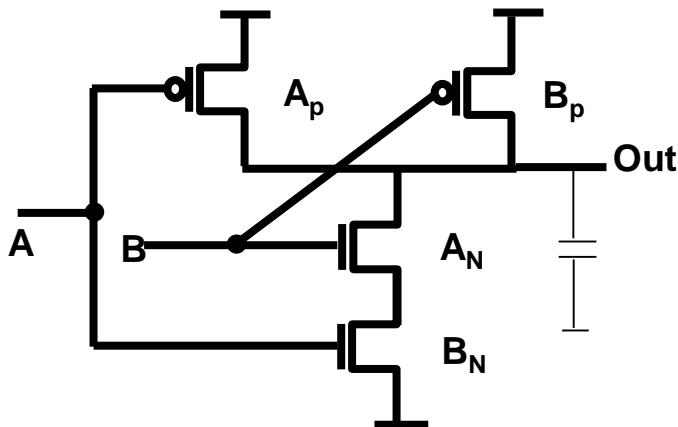
- **Q: How effective is SSF test sets for stuck-open faults?**
- **74LS181 ALU**
  - **Total 426 stuck-open faults**
  - **100% SSF tests cannot achieve 100% SOP fault coverage**

Test set	Krish	Br2	Goel	Mc1	Hugh
Test Length	12	14	35	124	135
SSF fault coverage %	100	100	100	100	100
SOP fault coverage %	79.3	79.6	90.8	87.1	93.4

SSF Not Enough for SOP

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SOP ≠ TDF [Li 02]

- **TDF is correlated with SOP fault, but they are NOT the same**
- **{11→01, 01→10, 00→11} has 100% TDF coverage**
  - **but only 75% SOP fault coverage (missed B_P)**

$A_1B_1 \rightarrow A_2B_2$	Out_{good}	Detected SOP	Detected TDF
11→01	0→1	A_P	A STF; Out STR
10→01	1→1	-	A STF
11→10	0→1	B_P	B STF; Out STR
01→10	1→1	-	B STF
00→11	1→0	$A_N B_N$	A STR; B STR Out STF

TDF Not Enough for SOP, Either

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Experimental Results [Woodhal 87] [Li 01]

- 1 μm CMOS [Woodhal 87]
  - Total population: 4,552 chips (passed parametric test)
    - 1,225 chips failed stuck-at test
    - **44** chips **(3.6% of 1225)** failed stuck-open test
    - **4** chips failed stuck-open test **escaped** stuck-at test
- 0.7μm CMOS, *Stanford Murphy experiment* [Li 01]
  - Total population 5.5K chips tested
    - 116 defective chips
    - **7** single stuck-open fault diagnosed
    - **2** multiple faults (stuck-at + stuck-open)

- About **5%** of failed chips are stuck-open

Stuck-open Cannot be Ignored

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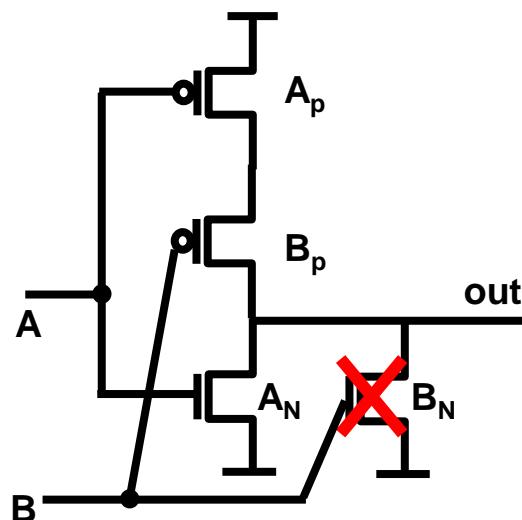
Quiz

Q1: Find a sequence of 2 patterns to detect B_N SOP fault in NOR

A:

**Q2: Find a sequence of 2 patterns that cannot detect B_N SOP fault (test escape)**

A:
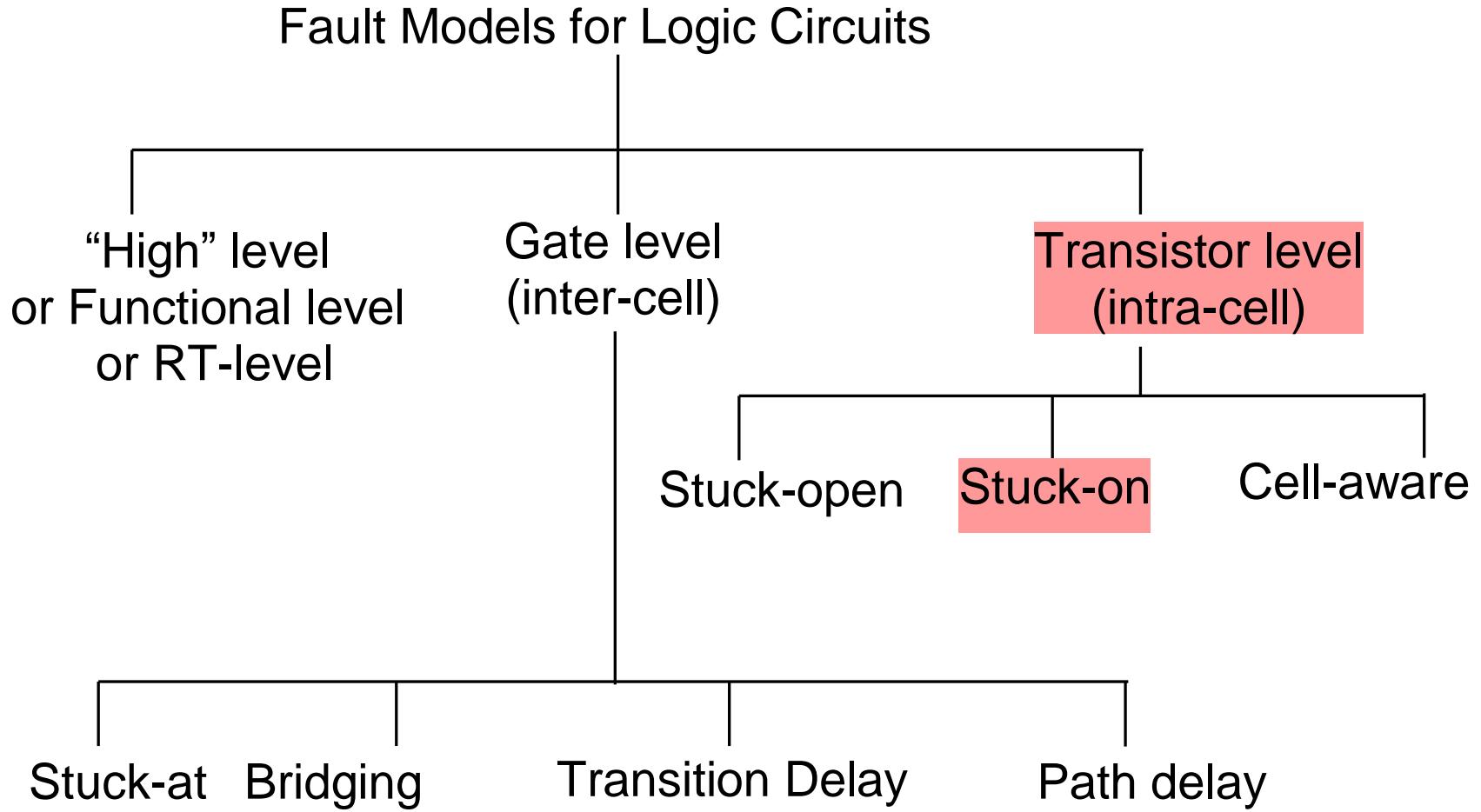
Sequence 1

A	B	Out$_{good}$	Out$_{faulty}$

Sequence 2

A	B	Out$_{good}$	Out$_{faulty}$

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Stuck-at   Bridging   Transition Delay   Path delay

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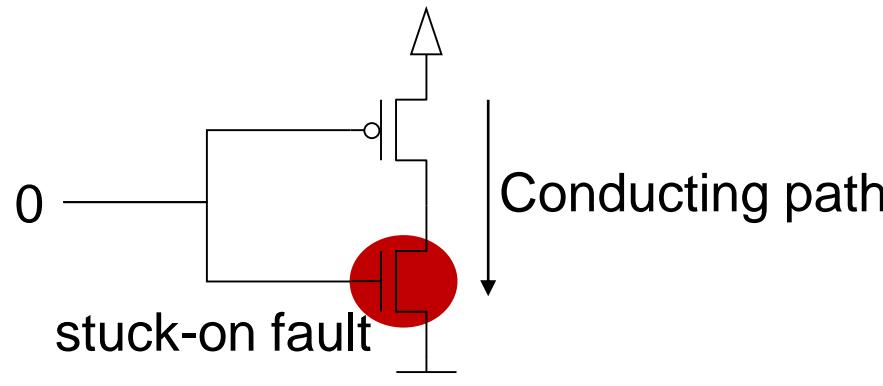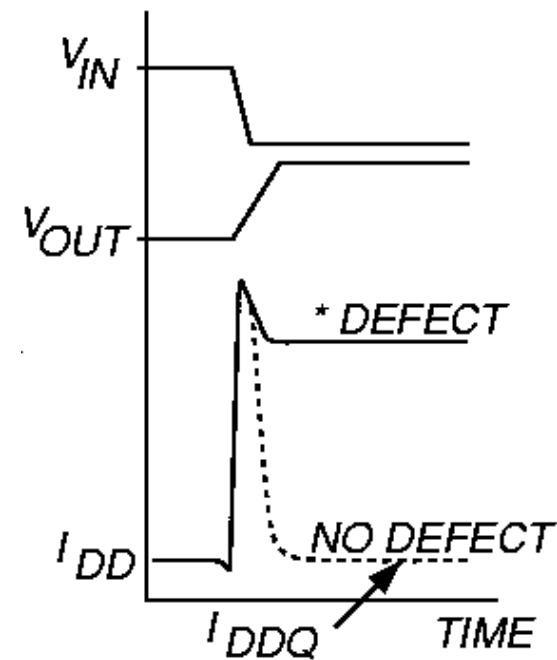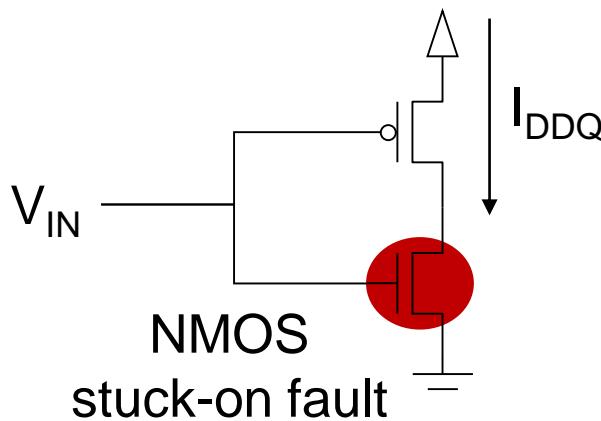
Stuck-On Fault

- **Faulty transistor is always on**
  - ◆ **Form a conducting path between Vdd and Gnd in static state**
- **Stuck-on fault may NOT be detected by Boolean testing**
  - ◆ **Output logic values depends on relative impedance of transistors**
- **Stuck-on fault can be detected by I_{DDQ} testing**
  - ◆ **Apply test pattern**
  - ◆ **Wait for a while**
  - ◆ **Measure *quiescent current* from power supply**

0

Conducting path

stuck-on fault

I_{DDQ} Testing [Mark 81]

- **Measure static power supply current, with test patterns applied**
  - ◆ **I_{DD} = power supply current from V_{DD}**
  - ◆ **Q = quiescent**
- **Very commonly used in CMOS technology***
- **Example: NMOS stuck-on fault**
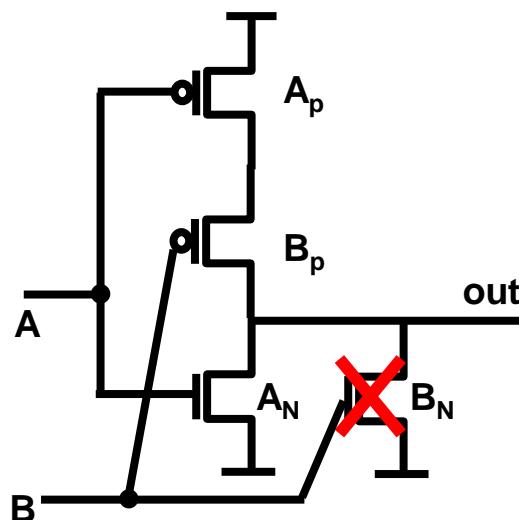
*but I_{DDQ} less effective for new technologies due to leakage

V_{IN}

I_{DDQ}

NMOS
stuck-on fault

V_{IN}

V_{OUT}

* DEFECT

I_{DD}

NO DEFECT

I_{DDQ} TIME
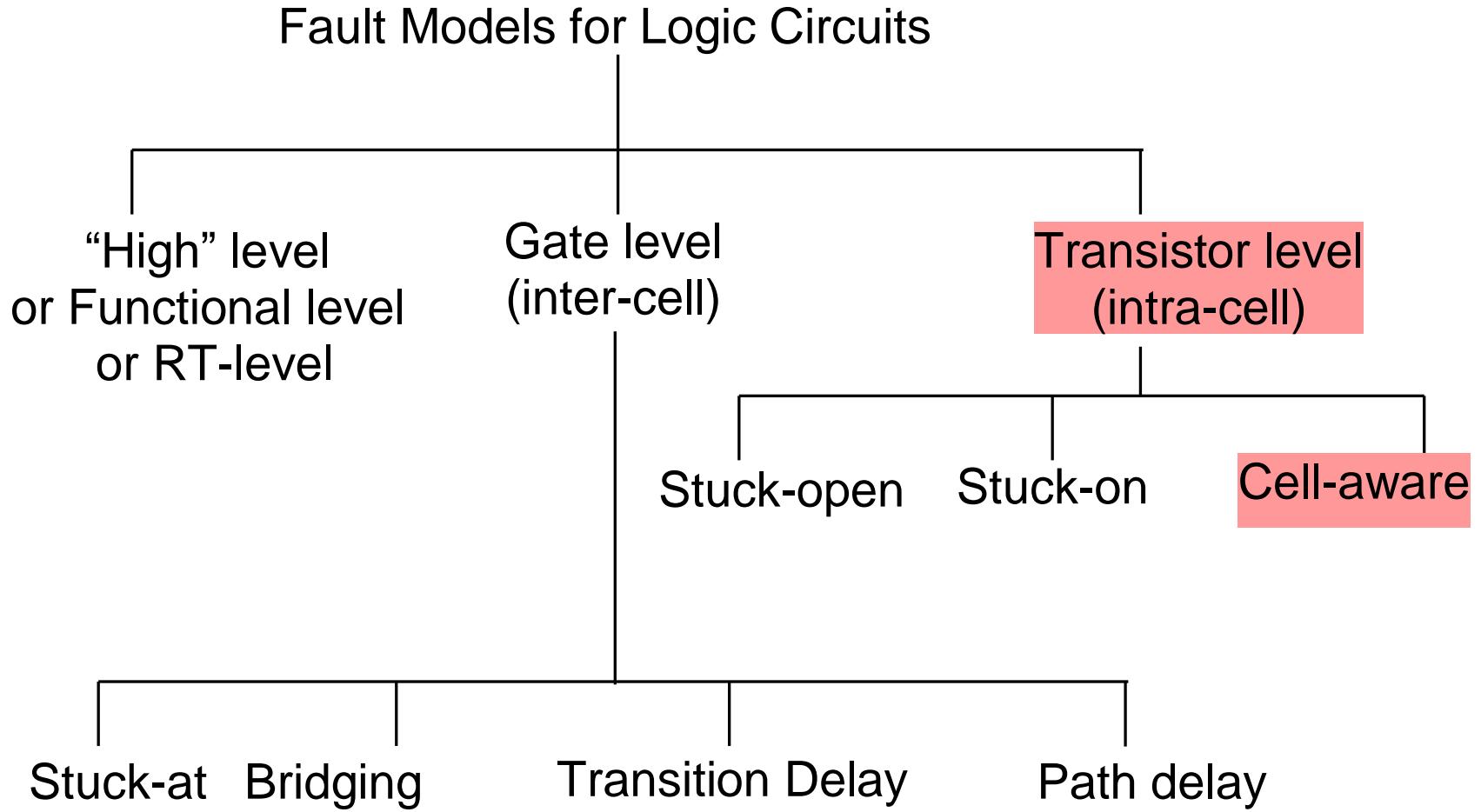
Quiz

Q: Find a test pattern to detect B_N Stuck-on fault in NOR by I_{DDQ}

A:

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Stuck-at   Bridging   Transition Delay   Path delay
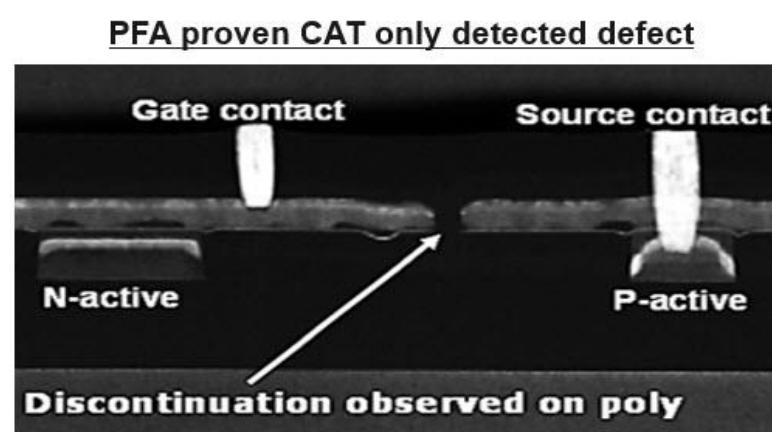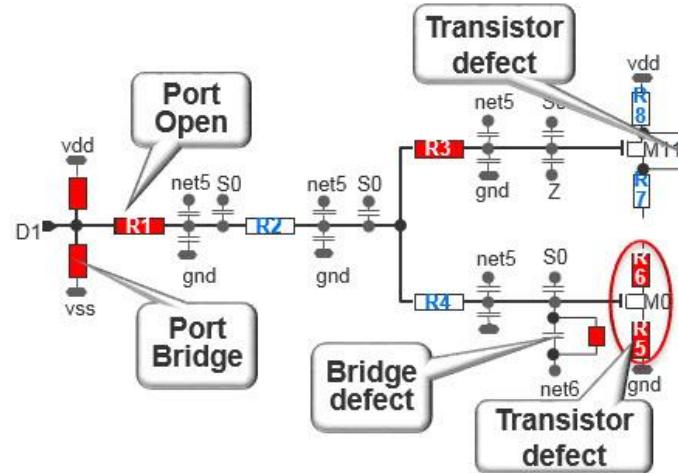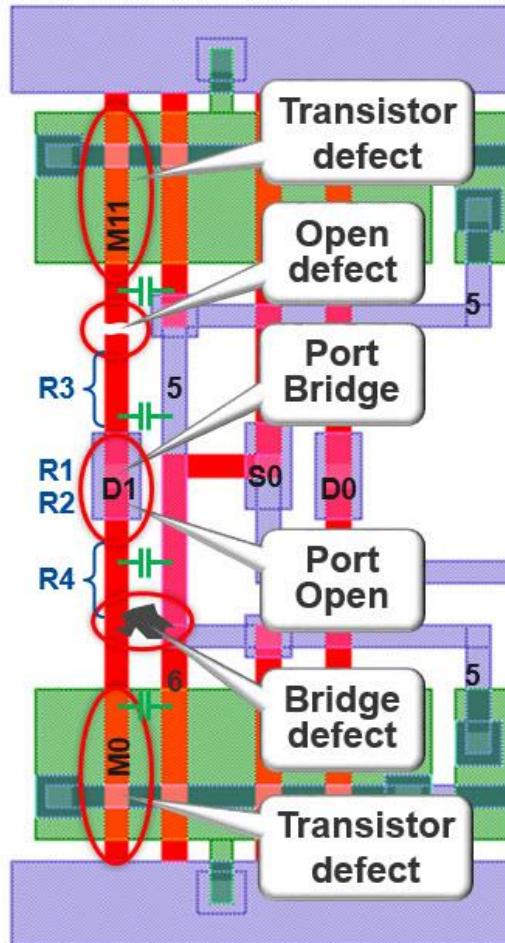
Cell-aware Test (CAT) [Hapke 09]

- **Consider different defects types inside cell: open, bridge, transistor**
- **Need *layout extraction* and *analog fault simulation***


PFA proven CAT only detected defect
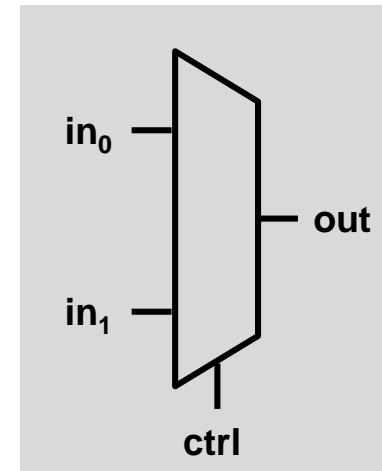
[Mentor website]

Why CAT more Effective?

- **4** test patterns detect **8** SSF at MUX I/O pins
  - ♦ **100% SSF coverage**
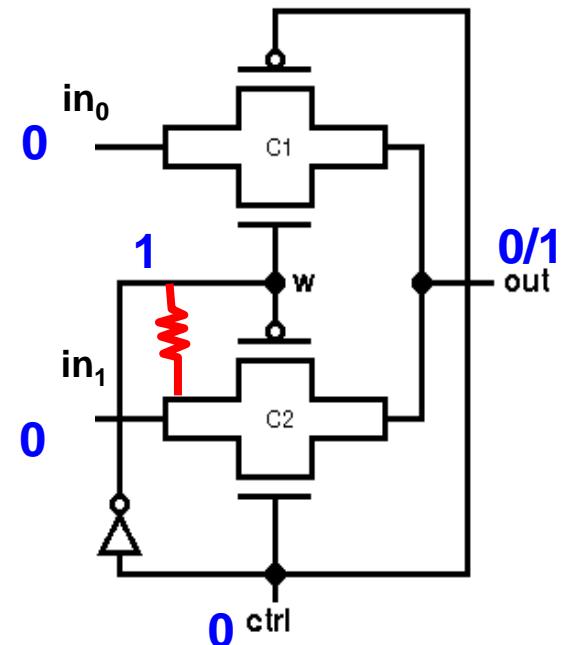
in_0	in_1	ctrl	out	detected SSF
0	1	0	0	ctrl SA1, out SA1, in_0 SA1
1	0	0	1	in_1 SA1
1	0	1	0	ctrl SA0, out SA0, in_0 SA0
1	1	1	1	in_1 SA0

- **CAT adds {000} to detect in_1/w bridging**
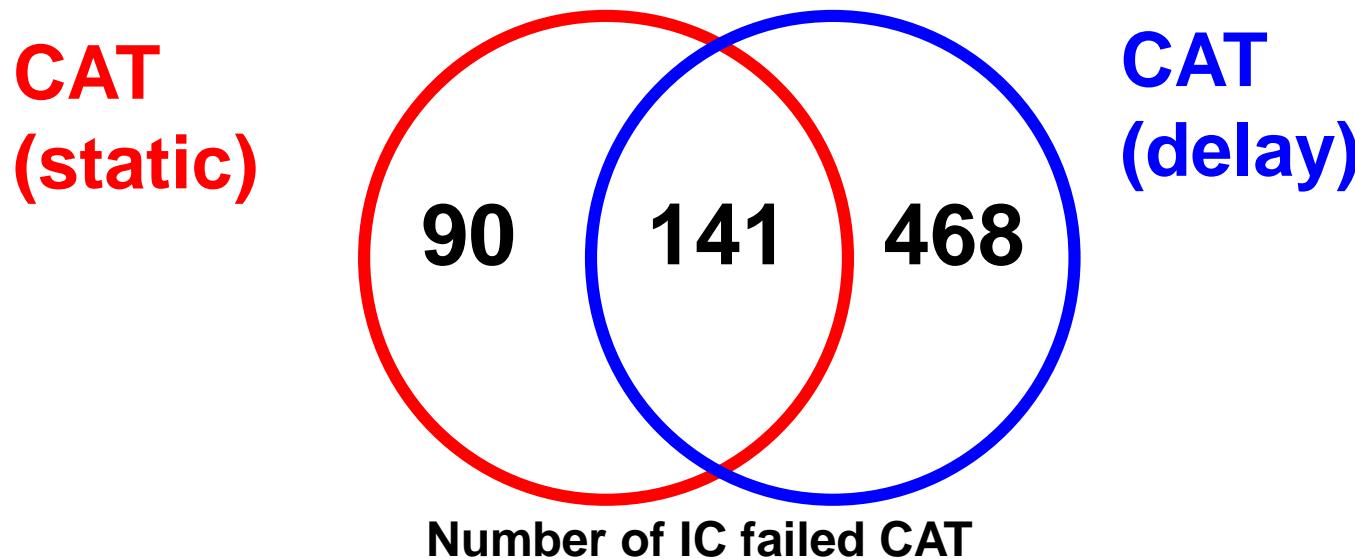
in_0	in_1	ctrl	out
0	1	0	0
1	0	0	1
1	0	1	0
1	1	1	1
0	0	0	0/1

CAT is Effective but Longer

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Experimental Results [Hapke 14]

- **AMD 32 nm, total 800K IC tested**
- **699 IC failed only CAT, passed other tests**

CAT (static)   90   141   468   **CAT (delay)**

Number of IC failed CAT

CAT Improves 885DPM

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- **<u>Fault Models</u>**
  - ◆ **Stuck-at fault (1961)**
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  - ◆ **Delay fault (1974)**
  - ◆ **Transistor-level fault (1978)**
 - ◆ **<u>Review</u>**
- **Fault Detection**
- **Fault Coverage**
- **Conclusion**

FIG. 2A

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Stuck-open
1978

Stuck-on
➡ **2009**

Cell-aware

Stuck-at
1961 ➡

Bridging
1973 ➡

1974 (Delay)

Transition Delay
Path Delay
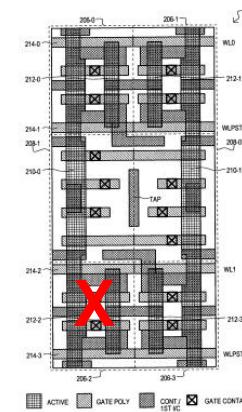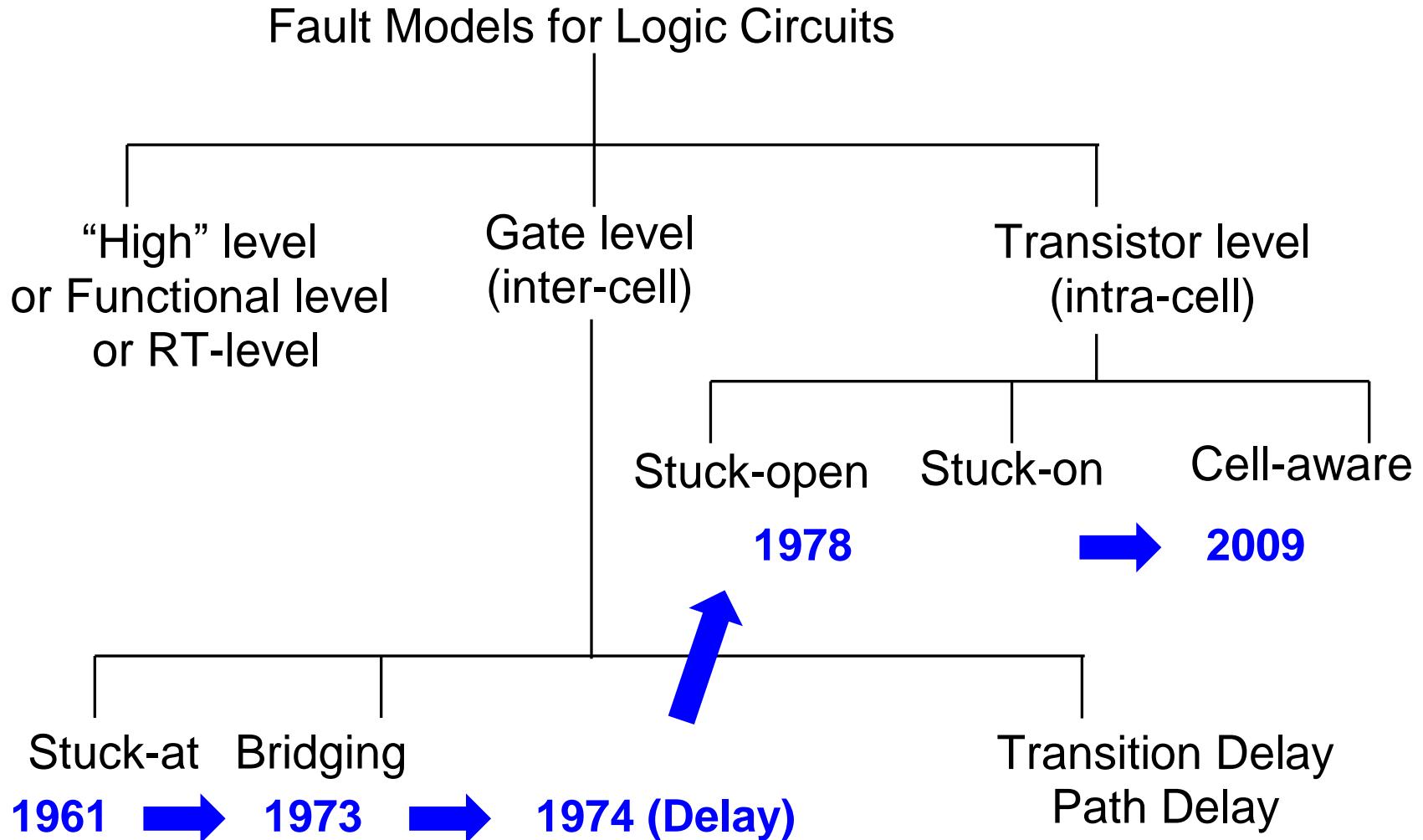
Fault Models Evolve with Technology

More Classifications

- **According to timing**
    - *AC faults*: **timing dependent**
        - ∗ **Delay faults**
    - *DC faults*: **not timing dependent**
        - ∗ **Stuck-at faults, stuck-open faults …**
- **According to memory effect**
    - *Sequential faults*: **faults that increase number of states**
        - ∗ **Stuck-open faults, feedback bridging faults**
    - *Combinational faults*: **faults do not increase number of states**
        - ∗ **Stuck-at faults, non-feedback bridging faults**
- **According to circuit under test (CUT)**
    - *Memory* **fault model (see** *memory testing* **chapter)**
    - *FPGA* **fault model**
    - **…**

No Single Best Fault Model for All Circuits

Summary

① **Transistor stuck-open (SOP)**

   ♦ **Sequence dependence**: faulty comb. logic has memory

   ♦ **TDF $\neq$ SOP**

② **Transistor stuck-on**

   ♦ **I_{DDQ} testing**

③ **Cell-aware testing**

   ♦ layout extraction + analog fault simulation

   ♦ **Improved DPM** but **longer** test

FIG. 2A

● **Fault models evolve with technology**

   ♦ **NO single best fault model** for all circuits

   ♦ New fault models needed for future technologies!

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