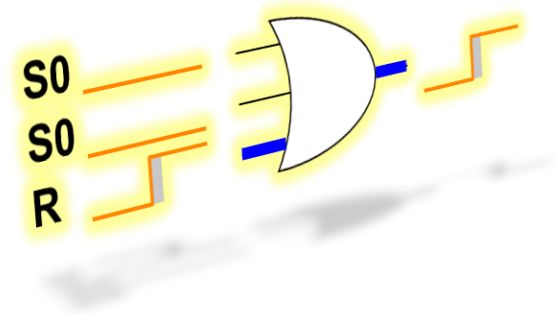


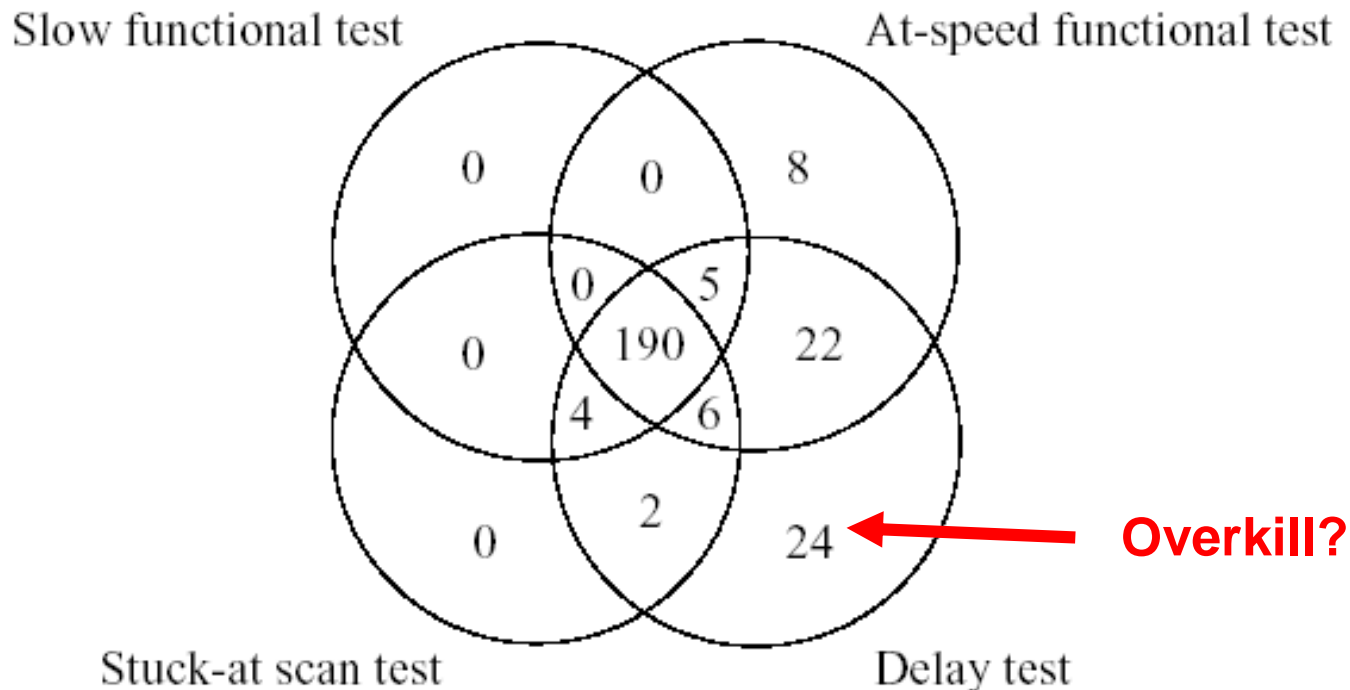
# Delay Test

- Introduction and delay fault models
- Path Delay Fault
- Transition Delay Fault
- **Experimental Results\* (not in exam)**
- **Issues of Delay Tests\*** (not in exam)
- **Conclusions**



# HP Experiment [Maxwell 96]

- Delay testing = TDF + some PDF
- Delay testing detects detected unique CUTs
  - ♦ that escaped other testing



# HP Experiment (Cont'd)

- **Observations: How useful are path delay tests?**
  - ◆ **2,000 longest paths chosen and only 148 paths have robust tests**
  - ◆ **Path delay fault tests only detect 18.5% of devices with delay faults**

# Stanford Experiment [EJM 00]

- Center for Reliable Computing, Stanford
- Murphy Experiment
  - ♦ Goal: evaluate effectiveness of different test techniques
- Murphy Chip
  - ♦ LSI Logic 150k CMOS Gate Array
  - ♦ 25k Gates, all combinational CUTs
  - ♦ 120-Pin Ceramic PGA Package
  - ♦  $L_{\text{eff}} = 0.7\mu\text{m}$
  - ♦ 5 volt Nominal Supply Voltage
  - ♦ Total 5.5K tested
    - \* 116 defective chips found



# SSF Test Results

|                      |             |               |                | Escapes           |               |                |
|----------------------|-------------|---------------|----------------|-------------------|---------------|----------------|
| SSF Tool             | Fault model | Cove-<br>rage | Test<br>length | characte<br>rized | slow<br>(1/3) | slow<br>(1/30) |
| 1**                  | gate        | 100           | 427            | 4                 | 7             | 9              |
| 2*                   | gate        | 100           | 313            | 3                 | 5             | 7              |
| 3**                  | pin         | 100           | 857            | 3                 | 6             | 7              |
|                      | gate        | 100           | 1,000          | 2                 | 5             | 7              |
| 4**                  | pin         | 100           | 456            | 6                 | 8             | 9              |
|                      | gate        | 100           | 603            | 2                 | 4             | 5              |
| 5**                  | pin         | 100           | 466            | 6                 | 9             | 9              |
|                      | gate        | 100           | 571            | 4                 | 6             | 8              |
| 6*                   | gate        | 100           | 547            | 3                 | 7             | 7              |
|                      | gate        | 99            | 532            | 4                 | 8             | 8              |
|                      | gate        | 98            | 490            | 6                 | 9             | 10             |
|                      | gate        | 95            | 467            | 10                | 12            | 13             |
|                      | gate        | 90            | 427            | 15                | 17            | 18             |
|                      | gate        | 80            | 334            | 20                | 23            | 23             |
| Weighted<br>random*  | gate        | 100           | 62,921         | 2                 | 7             |                |
| Weighted<br>random** | gate        | 100           | 21,892         | 2                 | 7             |                |
| Exhaustive           |             |               |                | 0                 | 2             | 4              |

\* academic ATPG tools

\*\* commercial ATPG tools

# Non-SSF Test Results

- delay fault testing does not detect unique defective chips
  - ◆ Performance not particular impressive

| Tool | Fault model                  | Test length | Escapes***    |            | # of CUTs tested |
|------|------------------------------|-------------|---------------|------------|------------------|
|      |                              |             | Characterized | Slow (1/3) |                  |
|      | IDDQ                         | 100         | 15            |            | 116              |
|      | VLV                          |             | 3             | 4          | 116              |
| 1**  | Transition                   | 1,444       | 6             | 8          | 116              |
| 2*   | Stuck open                   | 1,610       | 4             | 9          | 116              |
| 3*   | Gate delay fault             |             | 9             | 11         | 78§              |
|      | Gate delay fault, X->0       |             | 8             | 9          | 78§              |
| 4*   | Robust path delay, X->0      |             | 5             | 5          | 60§              |
|      | Robust path delay, X->random |             | 5             | 5          | 60§              |
| 5*   | Robust path delay            |             | 3             | 5          | 60§              |
| 6**  | Non-robust path delay        |             | 8             | 8          | 60§              |
|      | Non-robust path delay        |             | 2             | 5          | 60§              |
| 7    | Verification                 |             | 6             | 7          | 56§              |

\* academic ATPG tools      \*\* commercial ATPG tools

\*\*\* Tests applied at characterized speed

§ These patterns were not available for all of the CUT

# Delay Test

- Introduction and delay fault models
- Path Delay Fault
- Transition Delay Fault
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- Circuit Model for Delay Test ATPG
- Experimental Results\* (not in exam)
- Issues of Delay Tests\* (not in exam)
- Conclusions

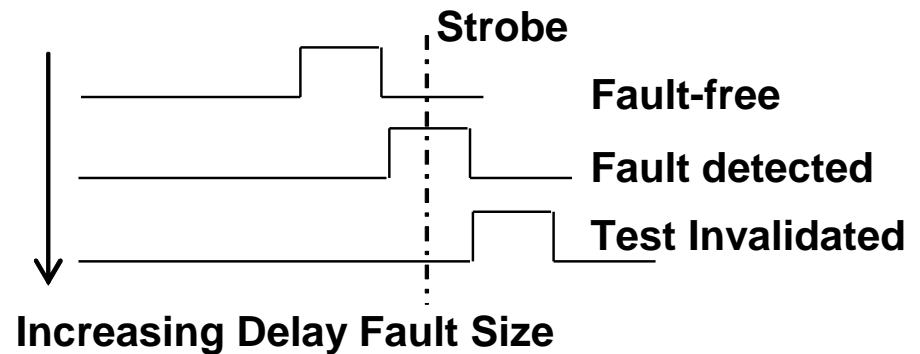
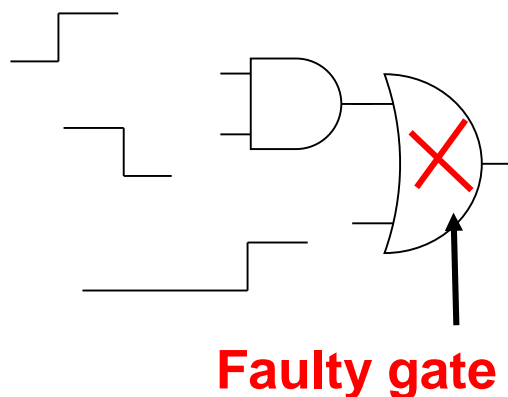
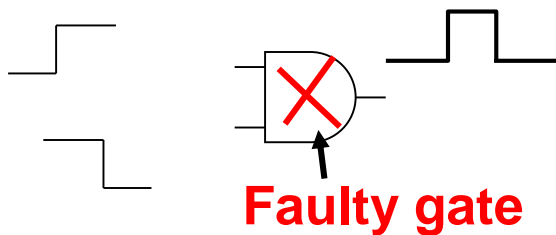
# Issues of Delay Tests

- Path selection is difficult
  - ◆ Too many paths in real circuits
  - ◆ e.g.  $2 \times 10^{20}$  paths in 32-bit multiplier (ISCAS'85 benchmark C6288)
  - ◆ Usually choose timing critical paths
    - \* good to verify the speed, but not good for defect testing
- Need fast ATE to detect small delay faults
- Strobe time hard to determine
- Timing-aware ATPG is slow
- Many untestable paths
- Multi-cycle paths

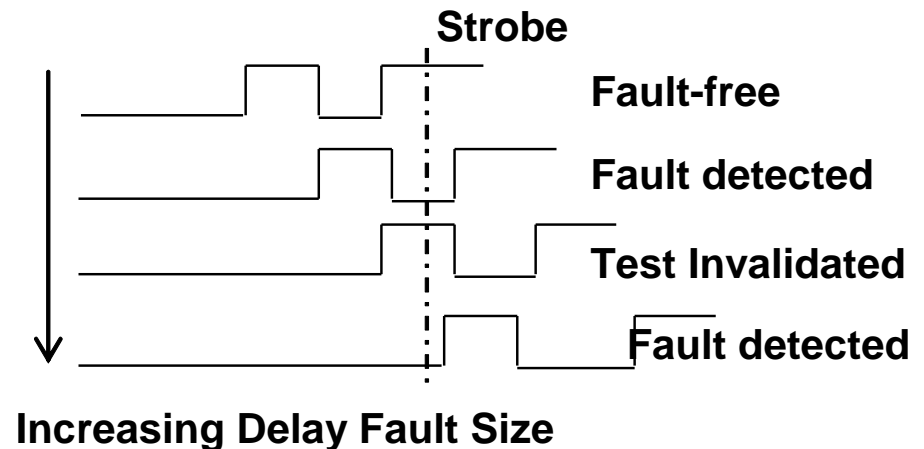


# Strobe Time Hard to Determine

- Strobe time hard to determine in advance
  - ♦ Fault size dependent
  - ♦ Process variation
- Example:

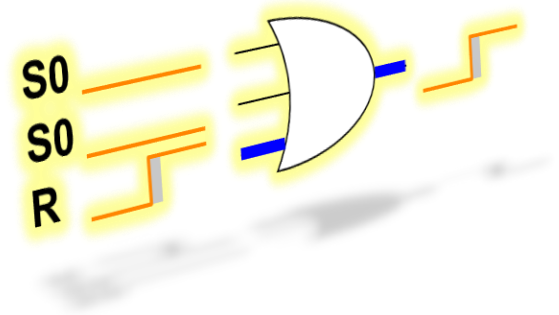


(a)

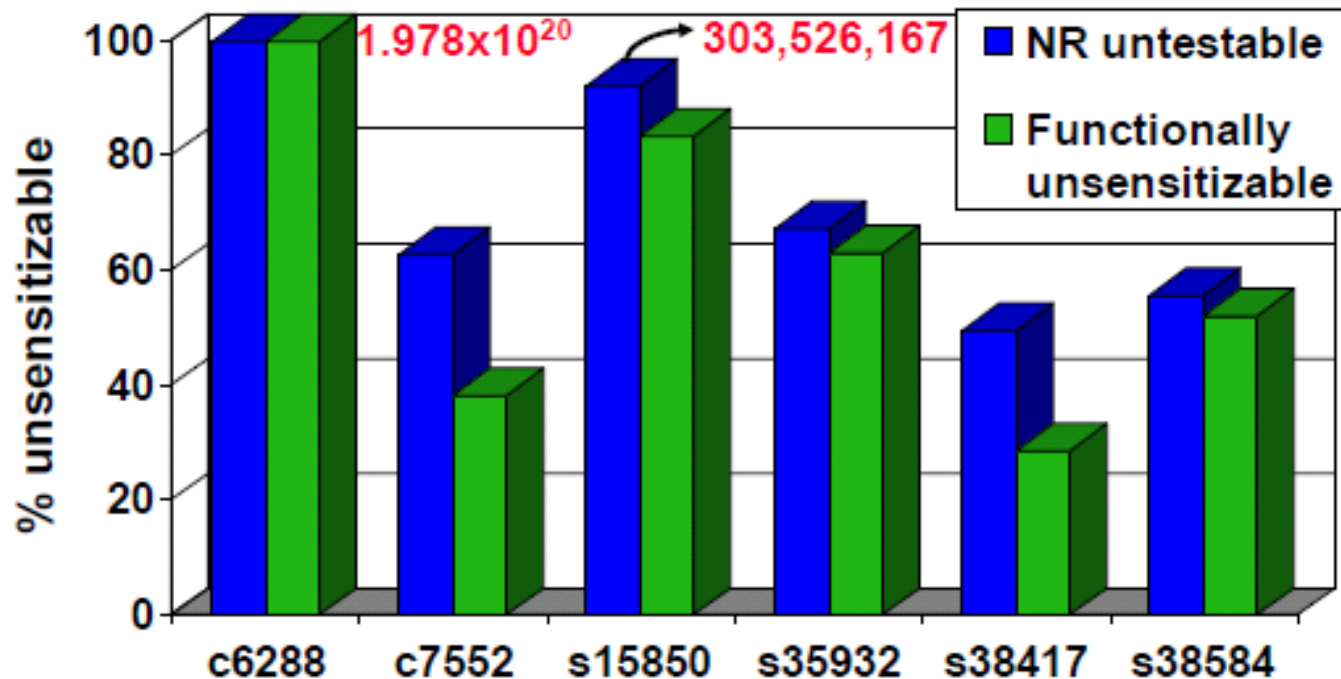


# Delay Test

- Introduction and delay fault models
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# Many Untestable Paths



# Difficulties in Delay Tests

- At-speed testing needs expensive ATE
- Path list hard to generate
  - ◆ Too many paths
- *Small delay faults* occur more frequent in nano-meter technologies
  - ◆ Need propagate fault through long paths
    - \* Timing-aware ATPG is slow
- At-speed delay testing very difficult
  - ◆ How to apply high speed clock in test mode?
  - ◆ At-speed delay testing induces signal/power integrity problem
    - \* IR drop, ground bounce, x-talk noise ...
- Overkill
  - ◆ Some IC fail delay testing but actually work in system
  - ◆ Test too many paths that never used in functional mode?

# Delay Testing Recommendation

- Must do **transition** delay fault ATPG
- Then select some critical paths for **PDF** ATPG
  - ♦ Timing analyzer (STA) selected critical paths
    - \* e.g. >95% clock period
  - ♦ Designers' choice
    - \* Remove special paths: e.g. multi-cycle paths
- If there are too many paths
  - ♦ Choose random samples that are not overlapped
- If they are not testable
  - ♦ Increase sample size or reduce threshold

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