Advanced Topics: ATPG

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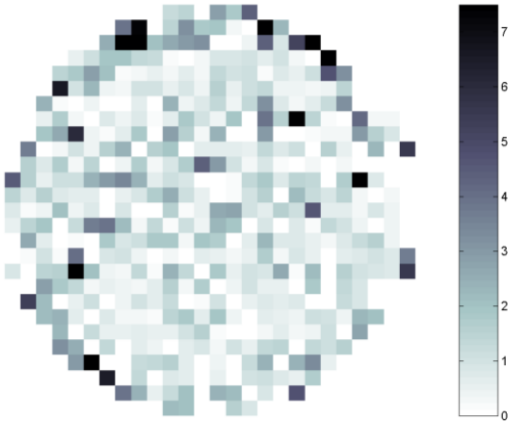
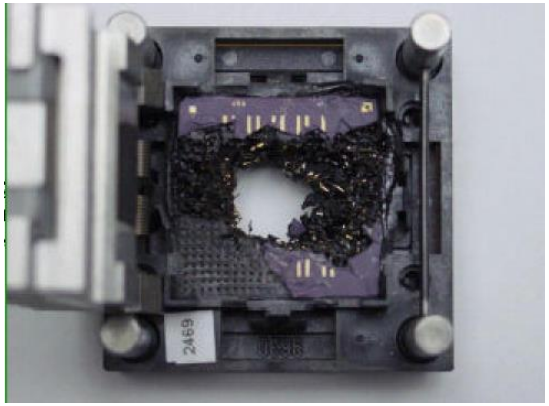
  - **Power-aware ATPG**
    - **Introduction**
    - **DFT solutions**
    - **ATPG solutions (KIT 2005)(Mentor 06)**
    - **Experimental Results**
- Conclusion



$P_{Test} >> P_{Function}$

- Test power is much higher than functional power, because
  - ① Scan chain shifting induces high switching activities
  - ② ATPG patterns are random inputs NOT used in functional mode

- Problems
  - Overkill: good CUT fails testing due to large *power supply noise*
    - Silicon data [Saxena/TI 2003]
  - Reduce lifetime (reliability) of CUT
  - Damage CUT!

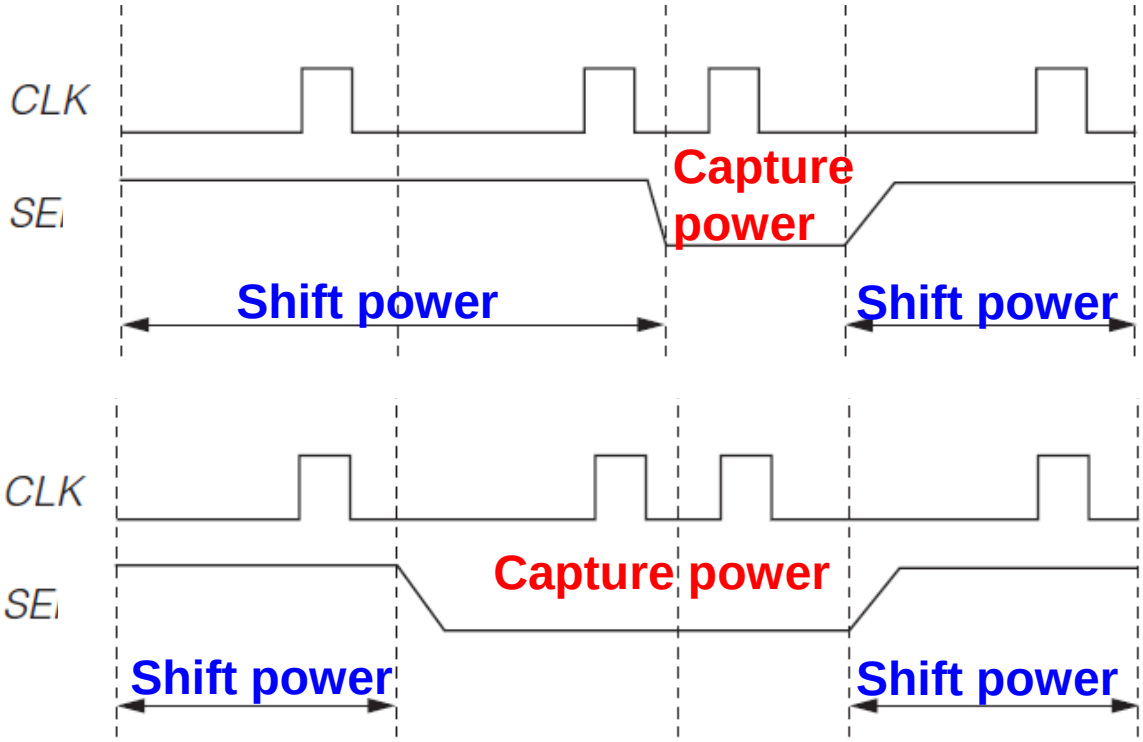


Source: Mill NGBI, 2001

Test Power Is Serious Concern
Especially for High Performance Chips

Two Types of Test Power

- ***Shift power:*** **When SE=1, scan chains shifting**
  - **Can be reduce by slower speed shift**
- ***Capture power:*** **When SE=0, capture cycle**
  - **Especially serious concern for *at-speed testing***
    - **Capture cycle is required to be fast**

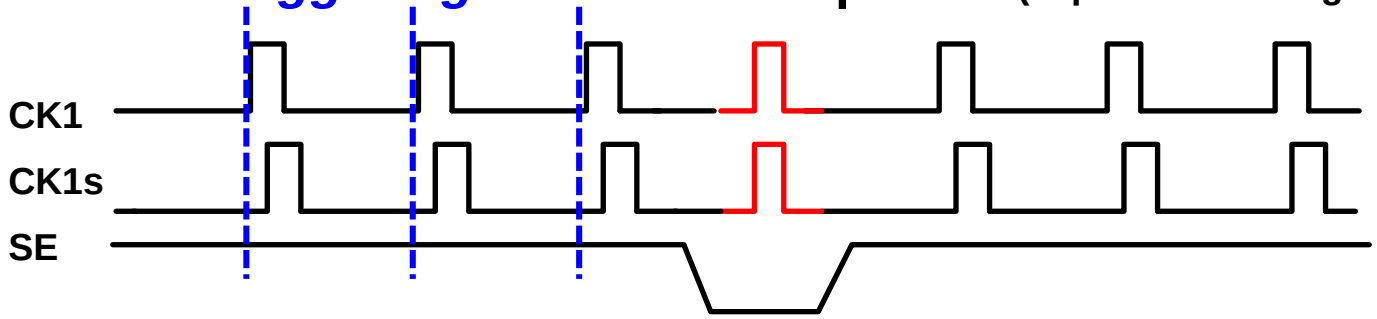


Launch on Shift
(see Video 11.3)

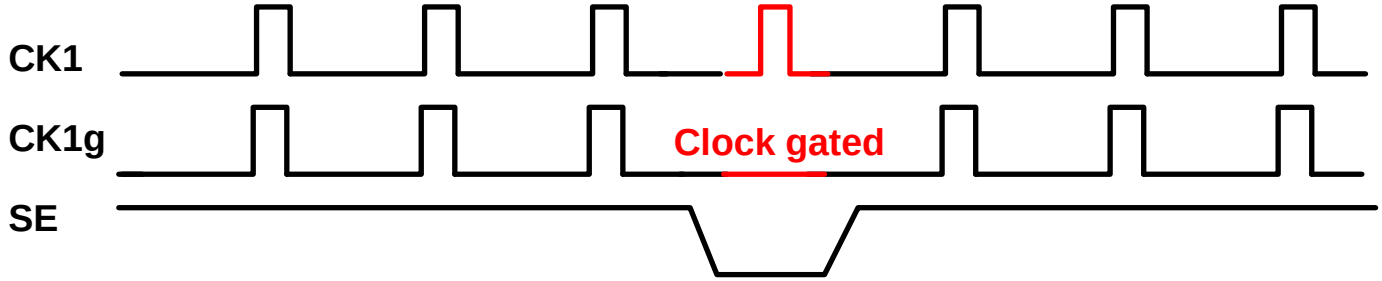
Launch on capture

DfT Solutions [Lee00] [Yoshida02]

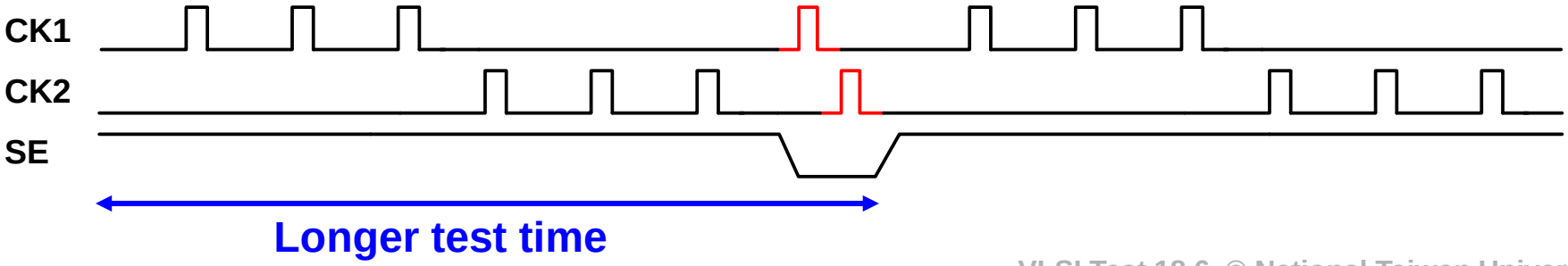
① *Shift Clock Staggering* reduces shift power (capture clock aligned, why?)



② *Capture Clock Gating* reduces capture power



③ *Test Clock Partition* reduced both shift (and capture) power



Pros and Cons

- Advantage of DfT solutions
  - ☺ Very effective
  - ☺ No or little change of ATPG
- Disadvantages of DfT solutions
  - ☹ Area over head
  - ☹ Longer test time or fault coverage loss
  - ☹ More complicated Physical / DfT design flow
    - More test clocks, timing verification

DfT Solution Alone is Not Enough

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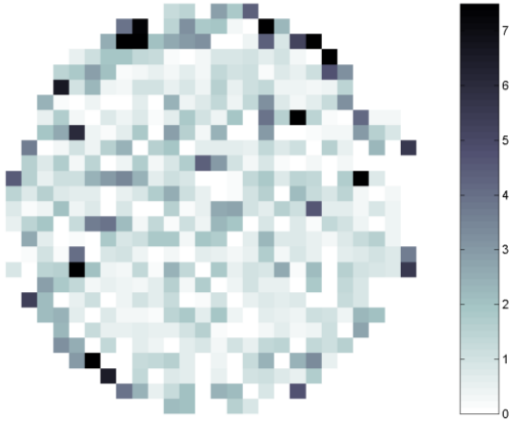
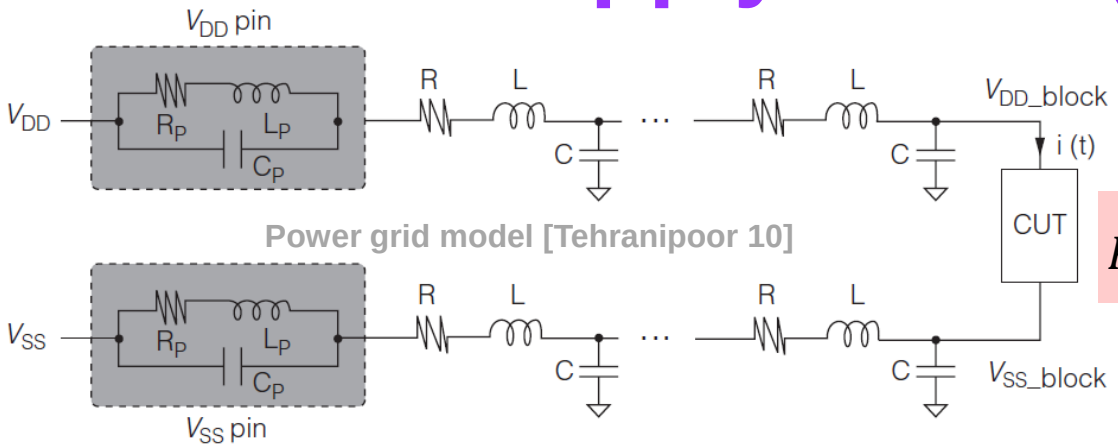


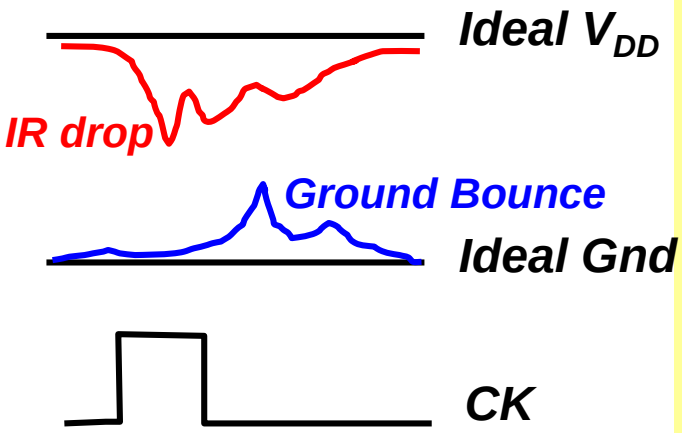
Power Supply Noise (PSN)

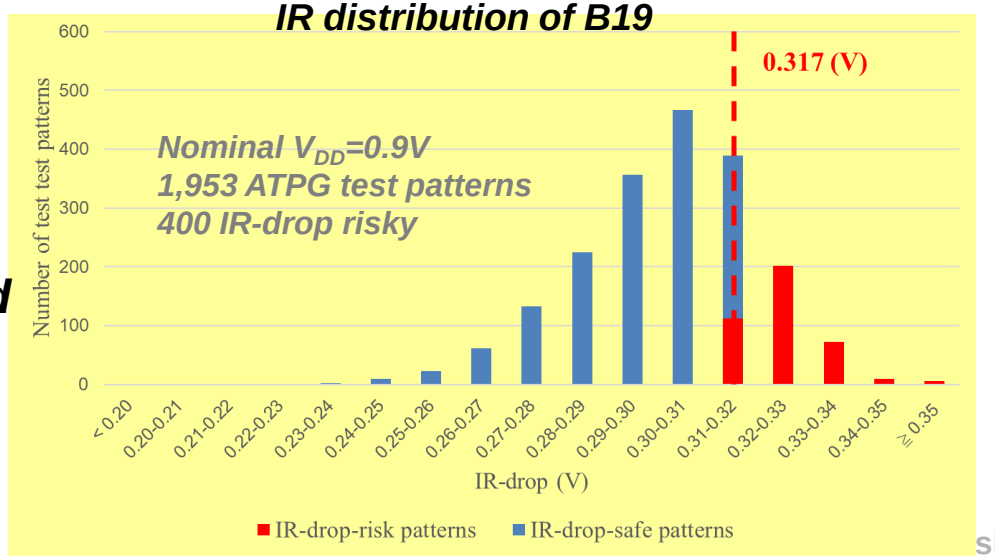


Power grid model [Tehranipoor 10]

$$PSN(t) = L\frac{di(t)}{dt} + Ri(t)$$

- **Two types PSN**
  - ***di/dt*: low/mid frequency, concern of package (not in this lecture)**
  - ***IR drop*/*ground bounce*: high frequency, concern of testing**





IR-Drop Analysis Is Slow

- ***IR-drop analysis*** **is very slow**
  - **Need to inverse large matrices**

$$I = YV \qquad Y^{-1}I = V$$

- **Alternative metrics for IR-drop during ATPG**
  - ① ***Flip-flop Toggle Count (FFTC)***
    - **Number of FFs that toggle**
      - **e.g. totally 4 FF**
      - **0→0,1→0, 1→1, 0→1 FFTC=2**

$$FFTC = \sum_{all\ FF\ k} t_k$$

  - ② ***Weighted Switching Activities (WSA)***
    - **Weighted summation of gate outputs that toggle**
    - **w_i are user defined weights**

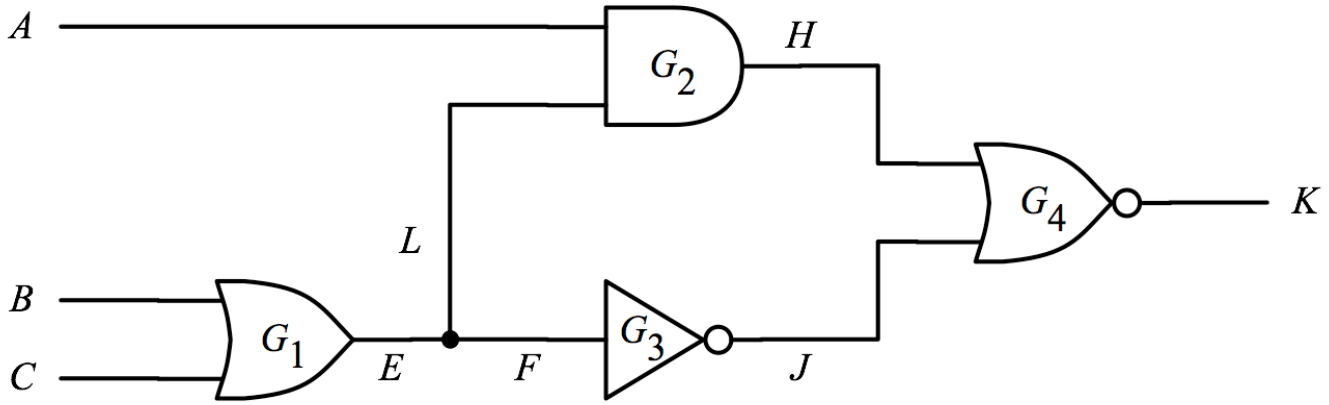
$$WSA = \sum_{all\ gate\ outputs\ i} w_i s_i$$

Quiz

Q: What is WSA of this test pattern pair?
Suppose Inverter weight =1, the other gate weight =2.
A:

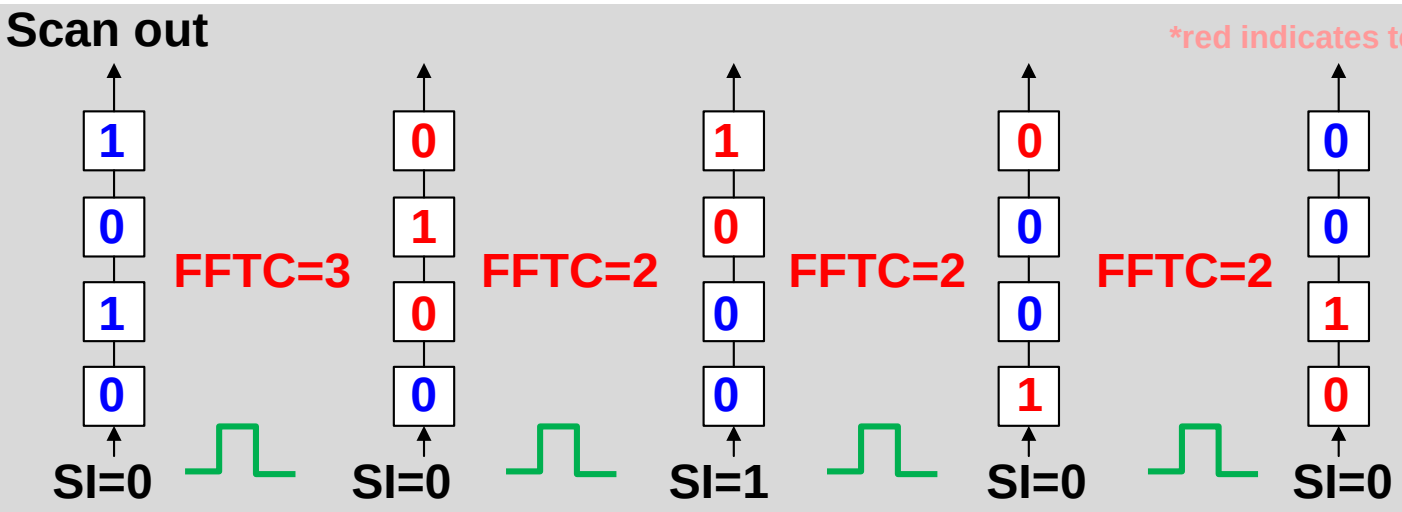
	A	B	C	E	H	J	K
V1	1	0	0	0	0	1	0
V2	1	1	0	1	1	0	0

$$WSA = \sum_{\text{all gate outputs } i} w_i s_i$$

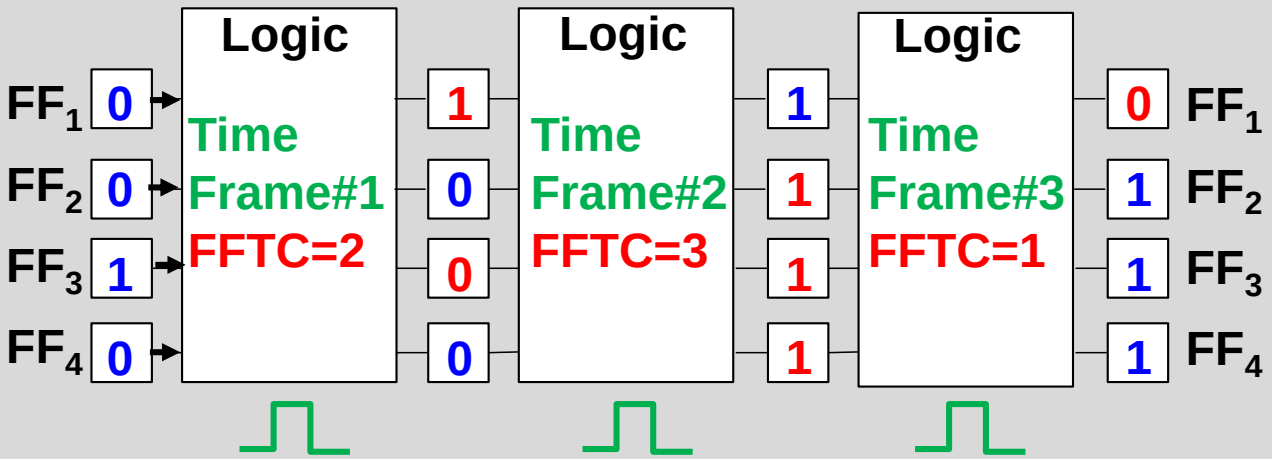


FFTC During Scan Test

Shift mode (4 cycles)



Capture mode (3 cycles)



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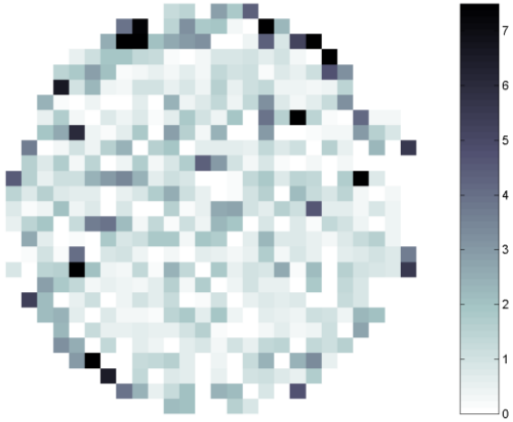
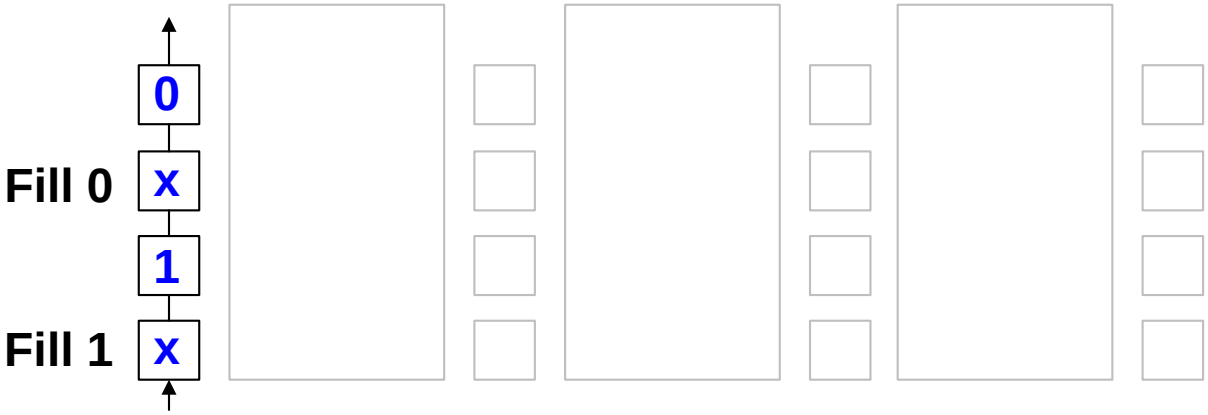


Adjacent Fill [Sankaralingam 00]

- Aka. *Minimum Transition fill*
- To avoid shift power, ATPG fills x the same value as its neighbor
  - Fast and effective because
    - Typical test cubes have many X (>80%) to fill in
- Examples:
  - 1) Before fill 0x1x ; after adjacent fill 0011
  - 2) Before fill 0xxx1xxx; after adjacent fill 00001111



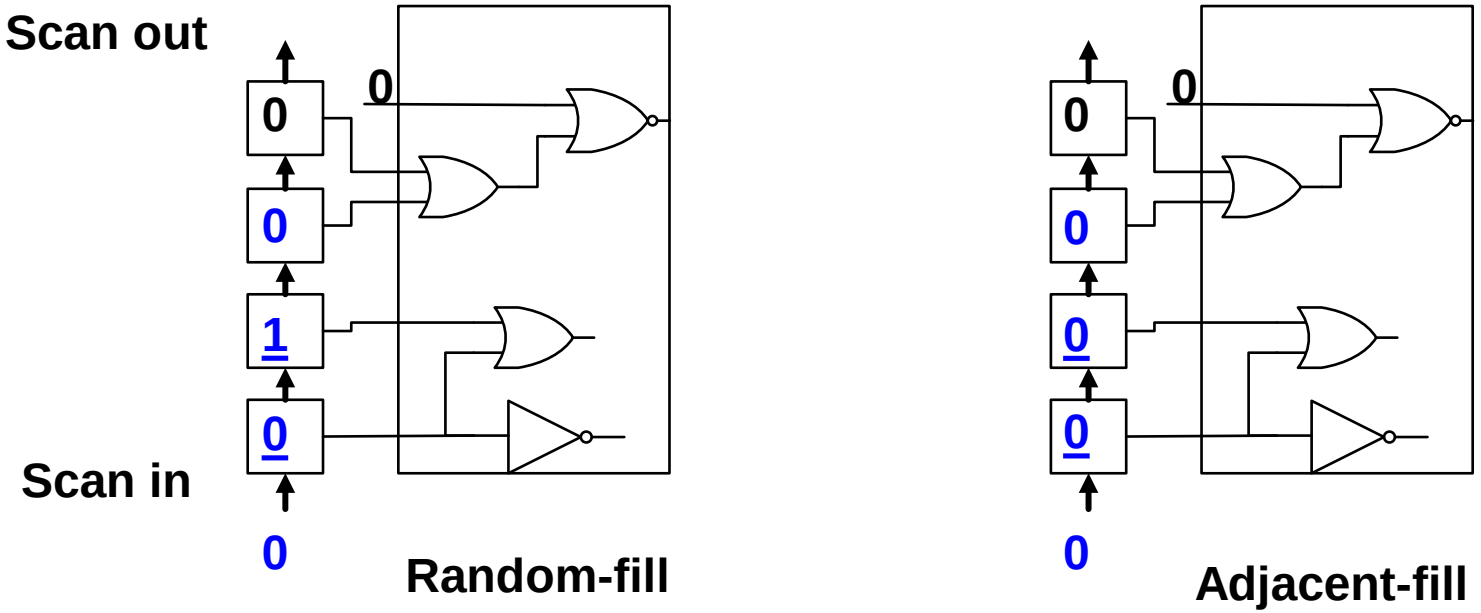
Adjacent Fill Easily Reduce Shift Power

Quiz

Inverter gate weight=1. Other gate weights =2. Suppose PI=0 and last pattern scan out=0. Give a test cube 0xx0,

Q1: What is FFTC and WSA of random-fill pattern when shifted by one cycle?

Q2: What is FFTC and WSA of adjacent-fill pattern when shifted by one cycle?



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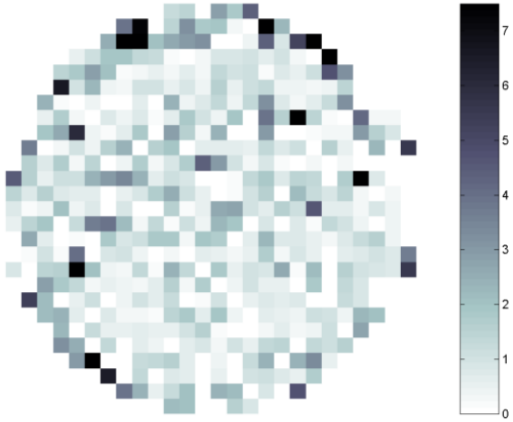
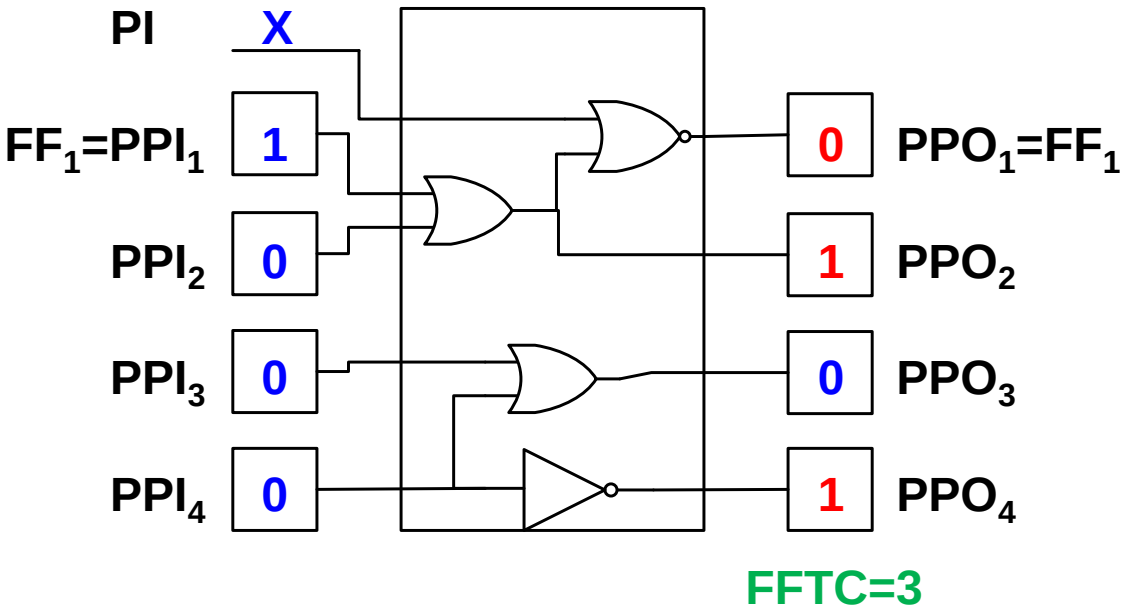


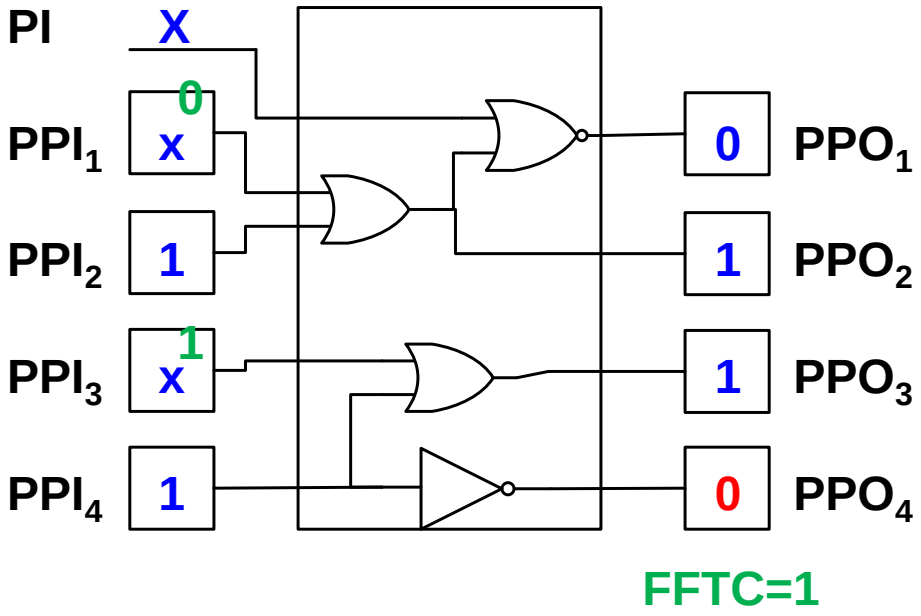
Low-Capture-Power Fill (1/4) [Wen 05]

- Idea: try to minimize FFTC during capture
- Case 1: No x in PPI and PPO
  - FFTC cannot be further improved
  - Just fill PI (maybe to reduce WSA)



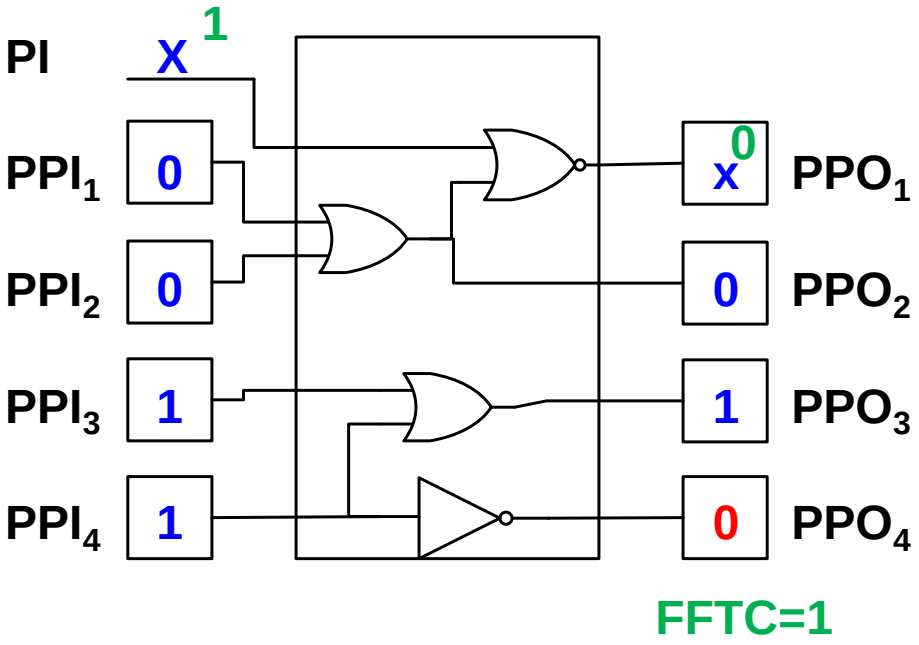
Low-Capture-Power Fill (2/4)

- **Case 2: Some PPI=x, but no PPO=x**
  - **Just assign PPI the same value as PPO**
  - **Example: assign PPI_1=0, PPI_3=1. FFTC=1**



Low-Capture-Power Fill (3/4)

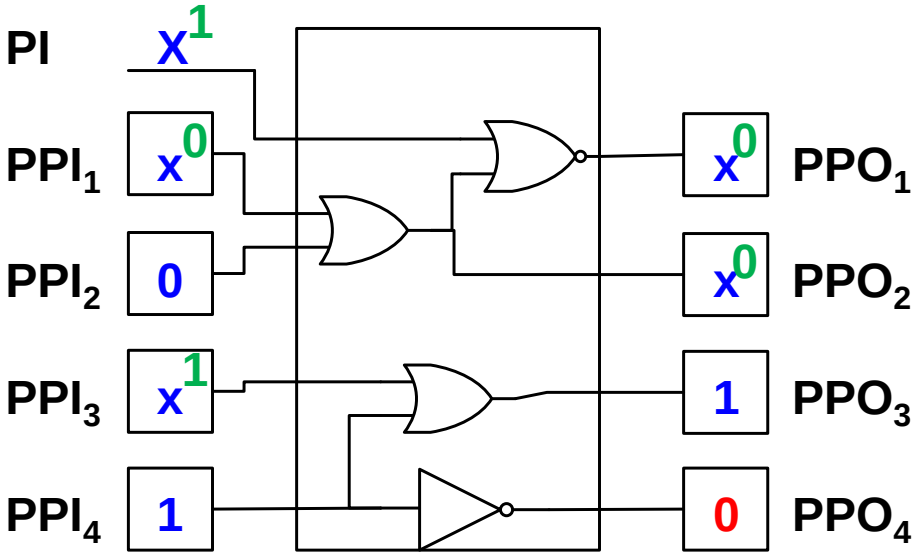
- **Case 3: No PPI=x. But some PI=x.**
  - **Fill PI to justify PPI = PPO**
  - **Example: To justify PPO_1=0, need to assign PI=1. FFTC=1**



- **Criterion #1: When there are multiple PPO=X**
  - **First choose PPO that has most PPI=X in its fan-in cone**

Low-Capture-Power Fill (4/4)

- Case 4: Some PPI=x. Some PPO=x
- Criterion #2:
  - If type-B more than type-C, process type-B first
    - Otherwise, process type-C first
  - After all type-B and C finished, then process type D
- Example: Type-B PPI_3=1. Type-C PPI_1=1.
  - Type-D PPI_1 turns into Type-C. PI=1

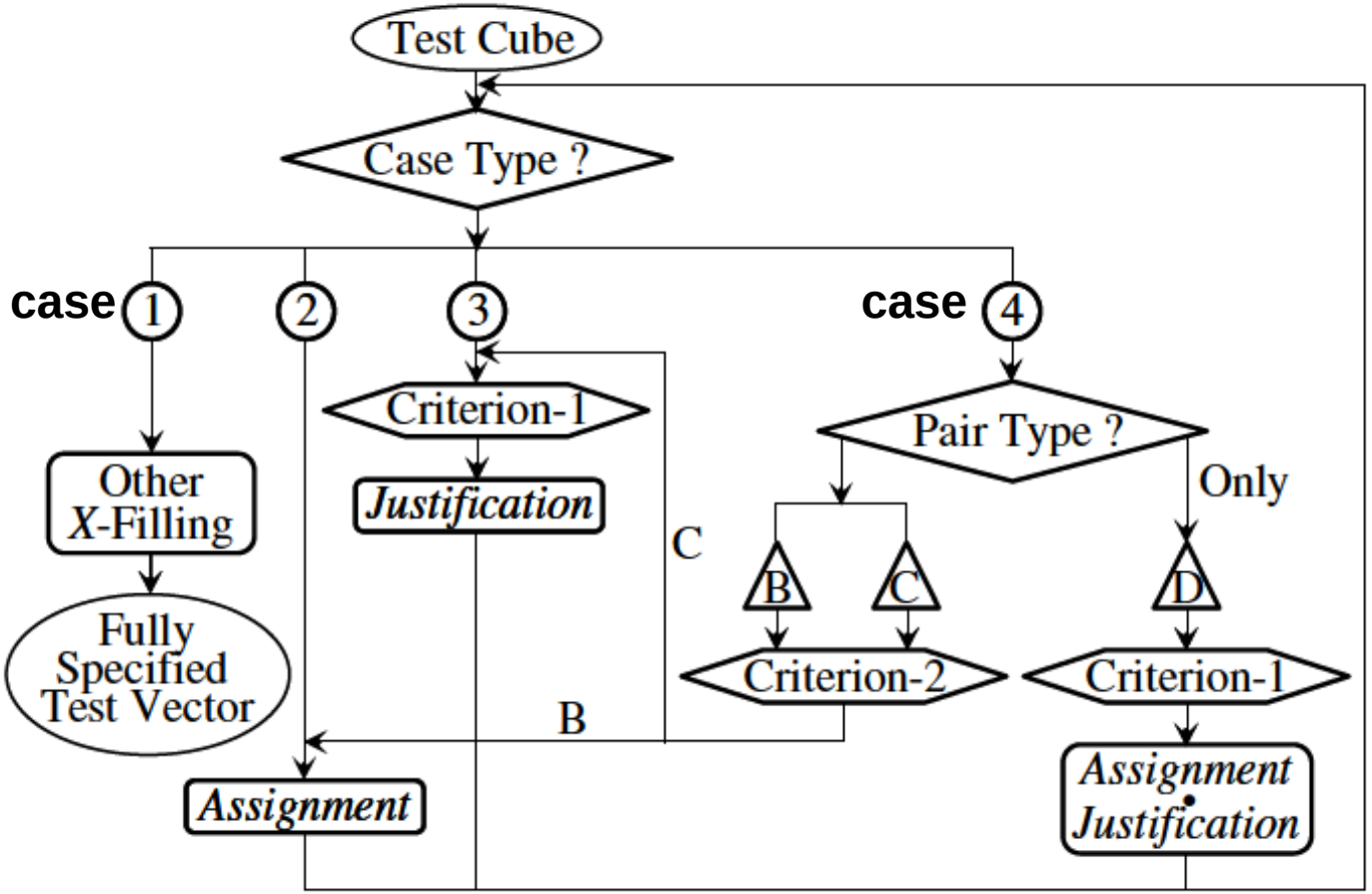


FFTC=1

Bit-pair types

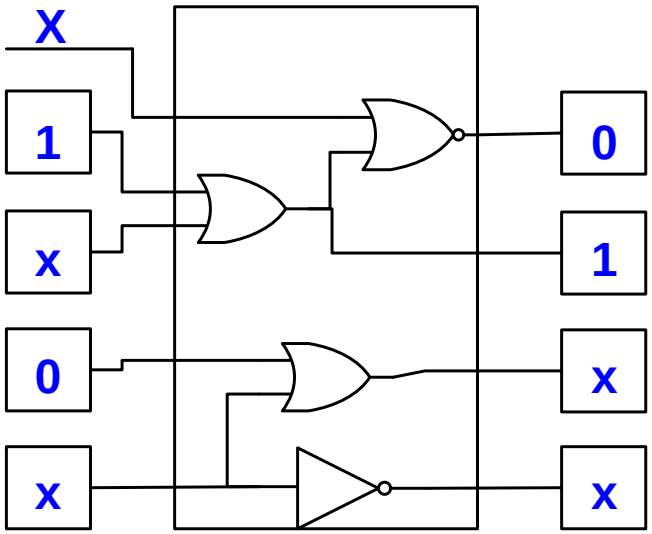
Type	PPI	PPO
A	0,1	0,1
B	X	0,1
C	0,1	X
D	X	X

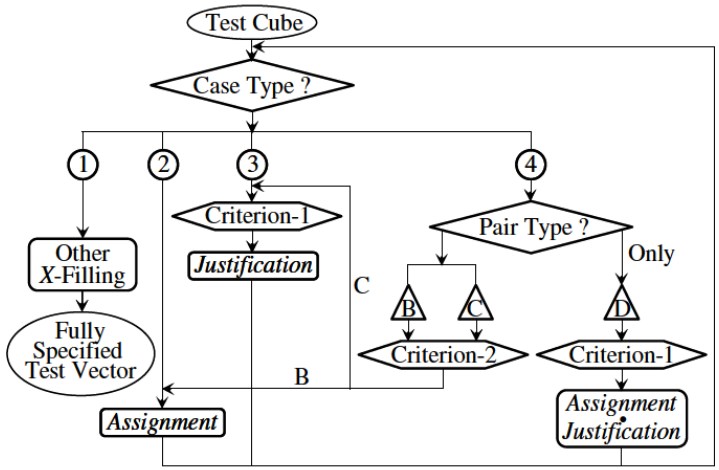
LCP Fill Algorithm [Wen 05]



Quiz

Q: What are types of bit pairs?
Please follow algorithm and fill in PI/PPI to reduce FFTC.
A:





Type	PPI	PPO
A	0,1	0,1
B	X	0,1
C	0,1	X
D	X	X

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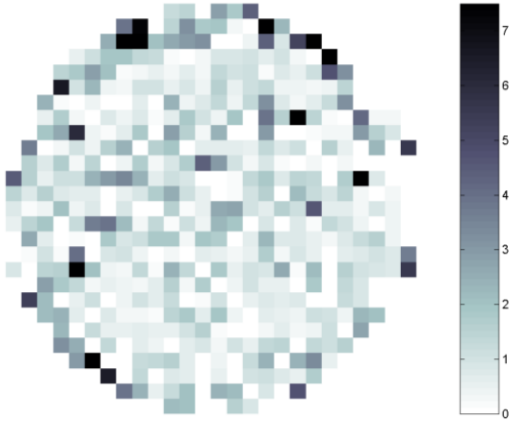
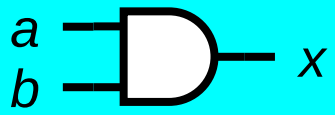
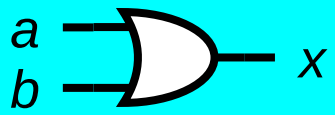
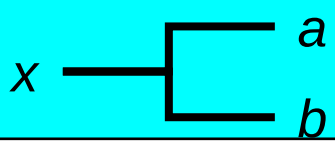


Too Many X bits to Fill. Any Faster Way?

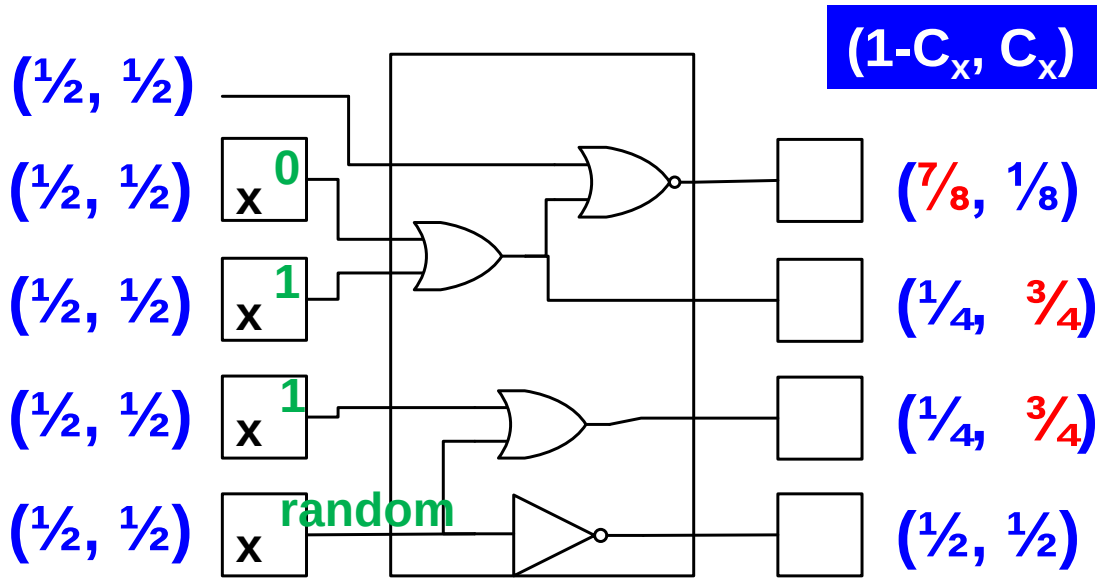
Review: COP (Video 6.3)

- ***Signal probability* of $x = C_x$ =probability of *x* being logic 1**
- **Assume gate inputs are independent**

	C_x
***x* = PI**	***0.5***
	$C_x = C_a \times C_b$
	$C_x = 1 - (1- C_a) \times (1- C_b)$
	$C_x = C_a = C_b$

Preferred Fill [Remersaro 06]

- Idea: Fill in the most likely PPO value to corresponding PPI
- Calculate C_x from input to output
  - Fill PPI=1 if C_x of PPO is larger than ½
    - Otherwise, fill PPI=0



Preferred Fill Very Fast and Scalable

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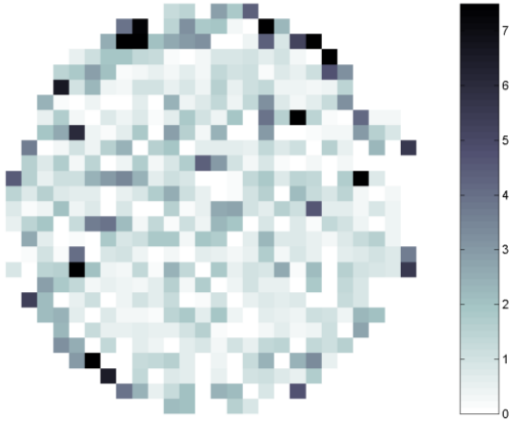


TI Experiments [Saxena 03]

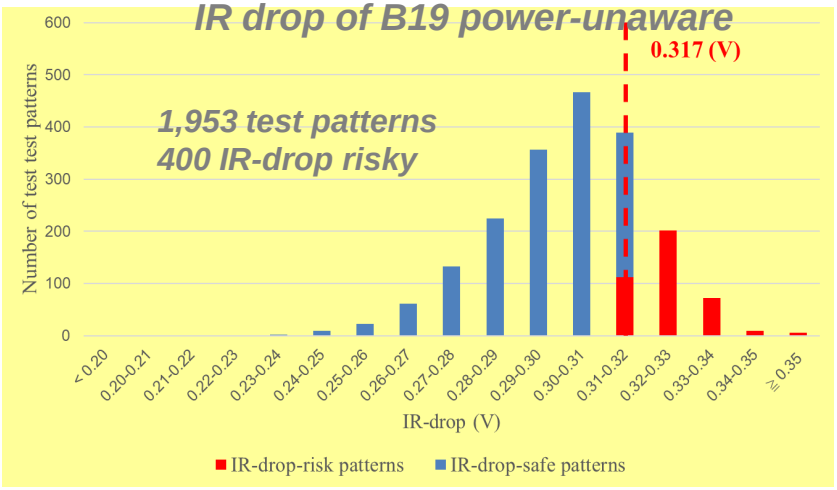
- Different test patterns induce different switching activities
- *Minimum functional V_{DD} (V_{min})* increases with switching activities
- PSN may cause test overkill if we use high SA test patterns

	Pattern name	% Nets Switching	V_{min}	
High SA	quiet0.pat	22.75	1.44 V	
	quiet10.pat	21.90	1.38 V	FAIL V_{min}>1.35V
	quiet20.pat	21.88	1.37 V	
	quiet30.pat	21.35	1.31 V	
	quiet40.pat	18.37	1.32 V	PASS V_{min}<1.35V
	quiet50.pat	15.16	1.31 V	
	quiet60.pat	13.05	1.31 V	
	quiet70.pat	14.52	1.29 V	
	quiet80.pat	10.82	1.27 V	
	quiet90.pat	6.12	1.24 V	
Low SA	quiet100.pat	1.47	1.21 V	

Table 1: A table of V_{min} value versus percentage of switching activity for different test patterns.

Power-aware vs Power-unaware [Liu 21]

- Machine-learning predict IR drop
- 45nm, Nominal V_{DD}=0.9V
- Commercial ATPG
  - Power-unaware ATPG
    - 20% IR-drop larger than 0.317V
  - Power-aware ATPG
    - Reduce FFTC 10%
    - 6.27% longer test length, 47% longer run time



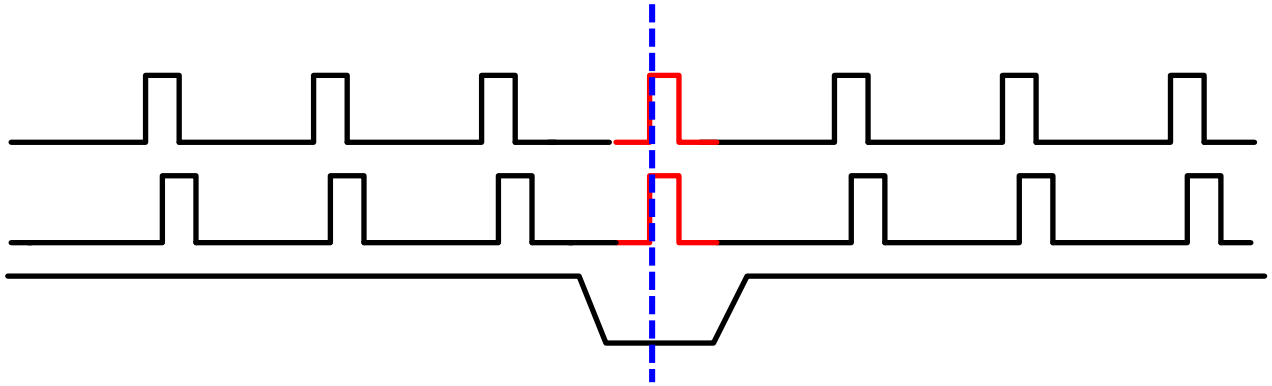
Circuit	Test Length		Fault Coverage		Runtime (min)	
	Power-unware	power-aware	Power-unware	power-aware	Power-unware	power-aware
b19	1,953	2,056	98.82%	98.40%	8.68	10.80
MEMC	187	314	92.92%	92.85%	0.50	0.80
leon3mp	3,558	3,684	96.36%	95.49%	11.00	18.11
Average	1,899	2,018 (+6.27%)	96.03%	95.58% (-0.45%)	6.73	9.90 (+47%)

Summary

- Test power much larger than functional power
  - Test overkill or reduce reliability
- DfT solutions
  - Clock staggering, clock gating, clock partition
  - Effective but area/design overhead
- ATPG solutions (use FFTC and WSA as metrics)
  - Shift power : Adjacent fill
  - Capture power :
    - LCP-fill: four cases
    - Preferred-fill: signal probability (scalable)
- Advantage of Pa-ATPG
  - ☺ Avoid test overkill
- Disadvantages of Pa-ATPG
  - ☹ Test length inflation ☹ Run time overhead

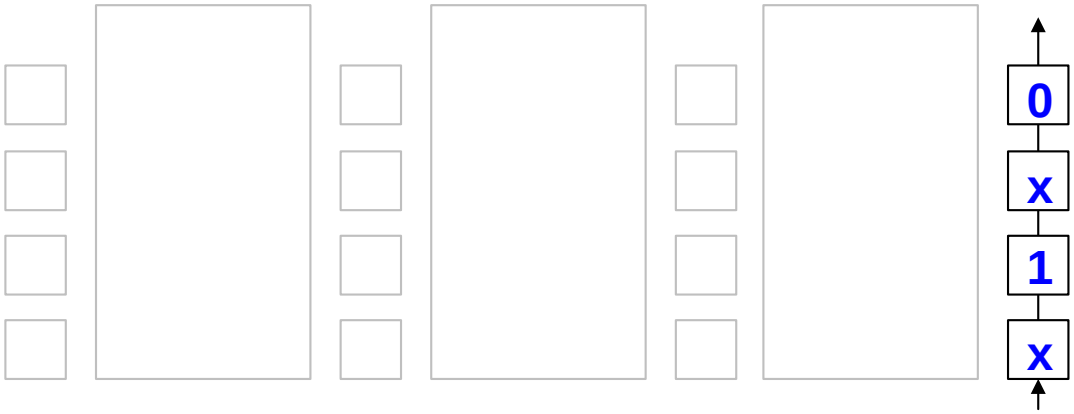
FFT

- **Q1: *Test Clock Staggering* reduces shift power only.**
  - **Why do not we stagger capture clock to reduce capture power too?**



FFT

- **Adjacent fill easily reduce shift in power**
  - **Q: how about shift out power?**



References

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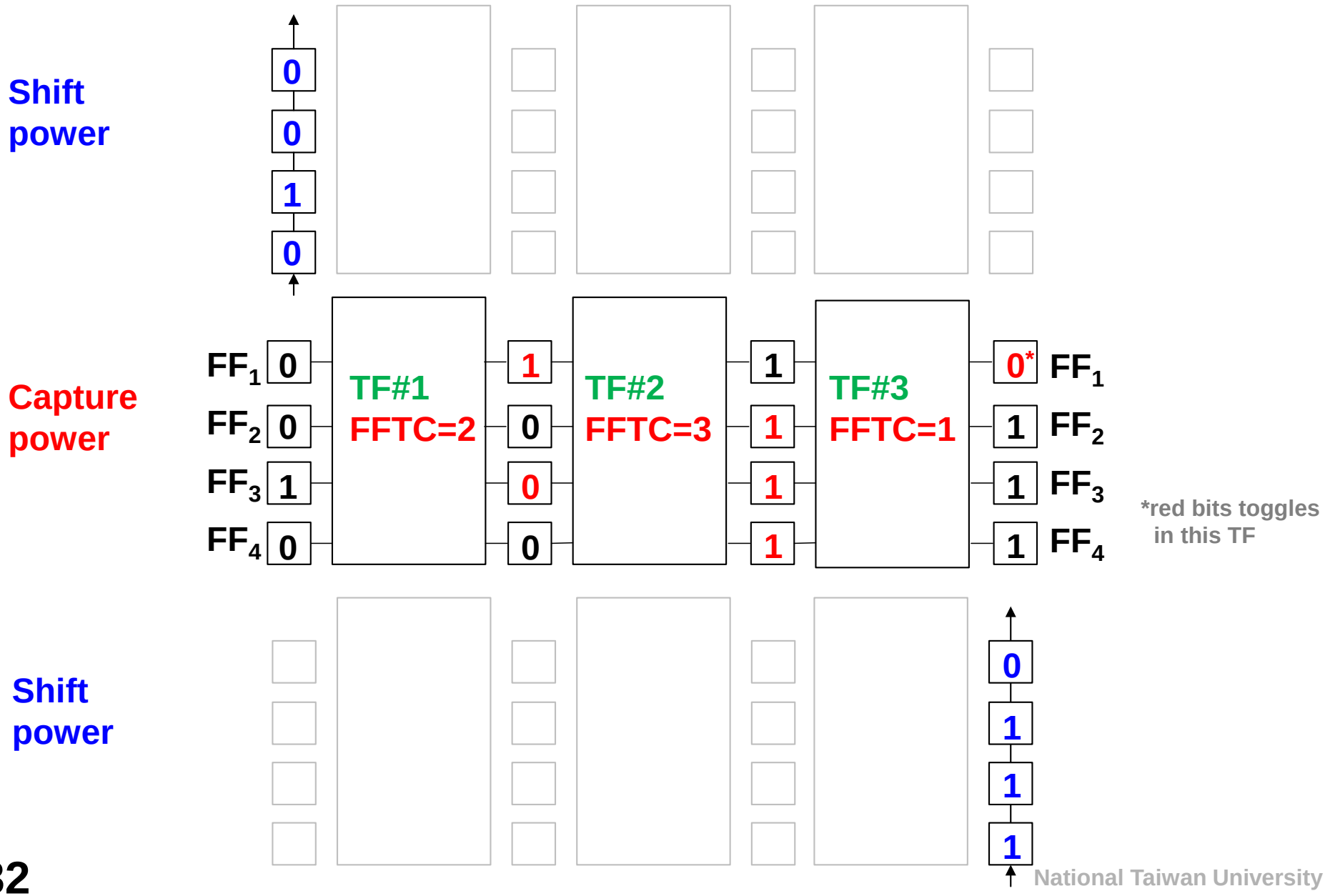
Time Frame Expansion Model



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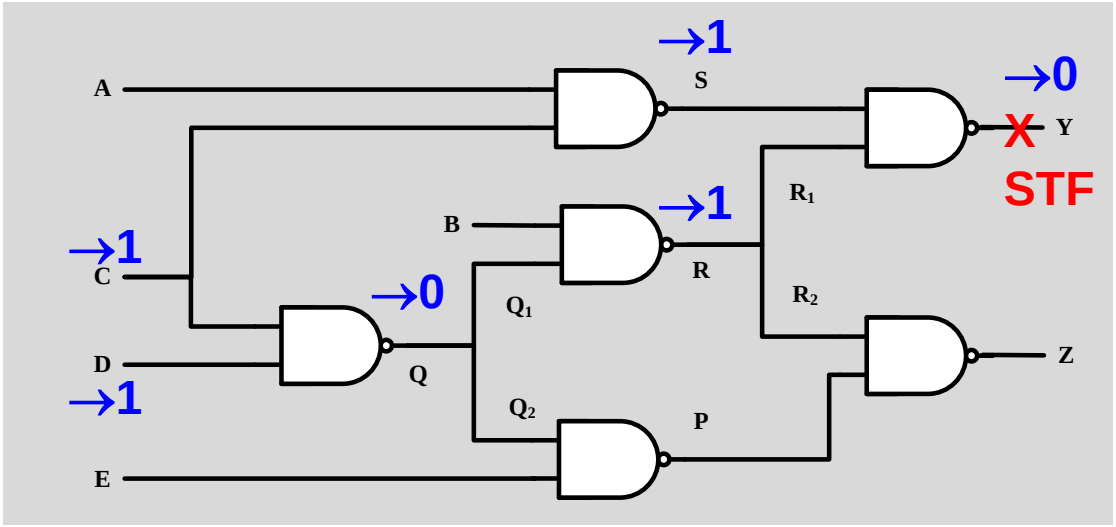
② Generate Test Pattern

- Target fault : Y STF
- V_2:
  - detect Y stuck-at one



- V_1:
  - Y falling transition
  - Backtrace long path