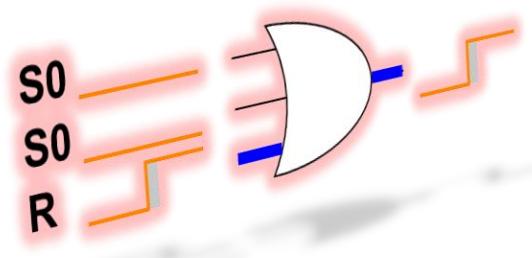


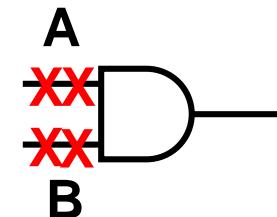
Delay Test

- Introduction and delay fault models
- Path Delay Fault
- **Transition Delay Fault**
 - ♦ Fault Simulation
 - ♦ Test Generation
- Experimental Results* (not in exam)
- Issues of Delay Tests* (not in exam)
- Conclusions



TDF Detection

- How to detect A STR fault ?
 - ◆ V_1 : Control A to **0**
 - ◆ V_2 : Detect A **stuck-at 0**
- How to detect A STF fault ?
 - ◆ V_1 : Control A to **1**
 - ◆ V_2 : Detect A **stuck-at 1**
- TDF assumes delay fault size very large
 - ◆ **No requirement** about propagation path

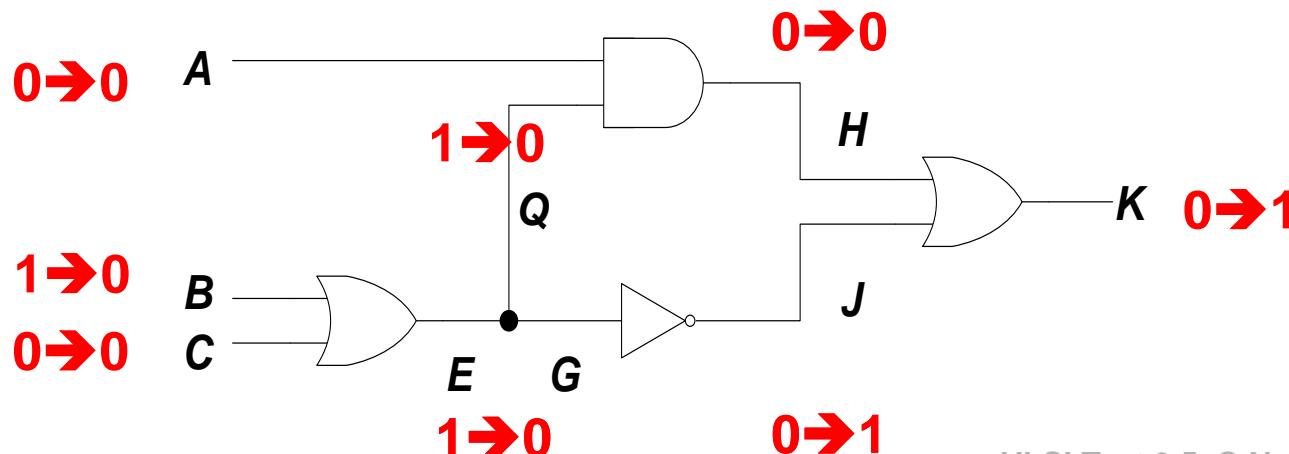


V_1 AB	V_2 AB	Detected input TDF
0X	11	A STR
1X	01	A STF
X0	11	B STR
X1	10	B STF

TDF Very Similar to SSF

TDF Fault Simulation

- Transition delay fault simulation can be built on SSF simulation
 - ◆ Just add additional check for V_1
 - ◆ V_2 is same as SSF simulation
- Example: V_1 $ABC = 010$, V_2 $ABC = 000$
 - ◆ V_2 detects B SA1, C SA1, E SA1, G SA1, J SA0, K SA0
 - ◆ $\{V_1, V_2\}$ Detected transition faults
 - * B STF, E STF, G STF, J STR, K STR
 - * C STF not detected because no transition
 - * Q STF not detected because Q SA1 not detected by V_2



Quiz

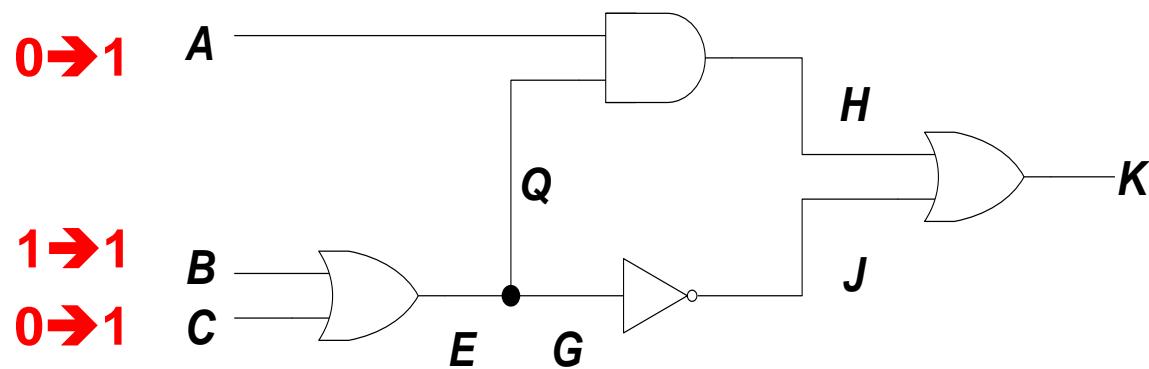
Q: Given this 2-patter test, which transition faults are detected?

V_1 ABC= 010

V_2 ABC= 111

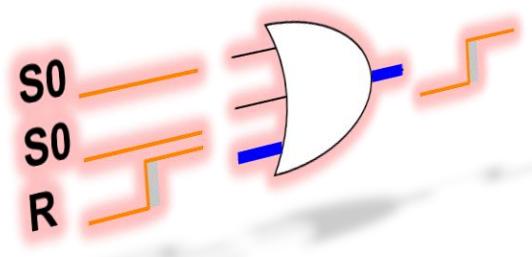
considers A STR, H STR, C STR faults

A:



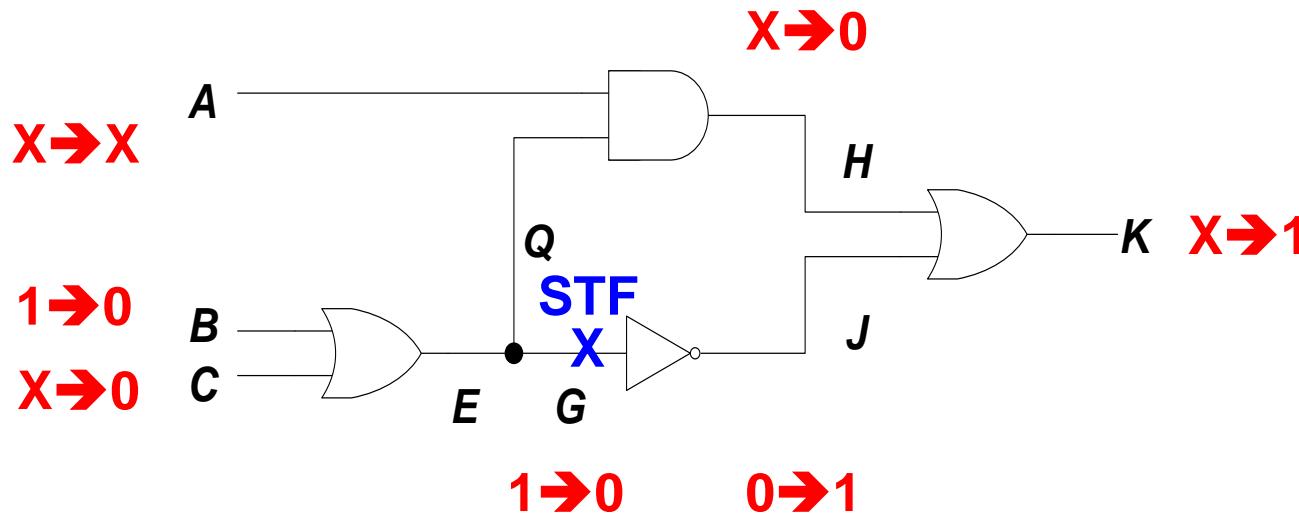
Delay Test

- Introduction and delay fault models
- Path Delay Fault
- **Transition Delay Fault**
 - ◆ **Fault Simulation**
 - ◆ **Test Generation**
- Delay Test Application
- Circuit Model for Delay Test ATPG
- Experimental Results* (not in exam)
- Issues of Delay Tests* (not in exam)
- Conclusions



TDF ATPG

- First SSF for V_2 , then control V_1
- Example: use PODEM for *G slow-to-fall (STF) fault*
 - ◆ V_2 objective: detect G stuck-at 1 $\rightarrow B_2=0$
 - ◆ V_2 objective: detect G stuck-at 1 $\rightarrow C_2=0$, V_2 generated
 - ◆ V_1 objective: $G = 1 \rightarrow B_1=1$
 - ◆ Test generated: V_1 $ABC = X1X$, V_2 $ABC = X00$



Generate V_2 , then V_1

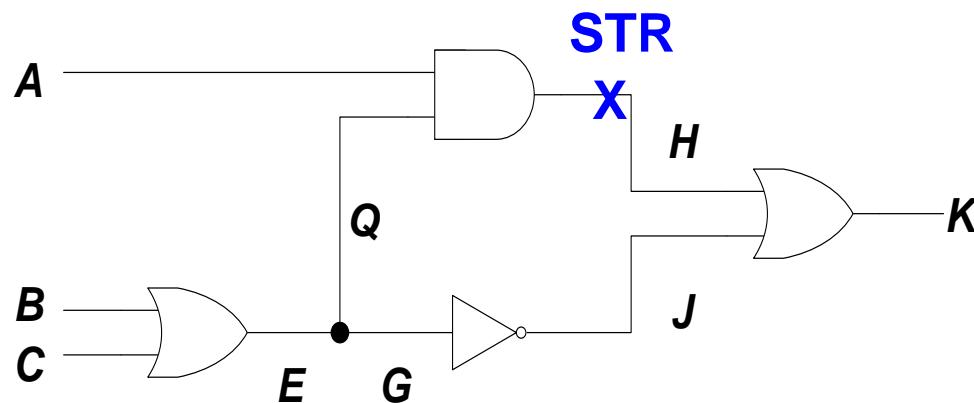
Quiz

Q: Generate a test for H STR fault

A:

$V_1 \text{ ABC} =$

$V_2 \text{ ABC} =$

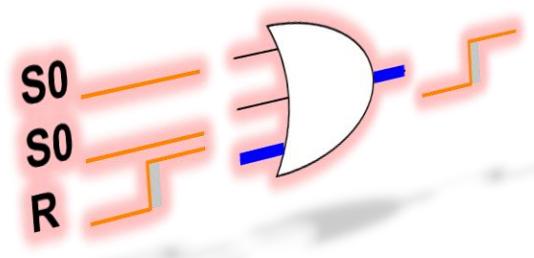


Pros and Cons of TDF

- Advantages:
 - + Leverage on mature SSF ATPG algorithm
 - + High coverage
 - + ATPG easy because no attention to path
- Disadvantages
 - SSF ATPG tends to trace short paths
 - ◊ may not effective for small delay defect (SDD)
- TDF test patterns currently “most basic” delay testing

Summary

- Transition Delay Fault
 - ◆ Fault Simulation
 - * Based on SSF fault simulation, check V_1
 - ◆ Test Generation
 - * Generate SSF for V_2
 - * Then control opposite value at V_1



FFT

- Q: why generate V_2 first, then V_1 . (why not V_1 first, then V_2)
- Example: use PODEM for G slow-to-fall (STF) fault
 - ◆ V_2 objective: detect G stuck-at 1 $\rightarrow B_2=0$
 - ◆ V_2 objective: detect G stuck-at 1 $\rightarrow C_2=0$, V_2 generated
 - ◆ V_1 objective: $G = 1 \rightarrow B_1=1$
 - ◆ Test generated: V_1 $ABC = X1X$, V_2 $ABC = X00$

