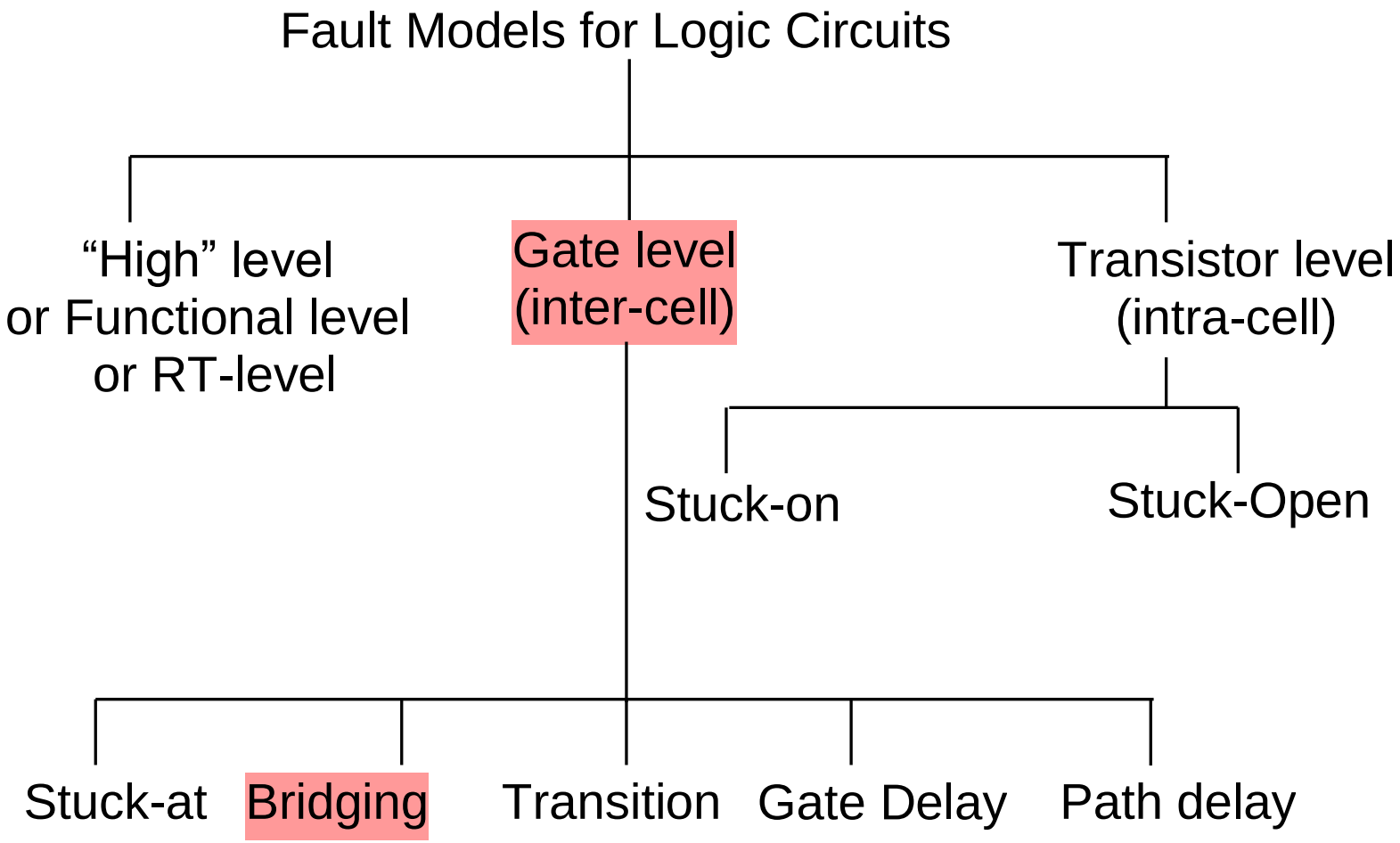
Fault Modeling

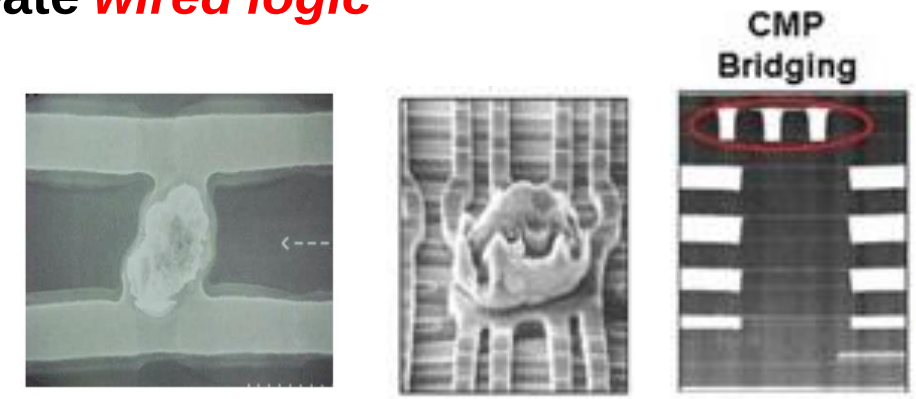
- Introduction
- **Fault Models**
  - Stuck-at fault (1961)
  - **Bridging fault (1973)**
  - Delay fault (1974)
  - Transistor level fault
- Fault Detection
- Fault Coverage
- Conclusion

Classification of Fault Models



Bridging Faults (BF) [Williams 73][Friedman 74]

- **Definition:**
  - **Two (or more) distinct logic signals unintended shorted together and create *wired logic***



CMP= Chemical Mechanical Polishing
Picture source: Mentor graphics

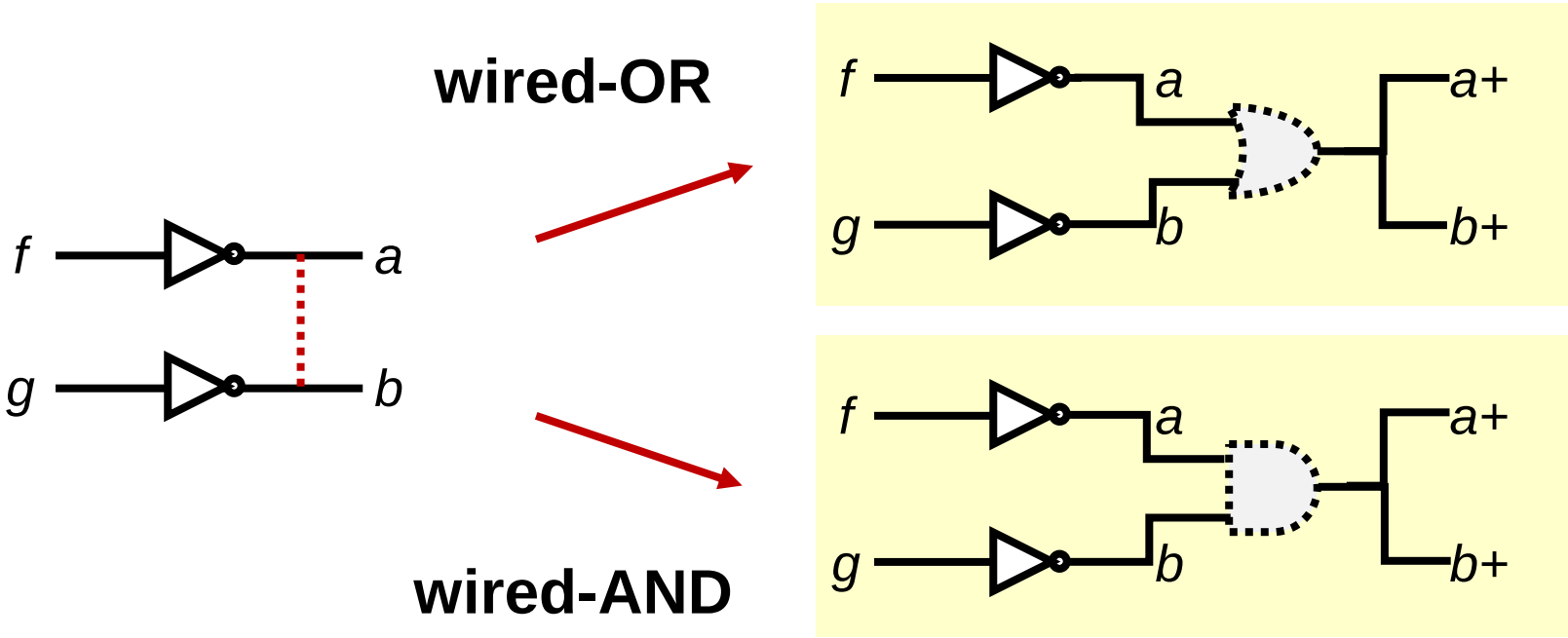
- **Q: How many two-way BF in a circuit of *n* signals?**
  - **Arbitrary choose two signals: $C^n_2 = O(n^2)$. too many!**
  - **Need to identify pairs of neighbor signals from layout**
    - ***Fault extraction***

Number of Bridging Faults is $O(n^2)$

Bridging Fault Models

- **Popular models for CMOS**
  - ***Wired-OR* (1-dominant)**
  - ***Wired-AND* (0-dominant)**
  - ***A-dominant***

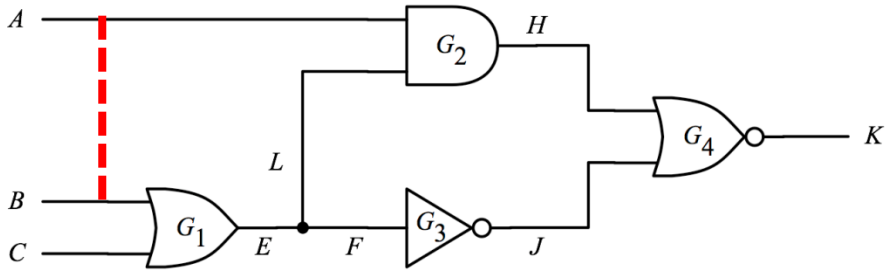
original a b	Wired-OR a^+ b^+	Wired-AND a^+ b^+	a-dominant a^+ b^+
0 0	0 0	0 0	0 0
0 1	**1** 1	0 **0**	0 **0**
1 0	1 **1**	**0** 0	1 **1**
1 1	1 1	1 1	1 1



Wired Logic Is Imaginary, not Real

Different Models Need Different Patterns

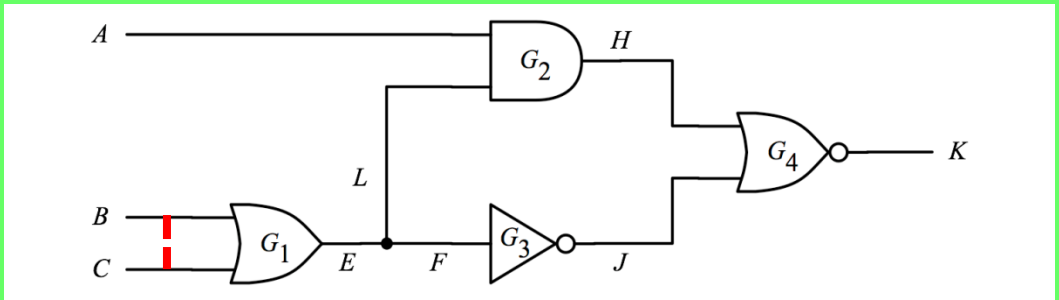
- **Consider (A, B) bridging fault**
  - **Wired-AND, Wired-OR detected by 011, or 010**
  - **A-dominant model detected only by 010**



Inputs A B C	Fault-free Output	Wired-OR	Wired-AND	A-dominant
0 0 0	0	0	0	0
0 0 1	1	1	1	1
0 1 0	1	**0**	**0**	**0**
0 1 1	1	**0**	**0**	1
1 0 0	0	0	0	0
1 0 1	0	0	0	0
1 1 0	0	0	0	0
1 1 1	0	0	0	0

Quiz

Q1: Fill in table with (B,C) bridging fault.
Q2: Which test pattern detects wired-OR fault?



Inputs A B C	Fault-free Output	Wired-OR	Wired-AND	B-dominant
0 0 0	0	0	0	0
0 0 1	1			
0 1 0	1			
0 1 1	1			
1 0 0	0			
1 0 1	0			
1 1 0	0			
1 1 1	0			

SSF Test Sets Not Good Enough

- How effective is SSF test sets for bridging faults? [Millman 88]
  - 74LS181 ALU, 100% fault coverage SSF test sets
    - Total 7,981 testable bridging faults

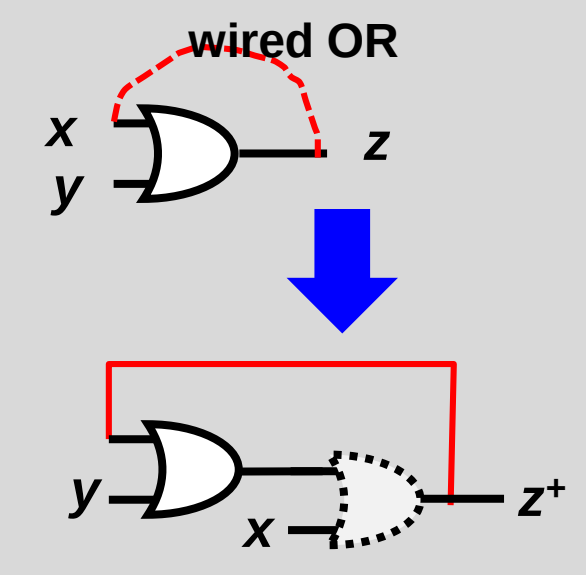
Test set	Bry2	Bry6	Goel	Hugh	Krish	McC4	Micz2
Test Length	14	12	35	135	12	124	17
# of missed BF	111	138	15	2	171	13	85
missed BF %	1.39	1.73	0.19	0.03	2.14	0.16	1.07

Some BF not Detected by SSF Test Sets

Feedback Bridging Faults

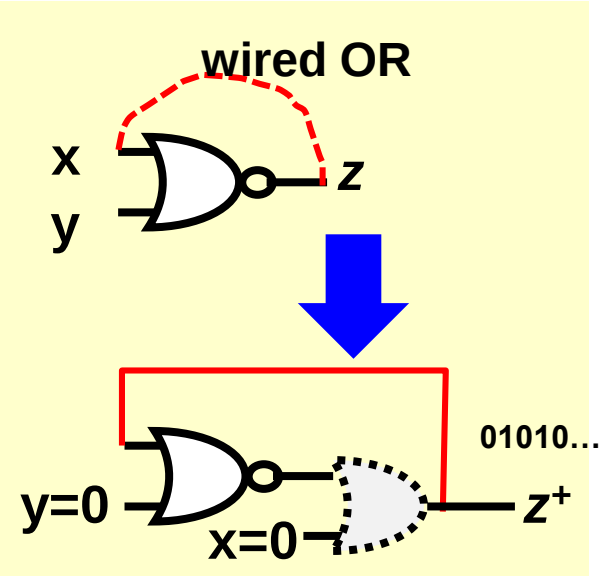
- **Type1: creates memory**
  - **Detected by *test sequence* 01→00**

Inputs x y	Fault-free Output	Faulty Output
0 0	0	unchanged
0 1	1	1
1 0	1	1
1 1	1	1



- **Type2: creates oscillation**
  - **"hard" detected by 10, or 11**
  - **"potentially" detected by 00**

Inputs x y	Fault-free Output	Faulty Output
0 0	1	oscillation
0 1	0	0
1 0	0	1
1 1	0	1

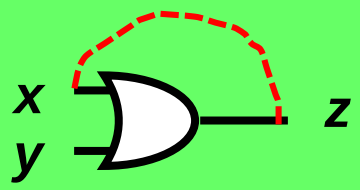


Quiz

Q1: Fill in table with a Wired-AND feedback BF (x, z)

A:

Inputs x y	Fault-free Output	Faulty Output
0 0	0	
0 1	1	
1 0	1	
1 1	1	



Q2: Find a test to detect this feedback BF

A:

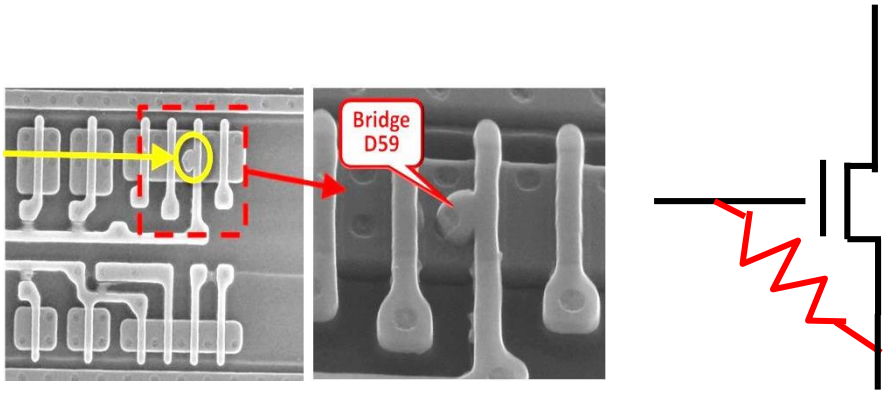
What are NOT Bridging Fault?

① BF does NOT consider shorts to power and ground

② BF does NOT consider defect resistance value

③ BF does NOT consider *Intra-cell* (intra-gate) defects

- BF is *gate-level*, NOT *transistor-level* fault model



Intra-gate bridging defect
[Mentor graphics]

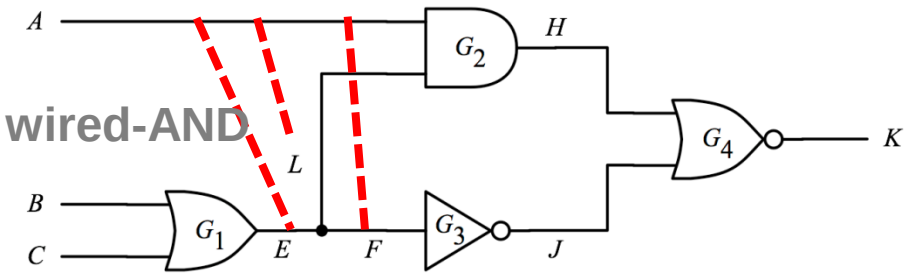
④ BF does NOT distinguish between fanout stem and branches

⑤ BF is NOT transient fault

(4, 5 see next slides)

Fanout Stem and Branches

- SSF on fanout stem and branches are different (see 3.2)
- BF on fanout stem and branches are the same
- Example: wired-AND model
  - $(A,E) = (A,L) = (A,F)$
  - Why? FFT

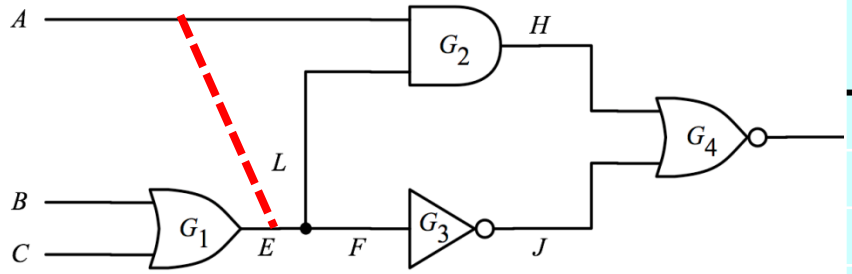


Inputs A B C	Fault-free Output	BF (A,E)	BF (A,L)	BF (A,F)
0 0 0	0	0	0	0
0 0 1	1	**0**	**0**	**0**
0 1 0	1	**0**	**0**	**0**
0 1 1	1	**0**	**0**	**0**
1 0 0	0	0	0	0
1 0 1	0	0	0	0
1 1 0	0	0	0	0
1 1 1	0	0	0	0

BF on Stem and Branches Are Same

Permanent Faults vs. Transient Faults

- ***Permanent faults*: faults always present**
  - **caused by defects**
  - ***e.g.* bridging faults caused by particle defects**
- ***Transient faults*: faults not always present**
  - **induced by environmental (EMI) or internal (IR drop...) disturbance**
  - ***e.g.* crosstalk faults caused by coupling effect**



Inputs A B C	Fault-free Output	per-manent	tran-sient
0 0 0	0	0	0
0 0 1	1	**0**	**0 or 1**
0 1 0	1	**0**	**0 or 1**
0 1 1	1	**0**	**0 or 1**
1 0 0	0	0	0
1 0 1	0	0	0
1 1 0	0	0	0
1 1 1	0	0	0

Summary

- Bridging fault models for CMOS
  - Wired-OR, wired-AND, A-dominant
- Number of bridging faults is O(n^2). too many!
  - Needs fault extraction from layout
- SSF test set may not good enough to detect all BF
  - Feedback BF may cause memory or oscillation
- BF model does NOT distinguish fanout stem and branches
- BF is permanent fault ; crosstalk fault is transient fault

FFT

- **BF does *NOT* distinguish fanout stem and branches**
  - $(A,E) = (A,L) = (A,F)$
- **FFT: BF is unlike SSF, why?**
  - E **SA1** $\neq$ F **SA1** $\neq$ L **SA1 (see 3.2)**