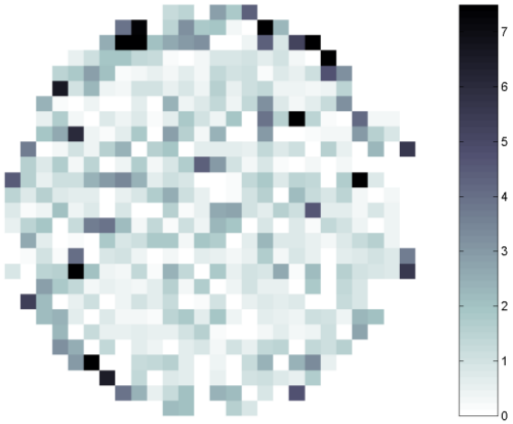
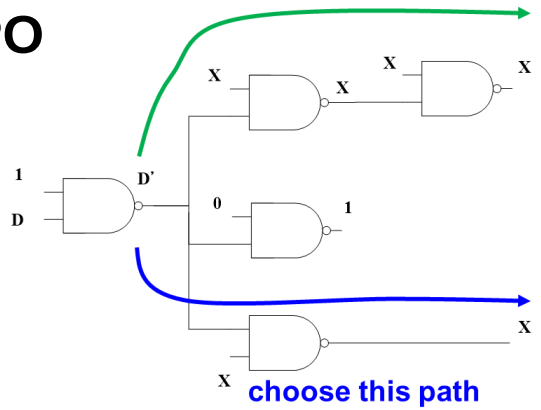
Advanced Topics: ATPG

- Introduction
- Defect-based Testing
- **Advanced ATPG**
  - N-detect ATPG (Stanford 1995)
  - Cell-aware ATPG (Mentor 2009)
  - **Timing-aware ATPG (Mentor 2006)**
    - **Introduction**
    - **ATPG algorithm**
    - **Experimental Results**
  - Power-aware ATPG (KIT 2005)
- Conclusion



ATPG Choose Short Path

- **Review: PODEM chose shortest X-path to PO**
  - **(Video 7.5)**



- **Stanford Murphy Experiment [Tseng 01]**
  - **Some outputs do not fail on tester**
  - **Shorter path can result in test escape**

Table 6: Failing Output Bits for Chip 2

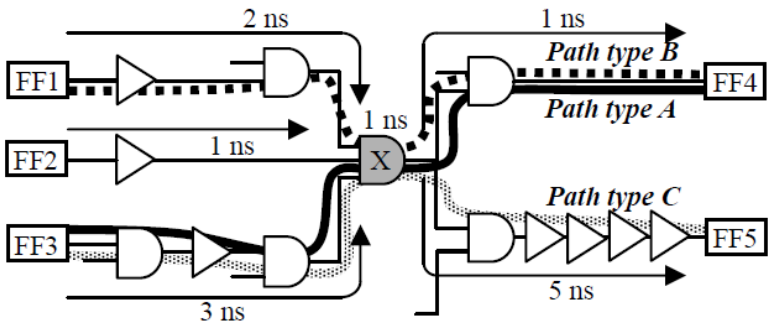
Test Set	Failing Output Bits	
	Simu-lation	Tester
SSF Tool 2A, 1-detect	1,2,3,9	9
SSF Tool 2A, 2-detect	1,2,5,8	5
SSF Tool 3C, 1-detect	2,8	
Tool 4C, 1-detect	1,5,9	5,9
Transition	1,2,5,9	5,9

Table 7: Failing Output Bits for Chip 5

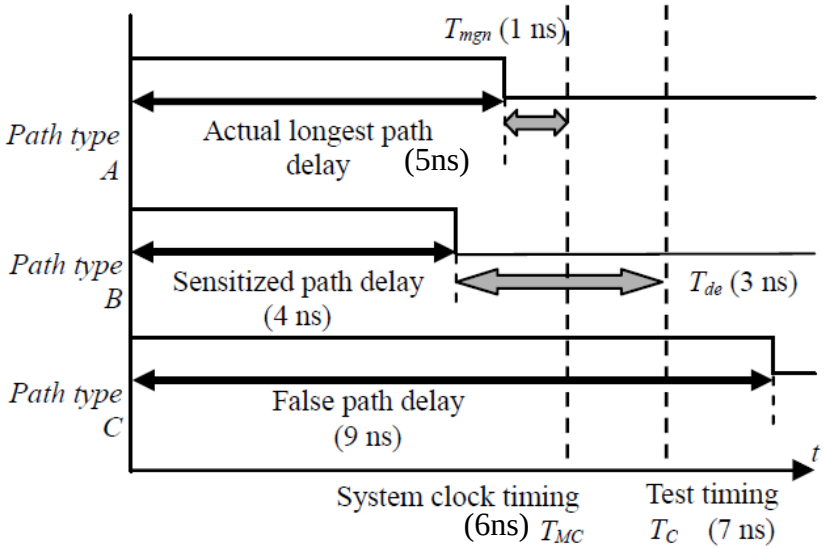
Test Set	Failing Output Bits	
	Simu-lation	Tester
SSF Tool 2A, 1-detect	1,2,3,9	1,9
SSF Tool2A, 2-detect	1,2,5,8	1
SSF Tool 3C, 1-detect	2,8	
Tool 4C, 1-detect	1,5,9	1
Transition	1,2,5,9	1,9

Short Paths are Fast
But Not Good Quality

Three Types of Paths and Clock Timing



Three types of paths through a fault.



Timing relations for the three types of paths.

Actual longest path = Sensitizable longest path in this design.
Sensitized path is activated and propagated by a test pattern.
False paths do not need testing because NOT sensitizable, or Functionally useless

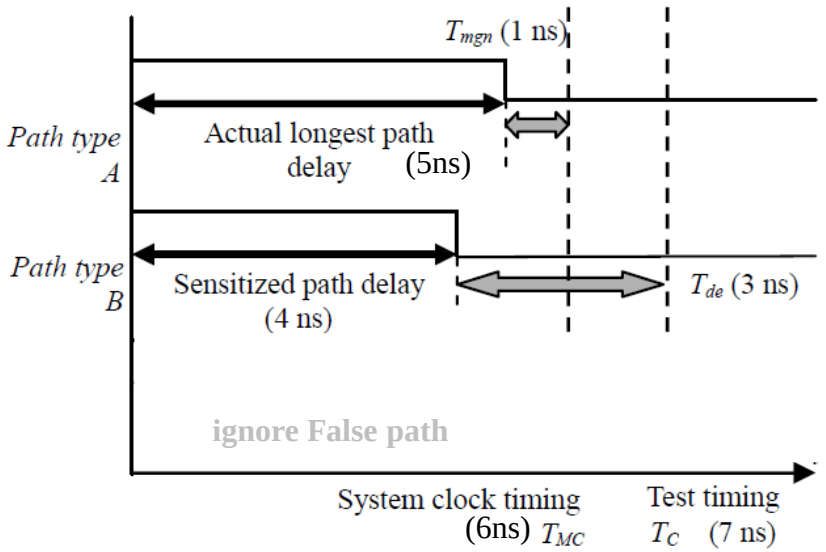
T_{MC} = system clock timing, limited by actual longest path. Used in functional operation.
T_C = test clock timing, limited by tester.
Typically, $T_{MC} \leq T_{TC}$

T_{mgn} = difference between actual longest path and system clock.
T_{de} = difference between sensitized path and test clock.

Good Test Sensitizes Long Paths but Not False Paths

Small Delay Defects (SDD) [Park 92][Sato 05]

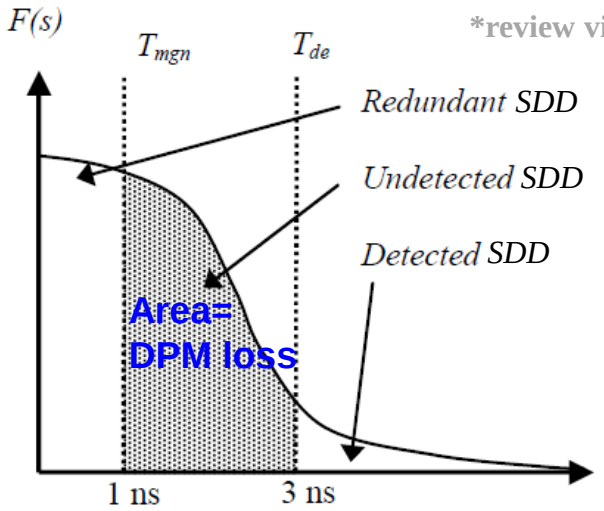
- SDD = small delay defects *NOT* easily detected by slow tests
- Two solutions to reduce SDD
  - 1) Smaller T_{de}: *at-speed testing* $T_{MC}=T_C$ (or faster than at-speed test $T_{MC} > T_C$)
  - 2) Longer sensitized path: *Timing-aware ATPG*



Timing relations for the three types of paths.

defect size *(s)* and density *F(s)* distribution*

*review video 1.3



additional delay defect size (ns)

Timing-aware ATPG Improves DPM

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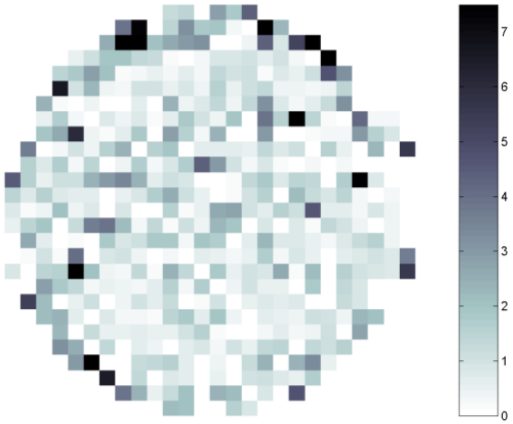
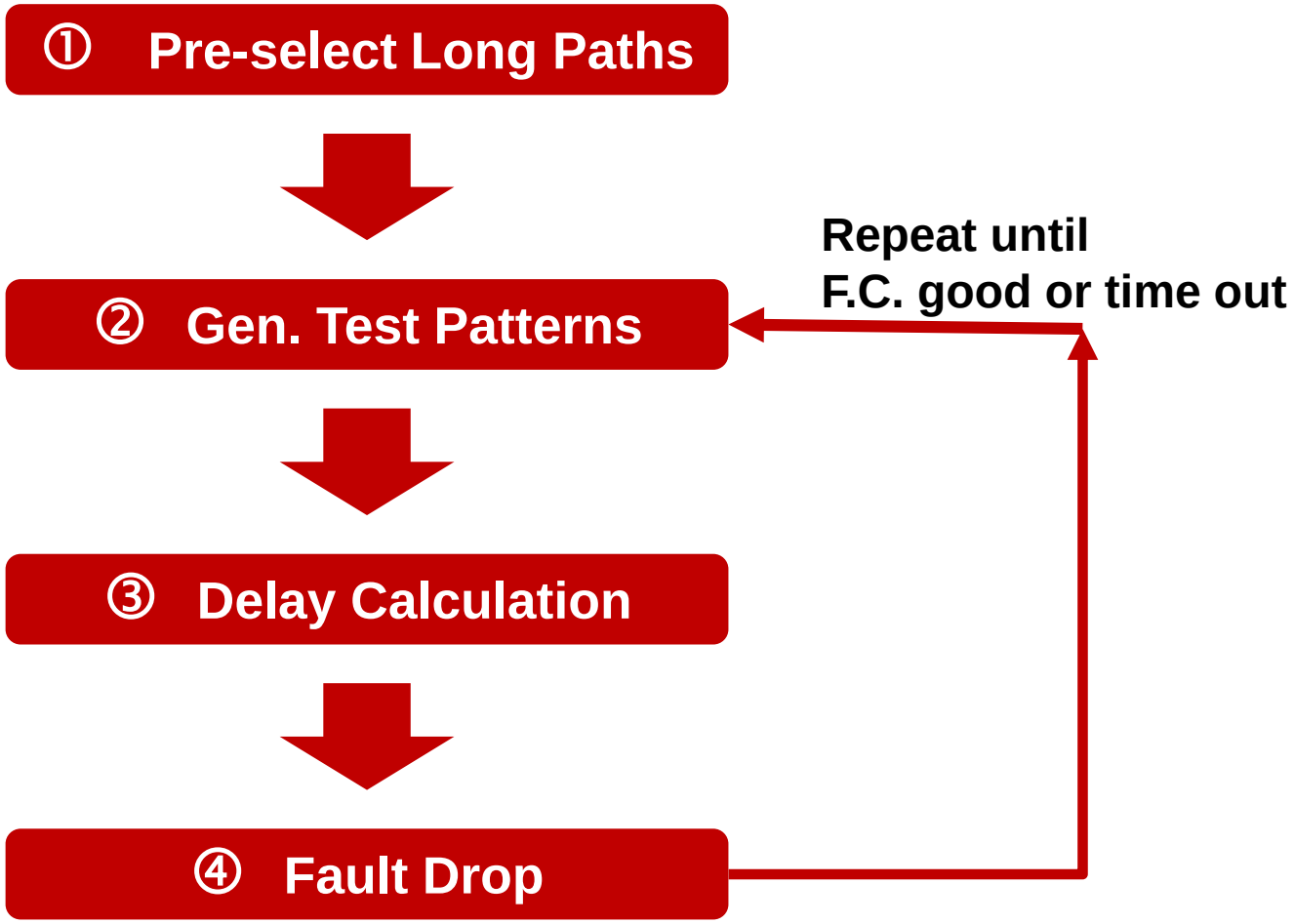


Timing-Aware ATPG* [Mentor/Lin 06]

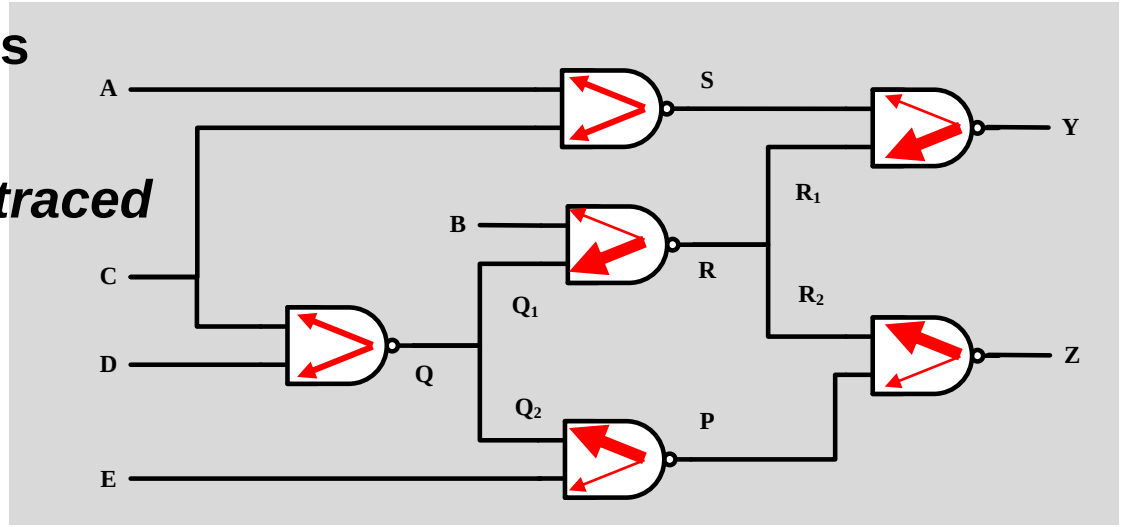


* Lin's work use TDF (transition delay fault)

Other Ta-ATPG:
ALAPTF [Gupta 04]
KLPG [Qiu 04]
Select long paths [Sharma 02][Ahmed 06]
…

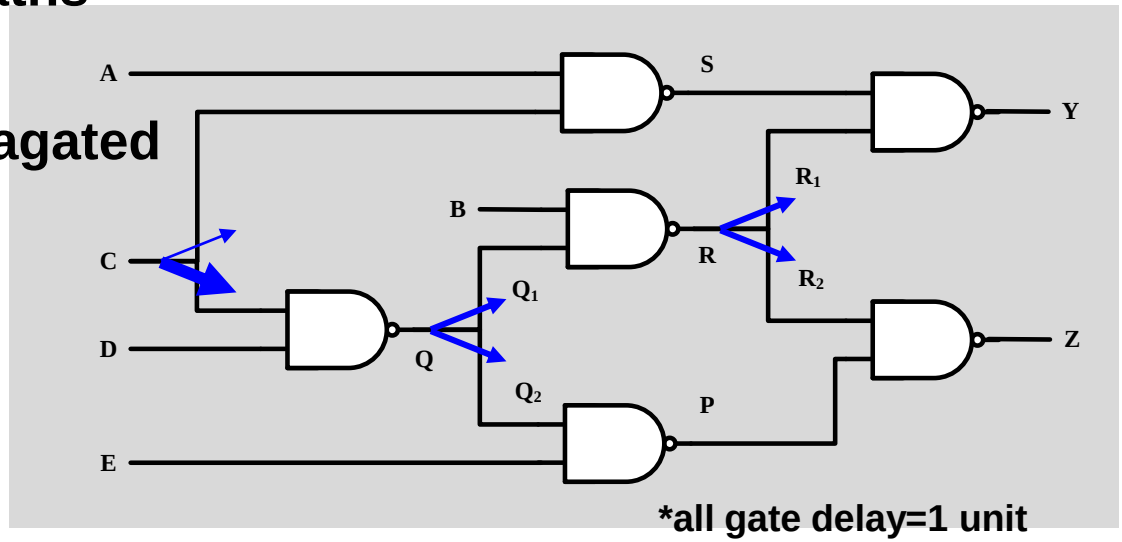
① Pre-select Act./Prop. Paths

- Pre-select **activation** paths
  - ***Static*** **longer paths**
  - **More likely to be *backtraced***



- Pre-select **propagation** paths
  - ***Static*** **longer paths**
  - **More likely to be propagated**

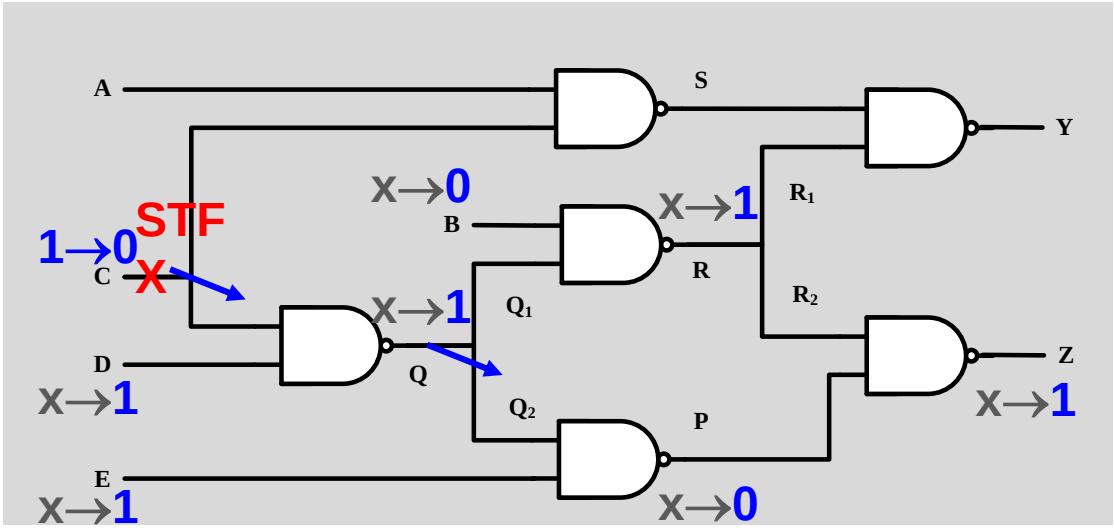
- **Static long paths**
  - **determined by STA**



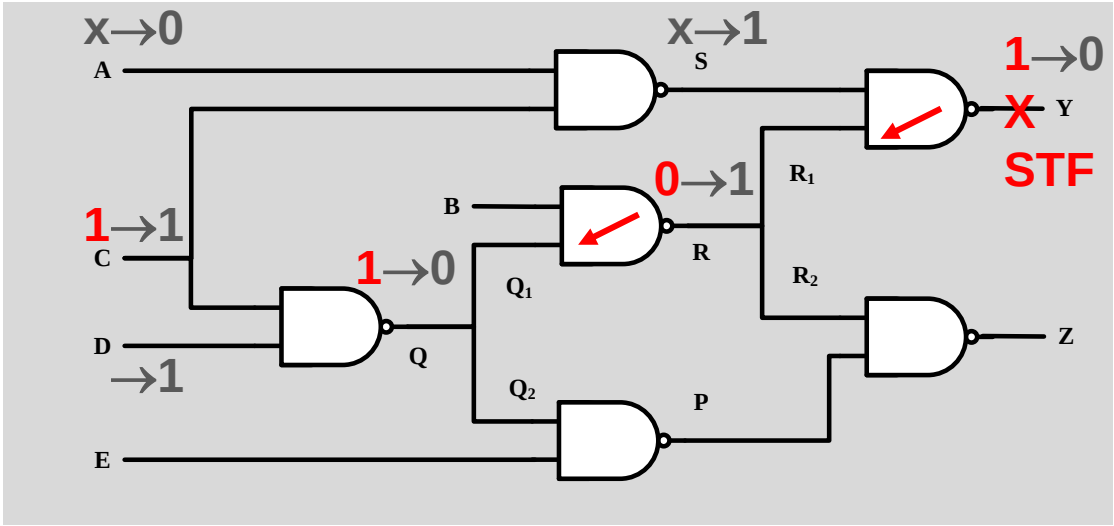
***all gate delay=1 unit**

② Generate Test Patterns

- Example 1: C STF
  - Long path propagated



- Example 2: Y STF
  - Long path activated

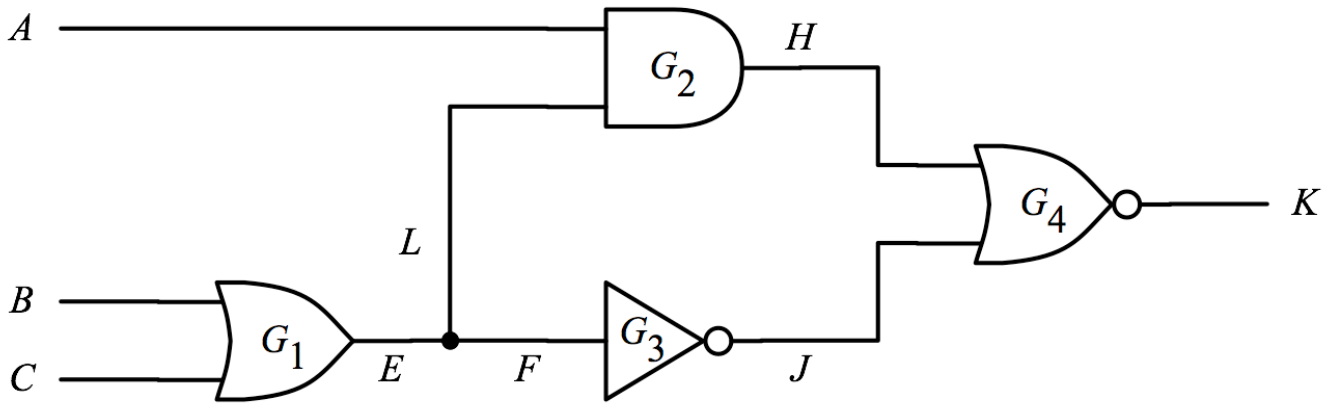


Quiz

Q: Suppose inverter delay is 1 and the other gate delays are 2. Generate timing-aware test pattern for *H slow-to-rise* fault.

A:

	A	B	C	E	H	J	K
V1							
V2							



③ Delay Calculation, AT

- *Arrival Time* AT_x= time to launch transition from PI/PPI to node *x*
- Calculate AT from input to output. Assign input transition AT_{PI} =0
  - If gate output *x* changes from controlled to non-controlled

$$AT_x = \max_{i \in I_{cn}}(AT_i + d_i)$$

I_{nc} = gate inputs from controlling to non-controlling

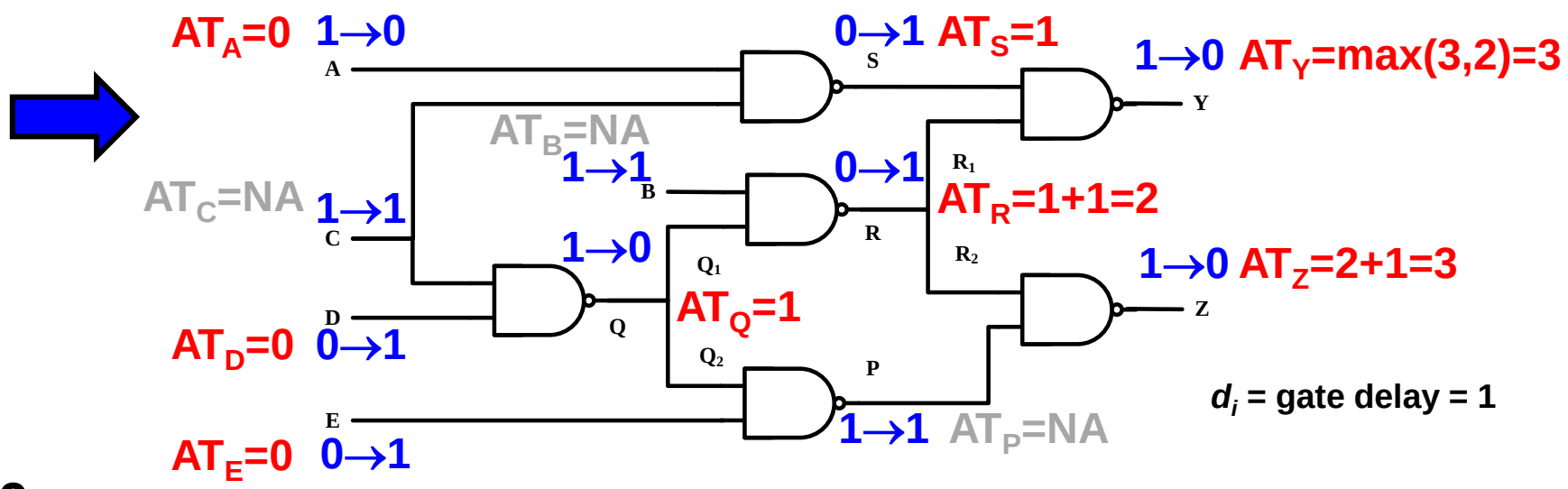
  - If gate output *x* changes from non-controlled to controlled

$$AT_x = \min_{i \in I_{nc}}(AT_i + d_i)$$

I_{nc} = gate inputs from non-controlling to controlling

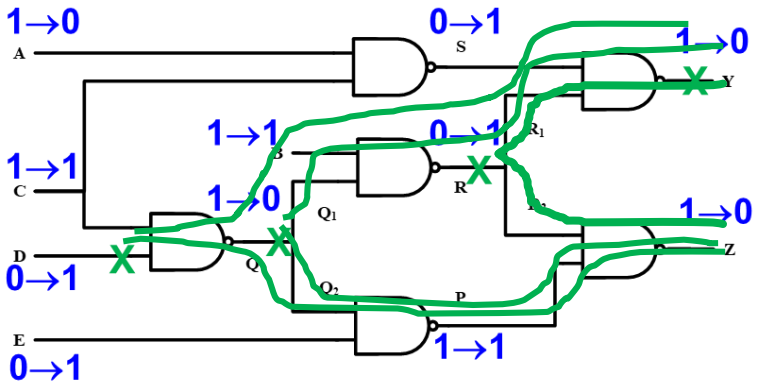
  - If gate output x does not change

$$AT_x = \text{N.A.}$$

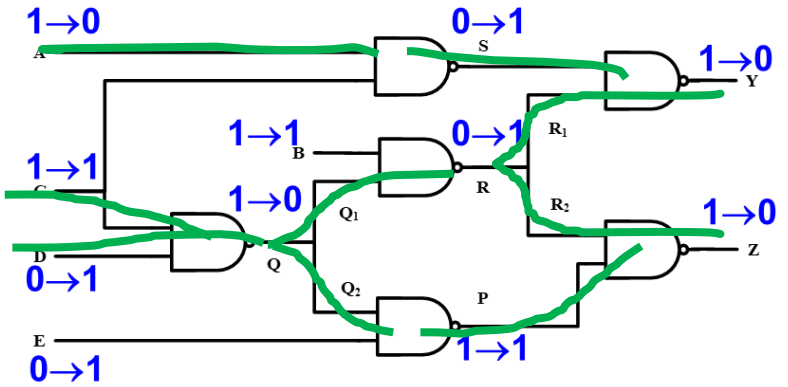


How to Calculate PT?

- *Propagation time* (PT_x)= time to propagate fault effect from *x* to PO/PPO
- Method 1: Forward calculation fault by fault
  - Slow, overlapped calculation
  - Example:
    - R→Y, R→Z
    - Q →Y, Q →Z
    - D →Y, D →Z



- Method 2: *Non-robust* path backtrace
  - *Side input is non-controlling* at V_2
    - (See Video 9.2)
  - Fast, no calculation overlap
  - Example:
    - YZ →SRP →QA →CD
    - E and B Not traced



Method 2 (Backward) is Better

③ Delay Calculation, PT

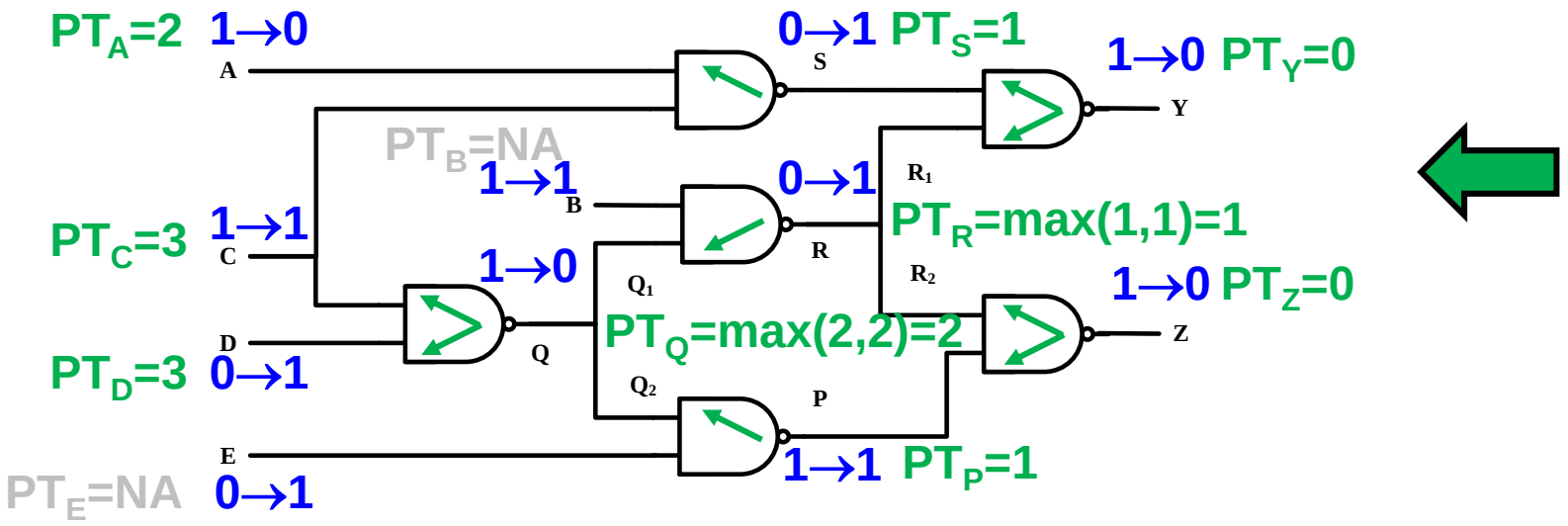
- **Calculate PT from output to input, trace non-robust sensitized paths**

$$PT_i = \begin{cases} PT_o + d_i, & \text{if gate is NR sensitized} \\ NA, & \text{if gate is not NR sensitized} \end{cases}$$

- **PT of fan out stem = maximum of PT of its branches***

$$PT_{stem} = \max_{i \in branches} (PT_i)$$

**Reconverged fanout branches must be handled carefully*

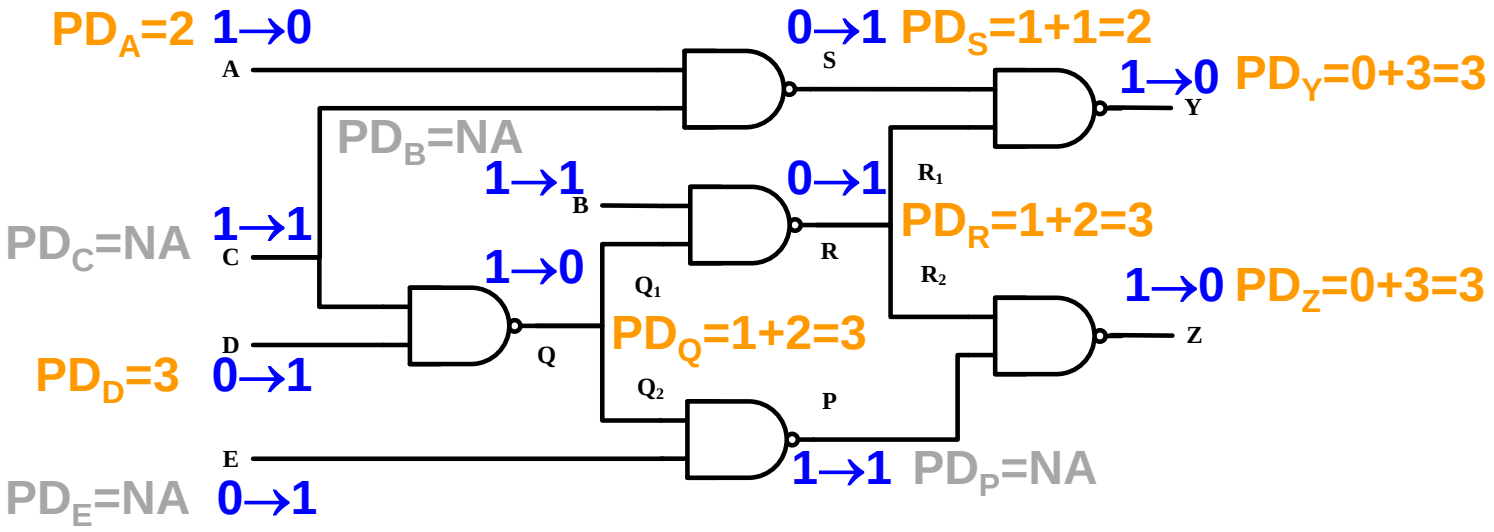


③ Delay Calculation, PD

- ***Propagation Delay*** **PD_x = time to travel from PI/PPI to PO/PPO through *x***

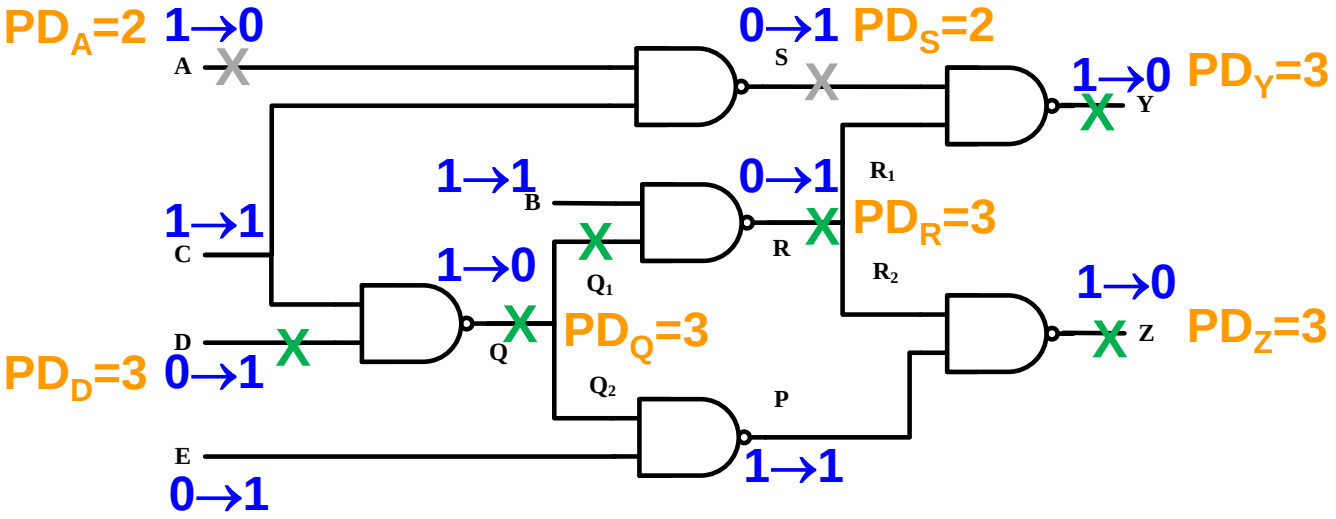
$$PD_x = AT_x + PT_x$$

- ***PD_x=NA if PT_x = NA or AT_x=NA***
  - ***C* and *P* are *NA* because *AT* = *NA***
  - ***E* and *B* are *NA* because *PT* = *NA***



④ Fault Drop

- Fault *f* is ***dropped*** when two conditions met
  - 1) TDF *f* is detected: AT≠NA and PT≠NA (WHY? FFT)
  - 2) PD_f is long enough* *user defined fault drop criteria
- Example: assume $PD_f \geq 3$ to be dropped
  - 1) 8 TDF faults detected
  - 2) but only 6 of them can be dropped

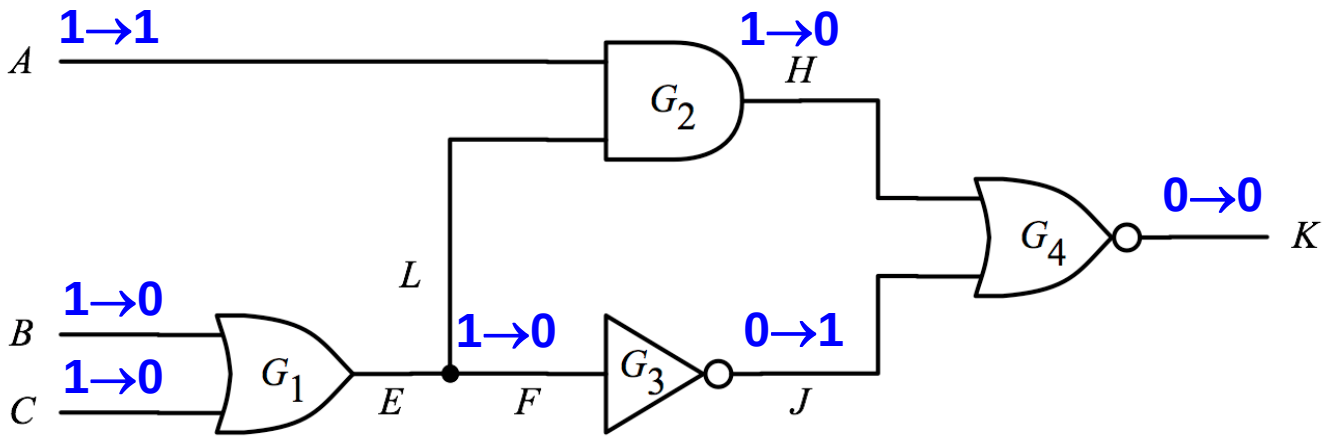


$$Fault\ Coverage_{TA} = \frac{number\ of\ dropped\ TDF}{number\ of\ total\ TDF} \times 100\%$$

Quiz

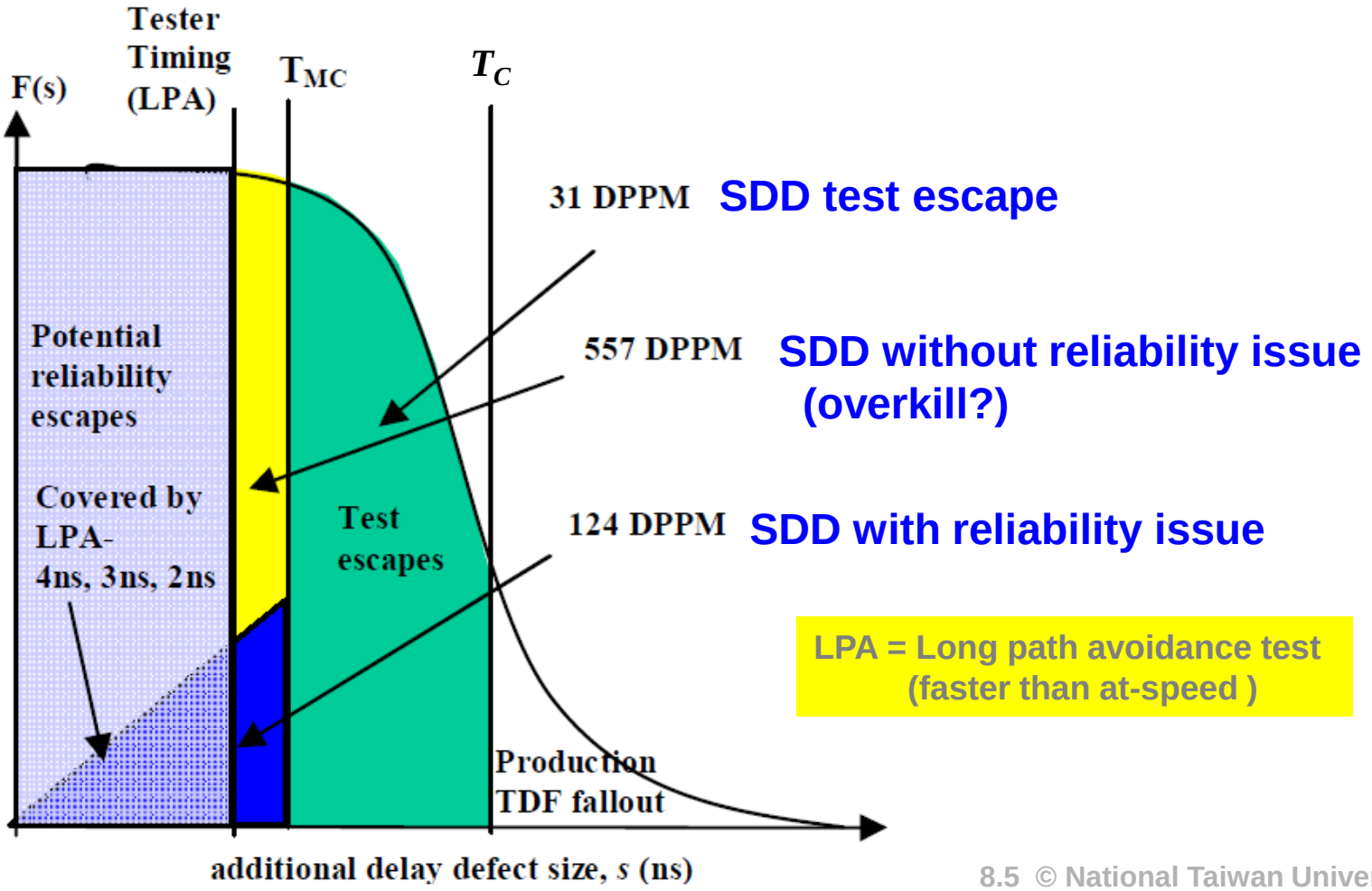
Q1: Suppose inverter delay is 1 and the other gate delays are 2.
What is PD_E?
Q2: Suppose fault drop criterion is PD >4. Can we drop E STF fault?

	A	B	C	E	H	J	K
AT							
PT							
PD							



LSI Logic Experiment [Turakhia 07]

- **Total 32K chips tested, 23 small delay defects**
  - **Before stress : 1 escaped slow test but fail fast functional test (31 DPM)**
  - **After stress, 4 failed (124 DPM), 18 passed (557 DPM)**



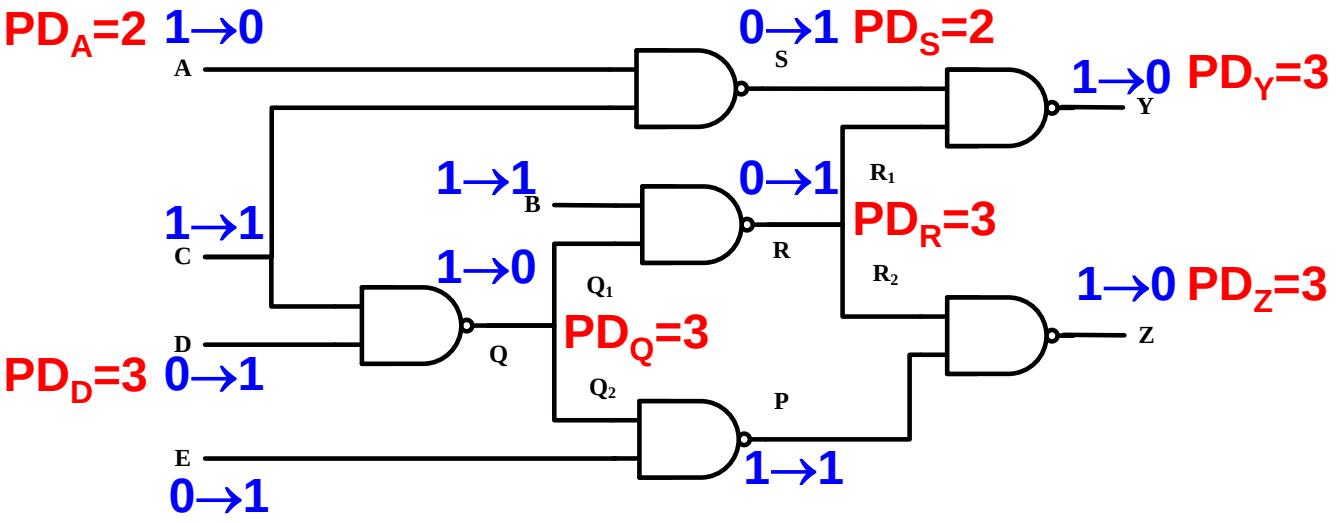
LPA = Long path avoidance test (faster than at-speed)

Summary

- Small delay defects (SDD) important for modern technologies
  - How to detect? Faster test or longer sensitization paths
- Timing-aware ATPG tries to
  - Activate long paths or Propagate fault effect through long paths
- Algorithm example
  - ① Pre-select long paths
  - ② Generate test patterns
  - ③ Calculate AT, PT, PD
  - ④ Drop faults that meet criteria
- Advantage of Ta-ATPG
  - ☺ Detect SDD : reduce DPM or potential reliability issues
- Disadvantages of Ta-ATPG
  - ☹ Longer test length ☹ Run time overhead

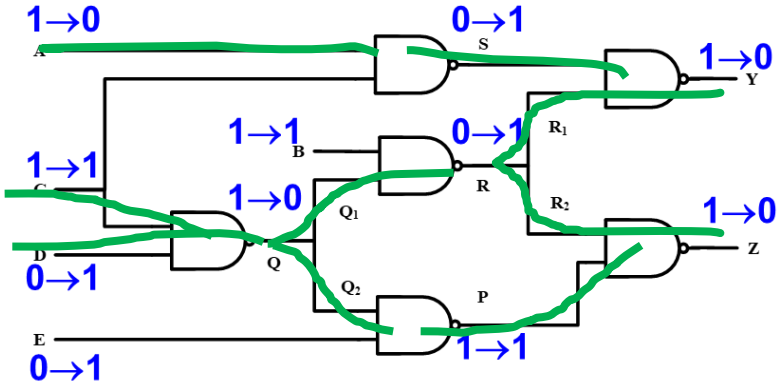
FFT

- Q: A STF is NOT dropped because $PD_f < 3$
  - How can we drop A STF?



FFT

- **Q1: TDF *f* is detected (*i.e.* AT≠NA and PT≠NA). Why?**
- **Q2: Any exception where fault f is detected but AT=NA or PT=NA ?**



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