Introduction

- **What Is Testing**
- **Types of Testing**
- **Test Quality**
- **Test Economics**
- **Issues in Testing**
- **Conclusion**

Types of Testing

Testing (generally speaking)

- Design Verification
- **Explicit Testing**
- Implicit Testing Or On-line Testing

don't worry about names too much

Explicit Testing:
- Characterization Test
- Production Test
- Reliability Test
- Diagnosis Test

Production Test:
- Wafer Test
- Package Test
- System Test

Reliability Test:
- Burn-in
- Acc. Life test

- Gross Test
- DC parametric Test
- AC parametric Test
- Boolean Test
- Delay Test
- Functional Test
- IDDQ, VLV

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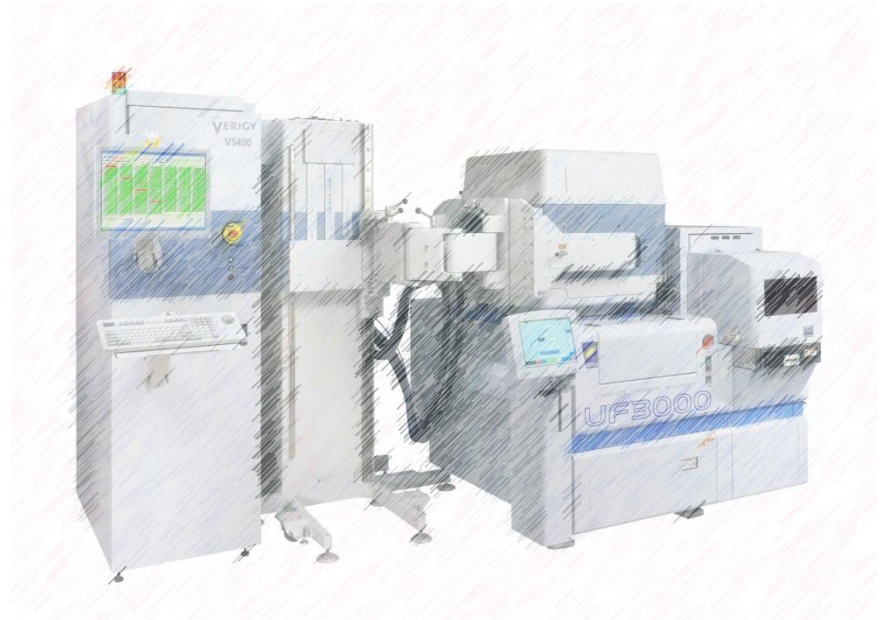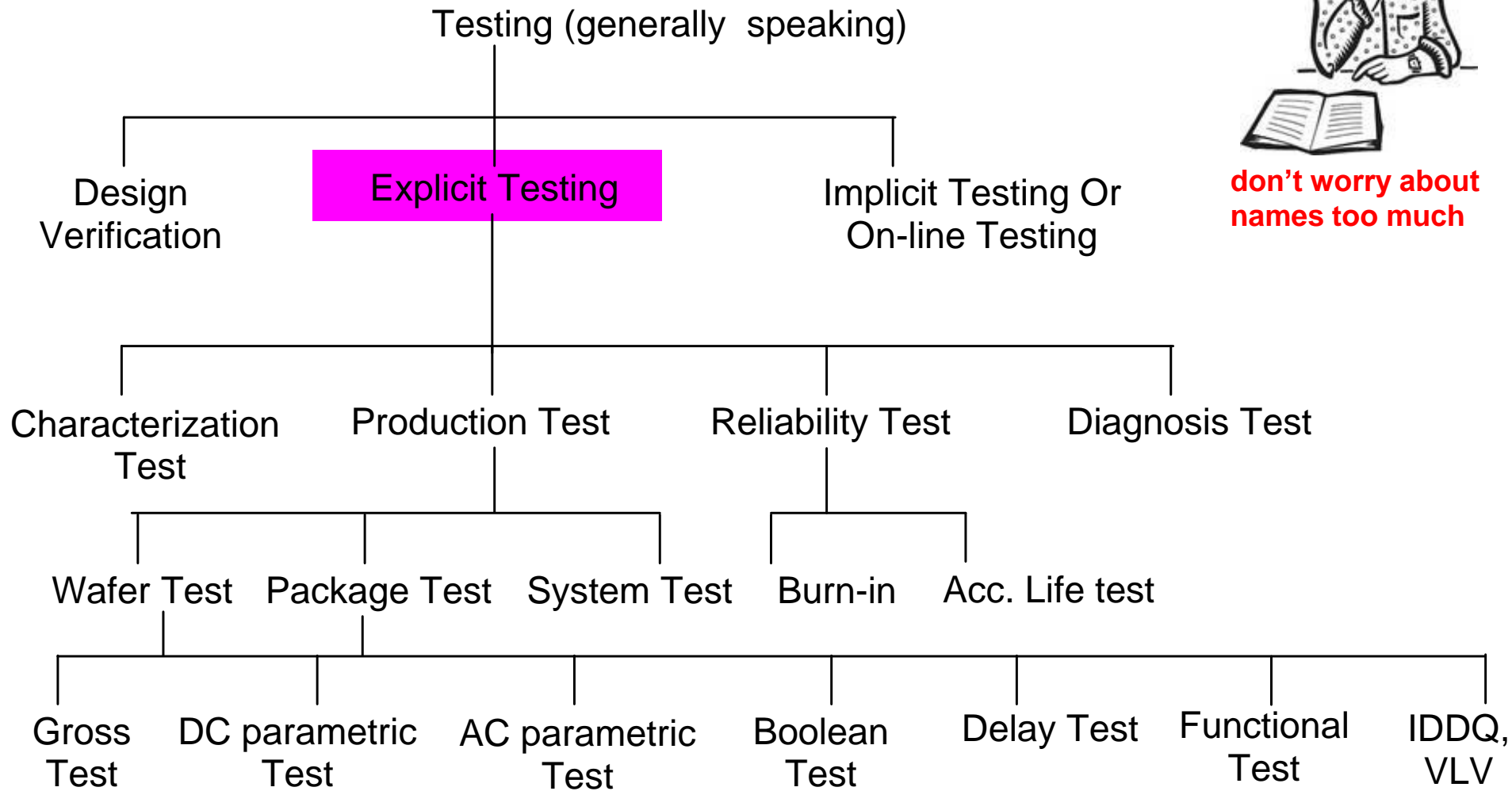
Why So Many Tests?

- **Design errors** → *Design Verification*
  - ♦ **Logic design errors, physical design errors**
- **Manufacturing Defects** → *Explicit Testing*
  - ♦ **Mask problems, lithography problem**
  - ♦ **Particles or scratches**
  - ♦ **Bad manufacture recipe**

  Focus of class

- **External or Environmental Disturbance** → *Implicit Testing*
  - ♦ **Electromagnetic interference**
  - ♦ **Alpha particles**
  - ♦ **Power supply disturbance**
- **Wear out** → *Reliability Testing*
  - ♦ **Electromigration**
  - ♦ **Corrosion**
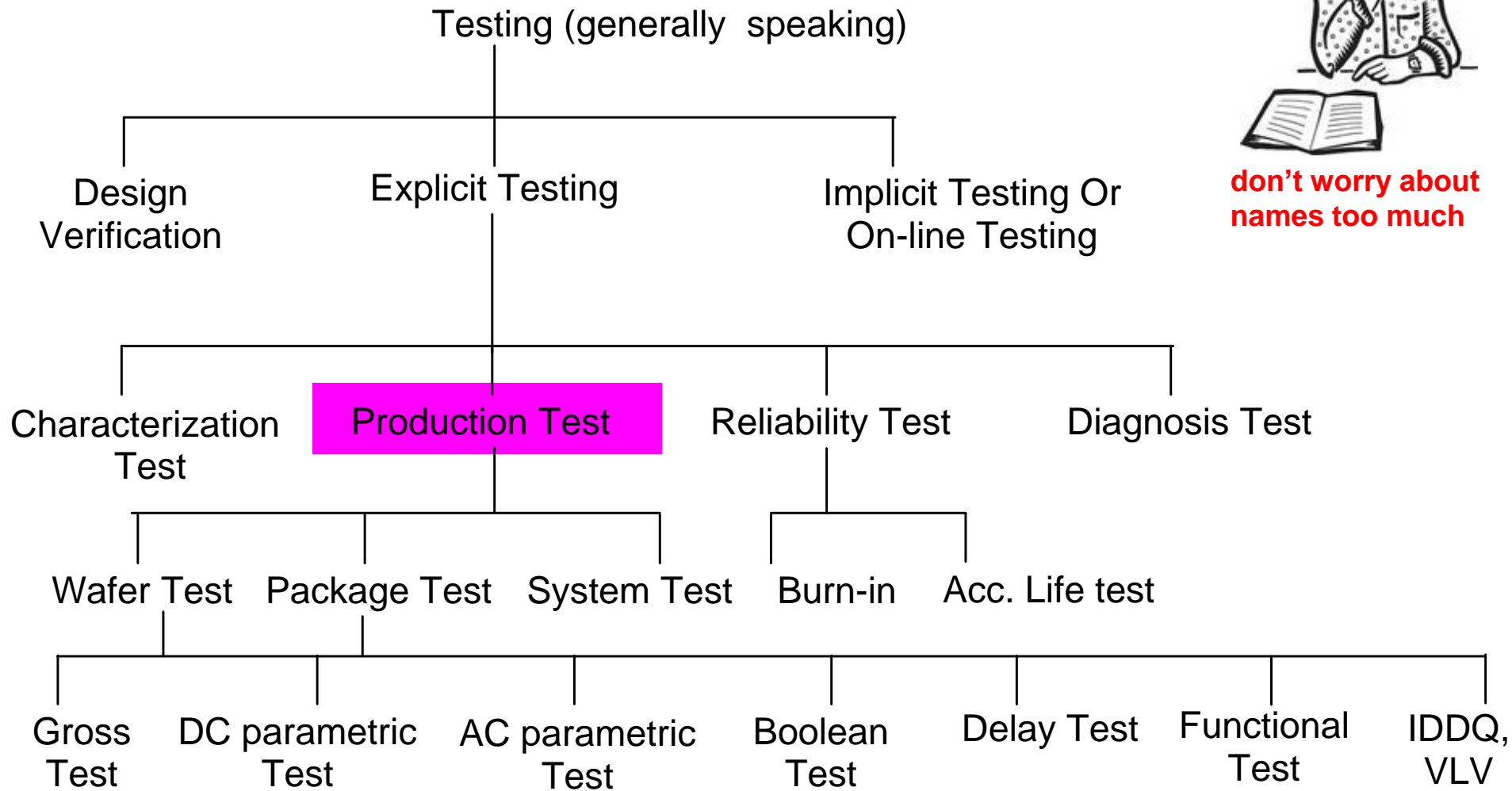
Because There Are Many Different Problems!

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Classification of Explicit Testing

- **According to purposes**
  - *Production test:* for volume production
  - *Characterization test:* for prototype IC, silicon debug
  - *Reliability test:* for reliability defects
  - *Diagnosis test:* for identify defect location
- **According to stages**
  - *Wafer test* (aka. *Wafer sort, wafer probe*): on wafer
  - *Package test* (aka. *Final test*): after packaging
  - *System test*: in system
- **According to test techniques**
  - **DC parametric test**: VOH/VOL/VIH/VIL ...
  - **AC parametric test**: rise/fall time, operation frequency …
  - **Boolean test** : apply test patterns at low speed for DC faults
  - **Delay test**: apply test patterns at fast speed for delay faults
  - **Functional test**: apply design verification patterns
  - **IDDQ test**: measure quiescent power supply current
  - **Low voltage test**: test at reduced power supply voltage
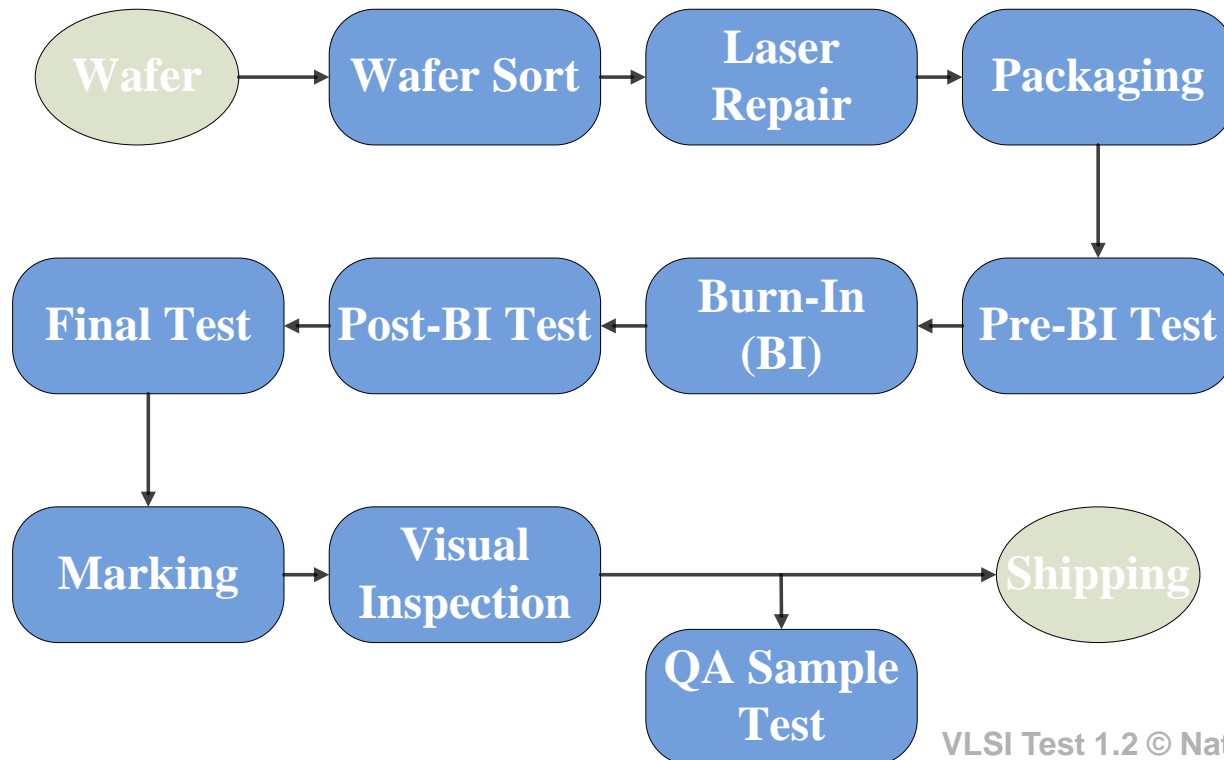
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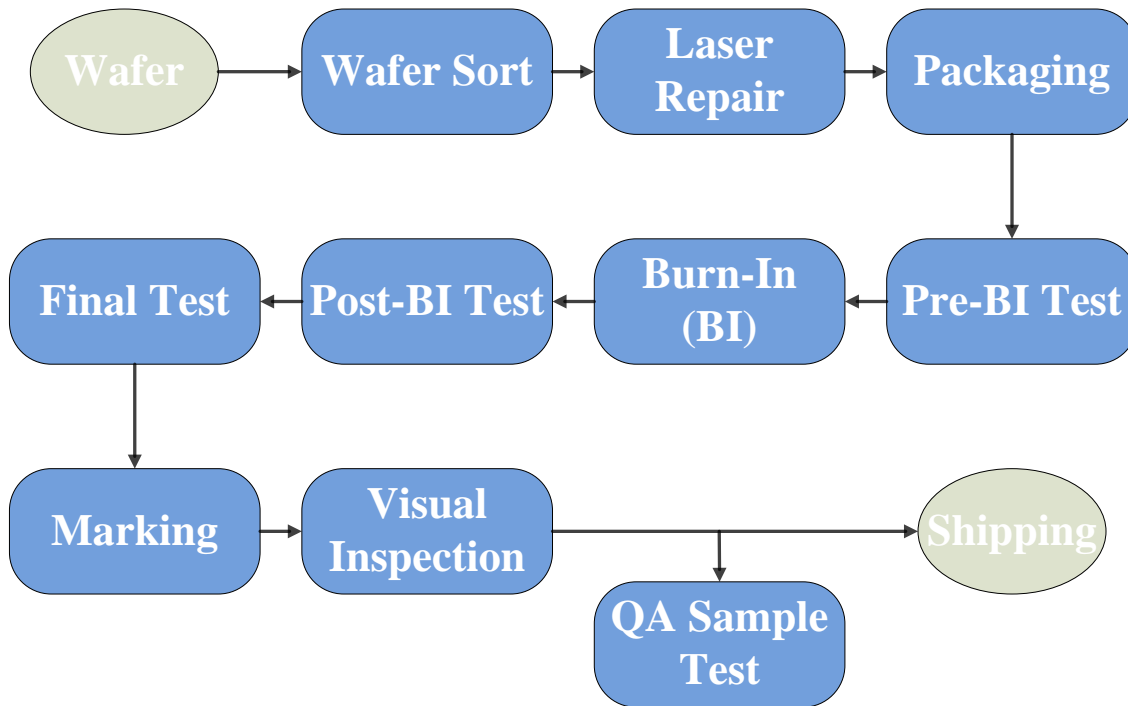- IDDQ, VLV

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Production Tests

- **Purposes:**
  - ♦ **1. Enforce quality requirements before selling to customers**
  - ♦ **2. Sort parts for different specifications**
    - ∗ *e.g.* **different speeds of CPU**
- **Example: a typical production test flow**
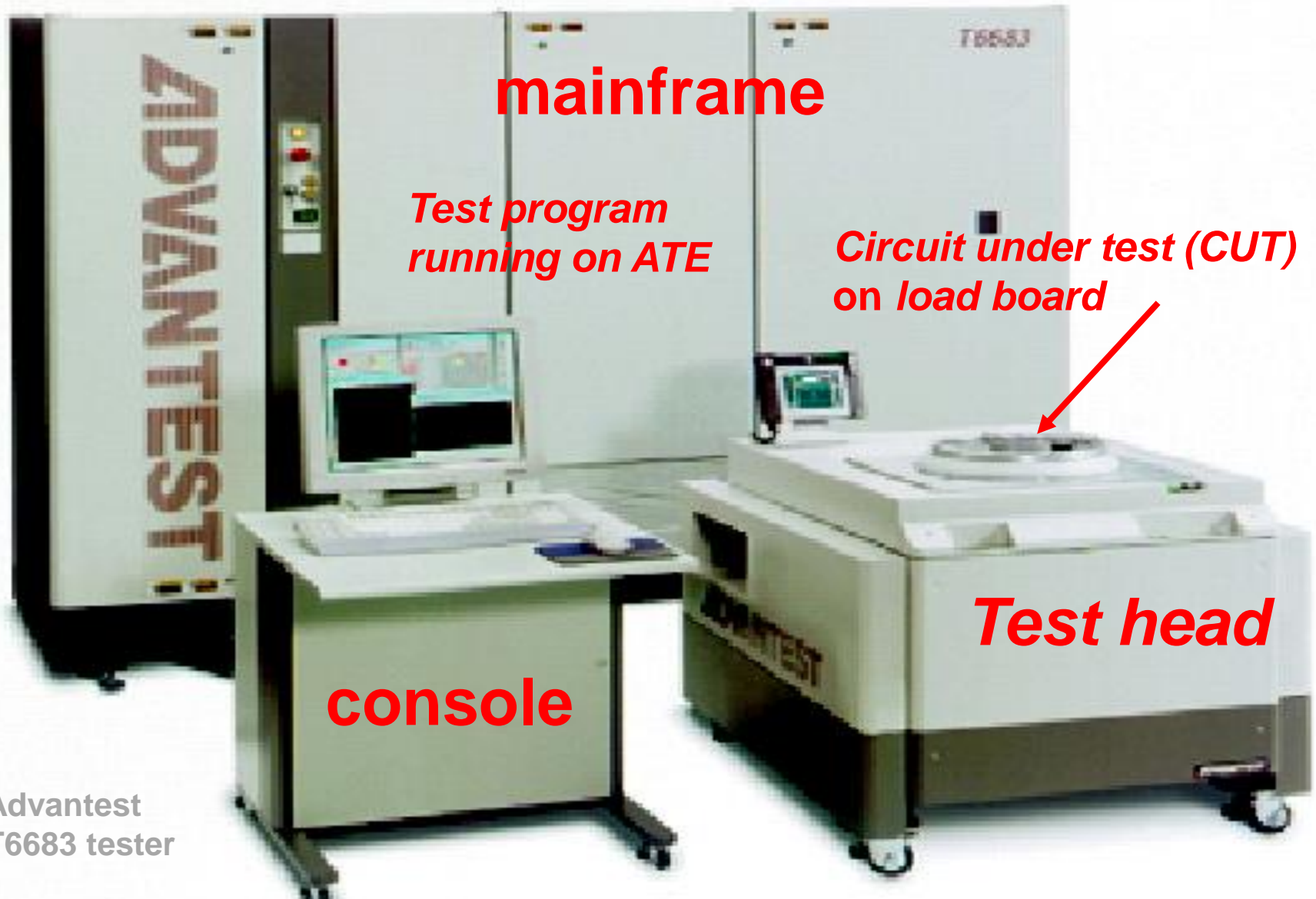 - ♦ **actual flow modified according to test cost and test quality requirements**

```
Wafer → Wafer Sort → Laser Repair → Packaging
                                         ↓
Final Test ← Post-BI Test ← Burn-In (BI) ← Pre-BI Test
   ↓
Marking → Visual Inspection → Shipping
                    ↓
              QA Sample Test
```

VLSI Test 1.2 © National Taiwan University

Food for Thought, FFT

- **Q: If we already have wafer test, why package test again?**

Production Test Floor

Yellow = Attention Needed
Green = PASS
Red = FAIL

Source: micron.com

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Automatic Test Equipment (ATE), Tester

mainframe

Test program running on ATE

Circuit under test (CUT) on load board

Test head

console

Advantest T6683 tester

Load Board

- **Test fixture to interface**
  - ♦ **ATE and**
  - ♦ *circuit under test (CUT)*

socket
(CUT inside)
Front side

Back side
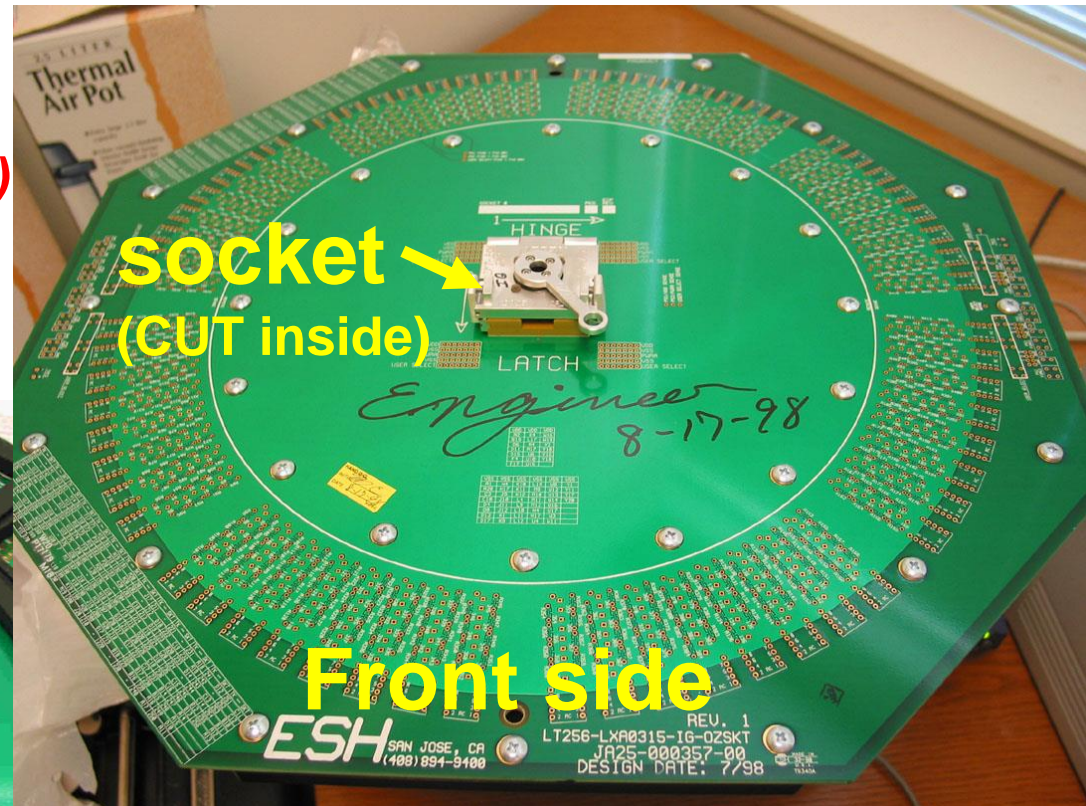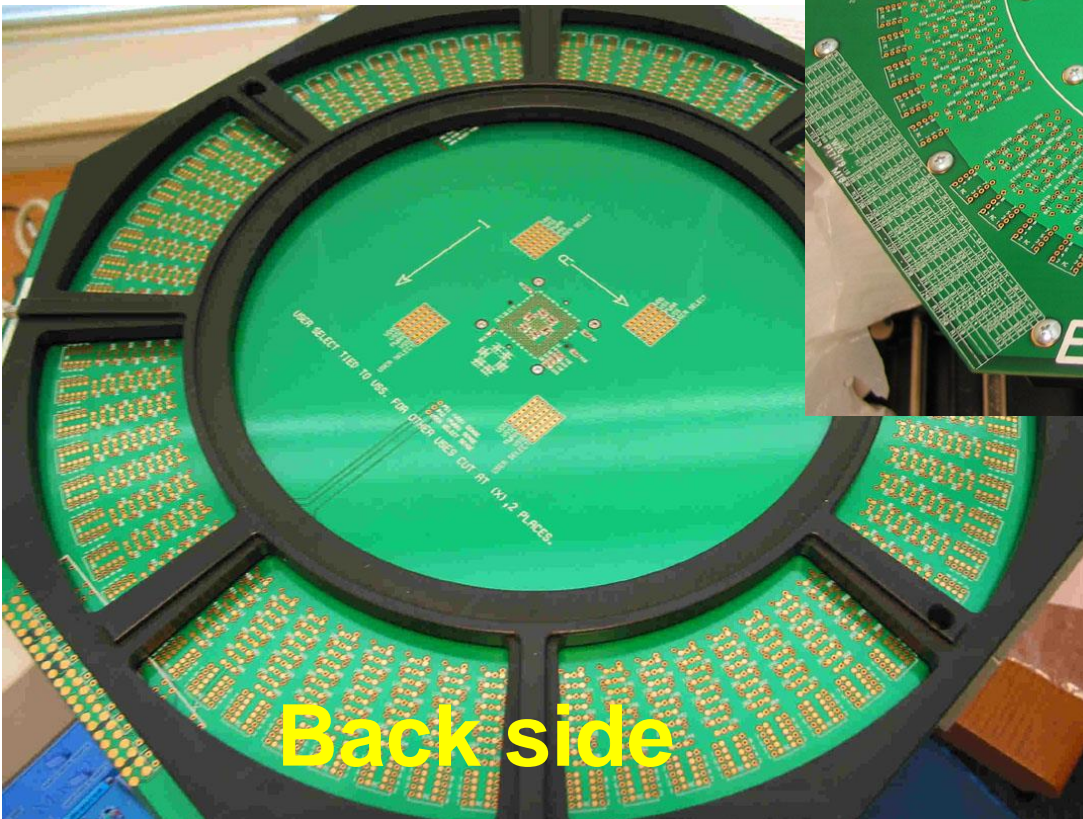
Handler

- **Robotic arm (inside) for moving packaged IC**
- **<Video demo>**

Advantest
M4541A handler

Types of Testing

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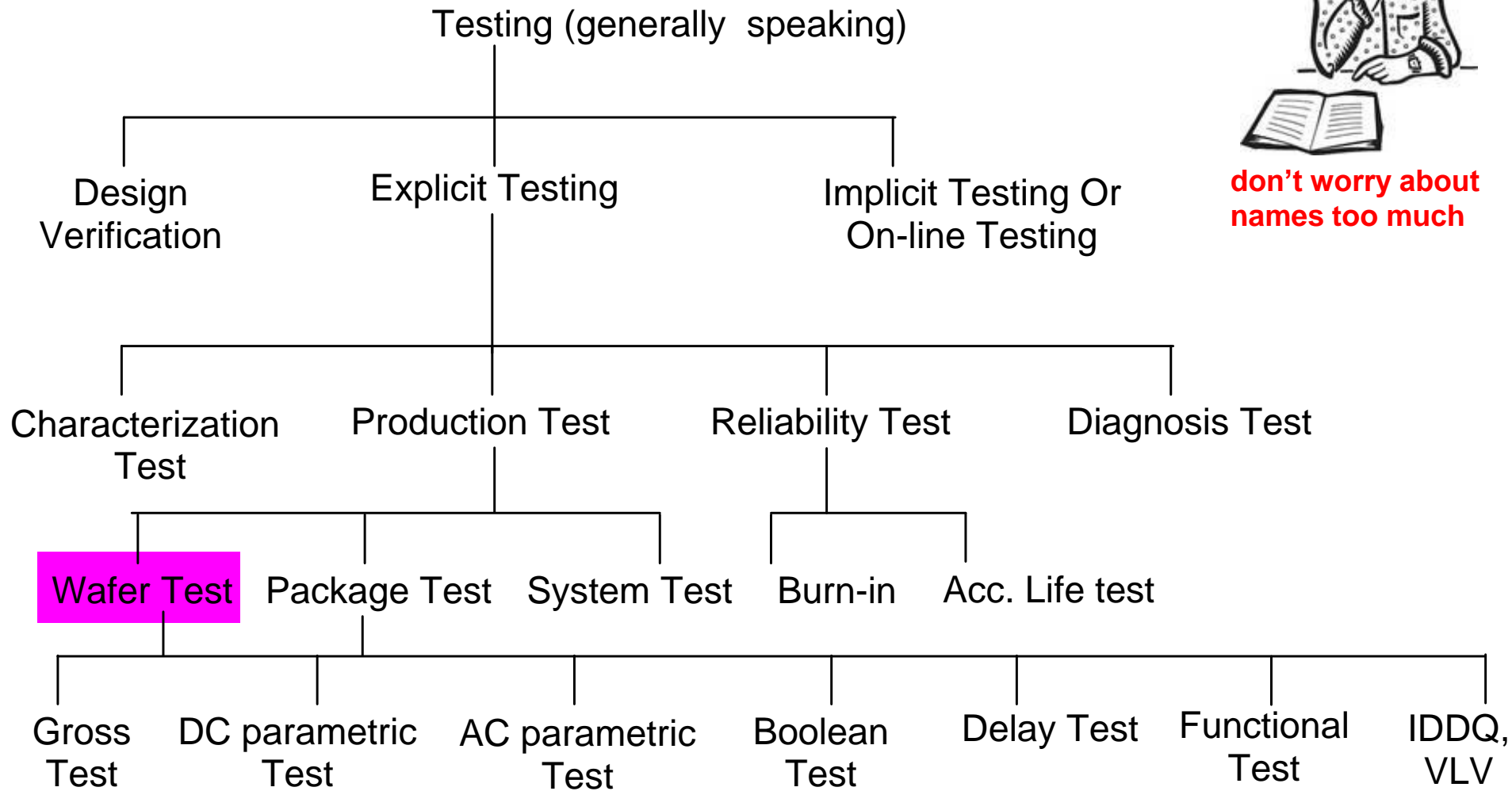
Wafer Test Setup

- **Source: Verigy.com**

Test head **(face down)**

wafer and probe card

ATE

Probe station

1

sity

Probe Card

- **Test fixture to interface load board and die**
- **Signal integrity is a big concern**
  - **Many tiny needles contacting die, cannot probe at fast speed**
  - **Must carefully balance inductance and capacitance of each pin**
  - **Need regular cleaning after a numbers of *touch downs***
- **Probe card wears out quickly so it should be replaced regularly**

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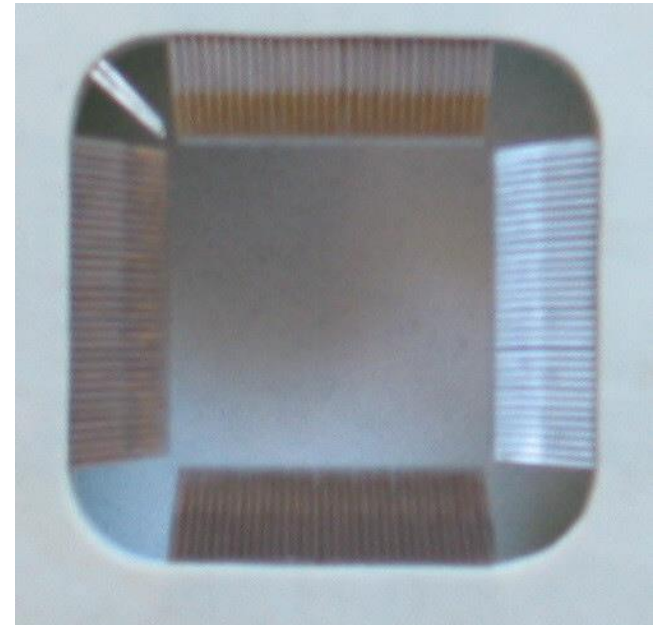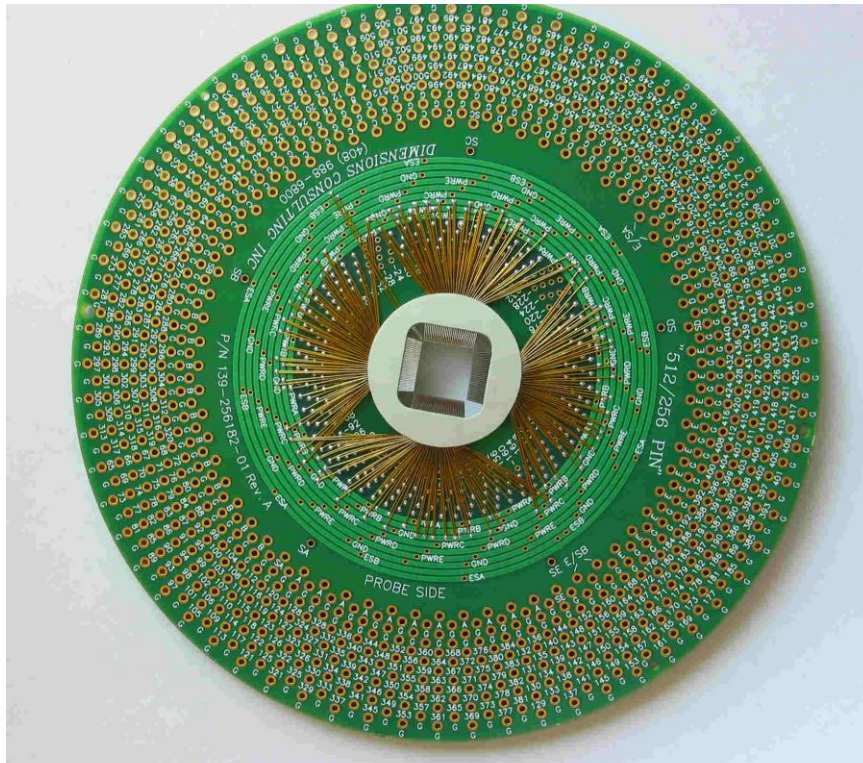
Wafer Map

- **Why we call it *wafer sort*?**
- ***Wafer map* shows test results**
  - **Die are sorted into different *Bins***
- **Example:**
  - **Bin #1: PASS ALL**
  - **BIN #2: FAIL FUNCTION test**
  - **BIN #3: FAIL IDDQ test**
  - **BIN #4: FAIL DC parametric test**
- **Wafer map very useful for**
  - **pass/fail decision**
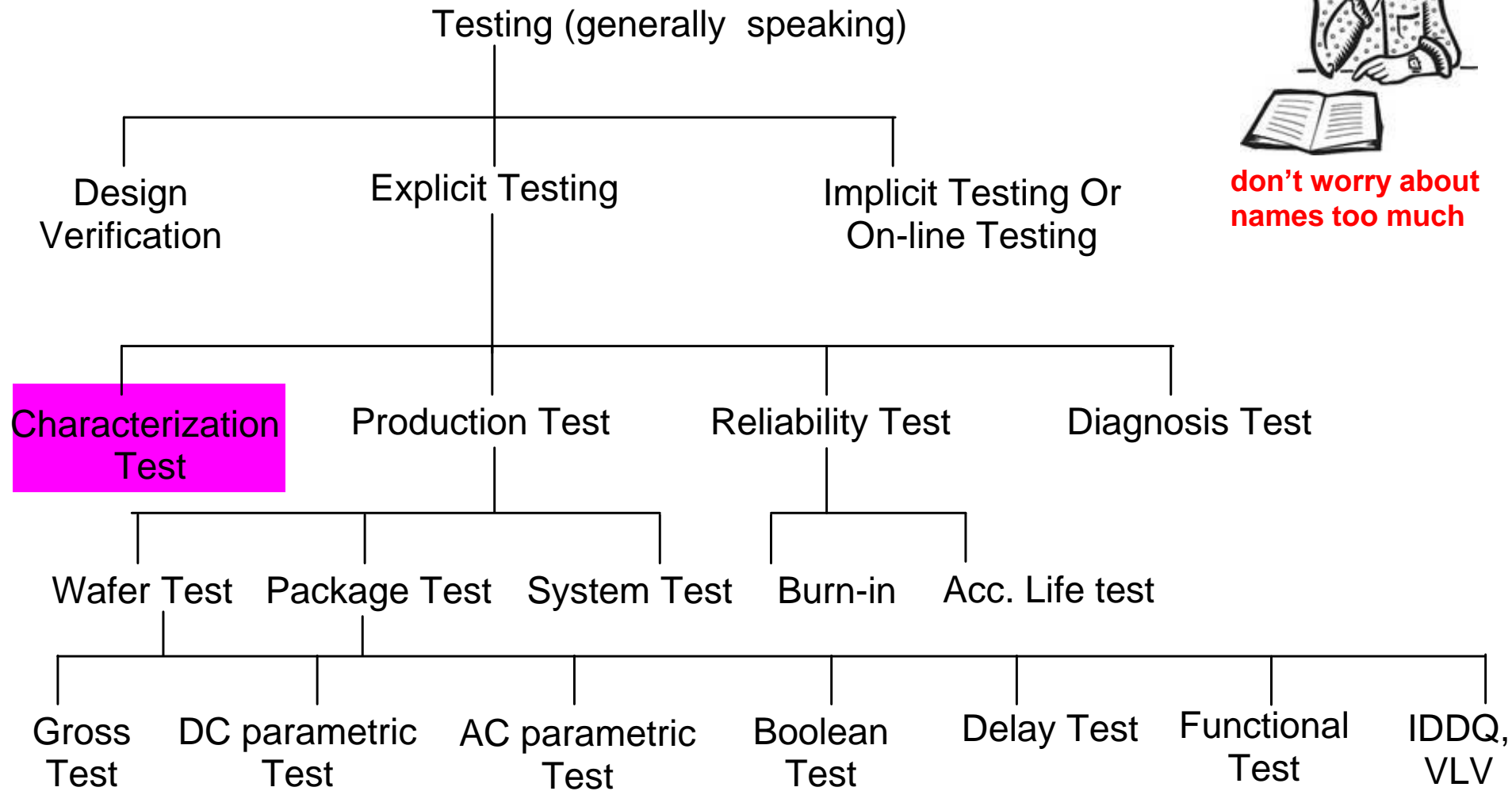 - **diagnosis**
  - **yield improvement**
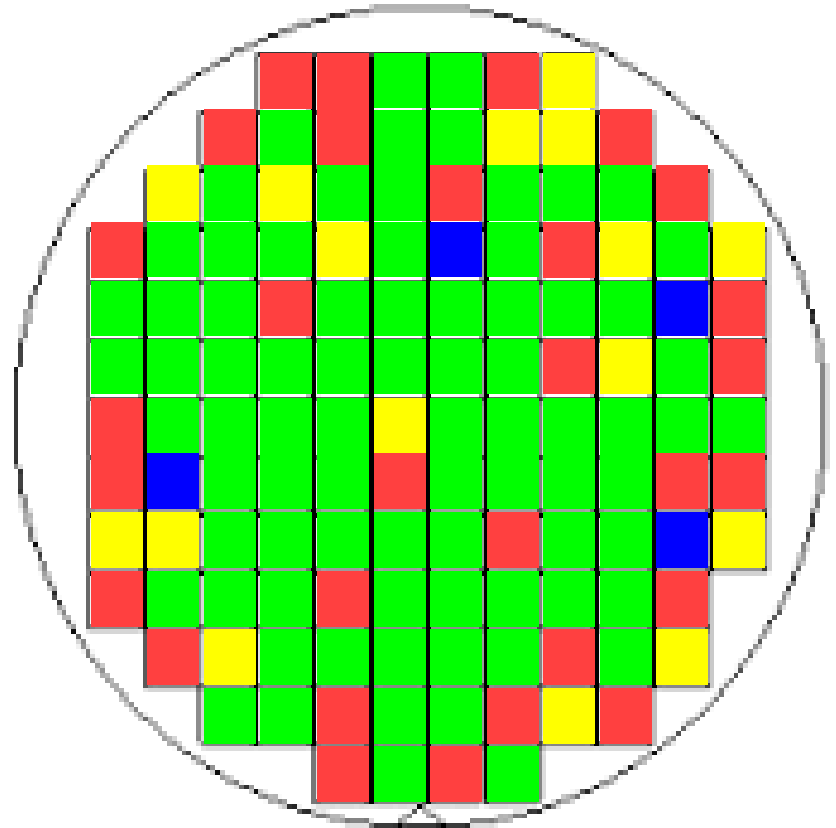
Yield=Bin#1/total = 78/130=60%

Video Clip

- You can see a typical production test environment

- youtube video
  - "DELTA Test solutions since 1976"
  - https://www.youtube.com/watch?v=yKI71IX8Zc0

- Terminology
  - Probe Station =Wafer prober
  - Component test = Package test
  - Electro Anti-static

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Production Test

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Diagnosis Test

Wafer Test   Package Test   System Test   Burn-in   Acc. Life test

Gross Test   DC parametric Test   AC parametric Test   Boolean Test   Delay Test   Functional Test   IDDQ, VLV

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Characterization Tests

- **Test a small amount of prototype IC very thoroughly**
  - ◆ **Test cost and test time are not big concerns**
- **Purpose of characterization test**
  - ◆ **1. Verify IC function is same as design (silicon debug)**
  - ◆ **2. Confirm IC specifications under different test conditions**
    - ∗ **Specifications: speed, VOH/VOL, rise/fall time …**
    - ∗ **Conditions: VDD, Temperature …**
  - ◆ **3. Developing test program for production test**
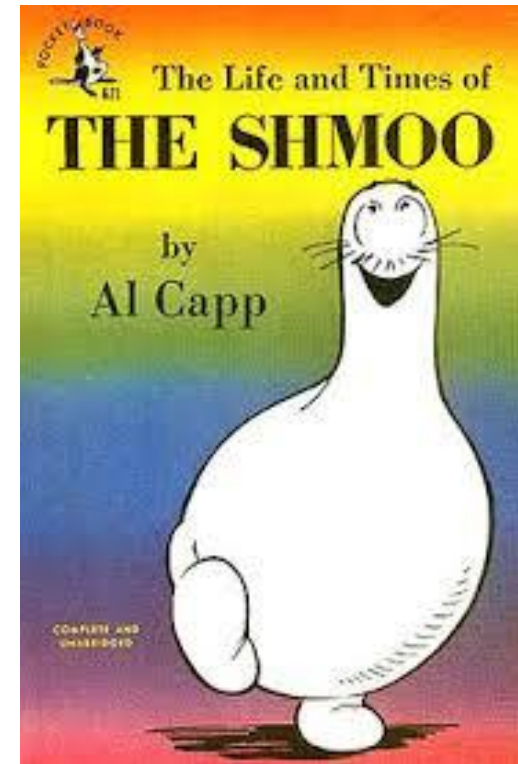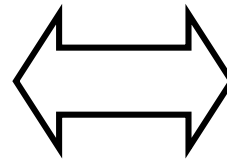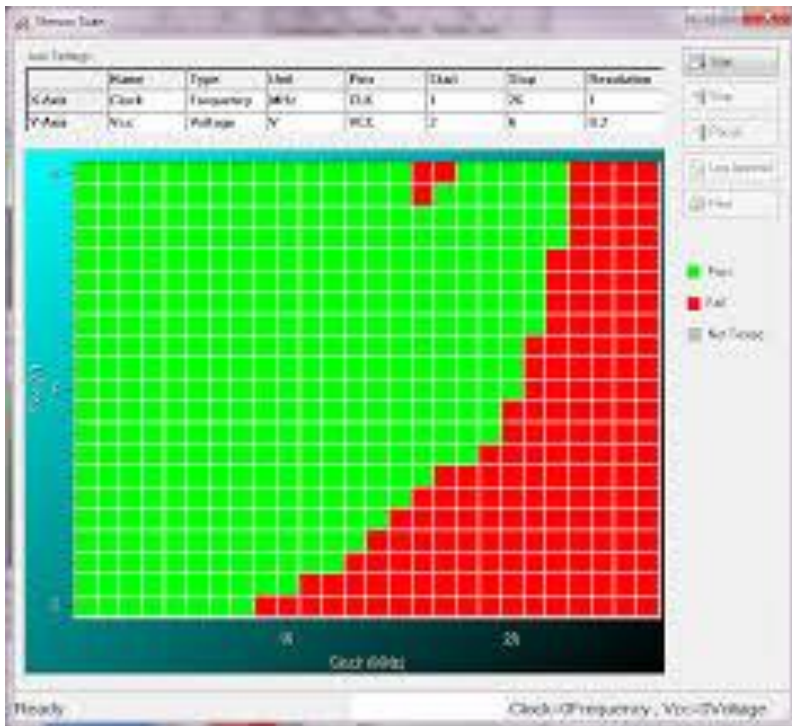   - ∗ **Determine Pass/Fail limits**

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Shmoo Plot

- **Graphical display of CUT test results under different test conditions**
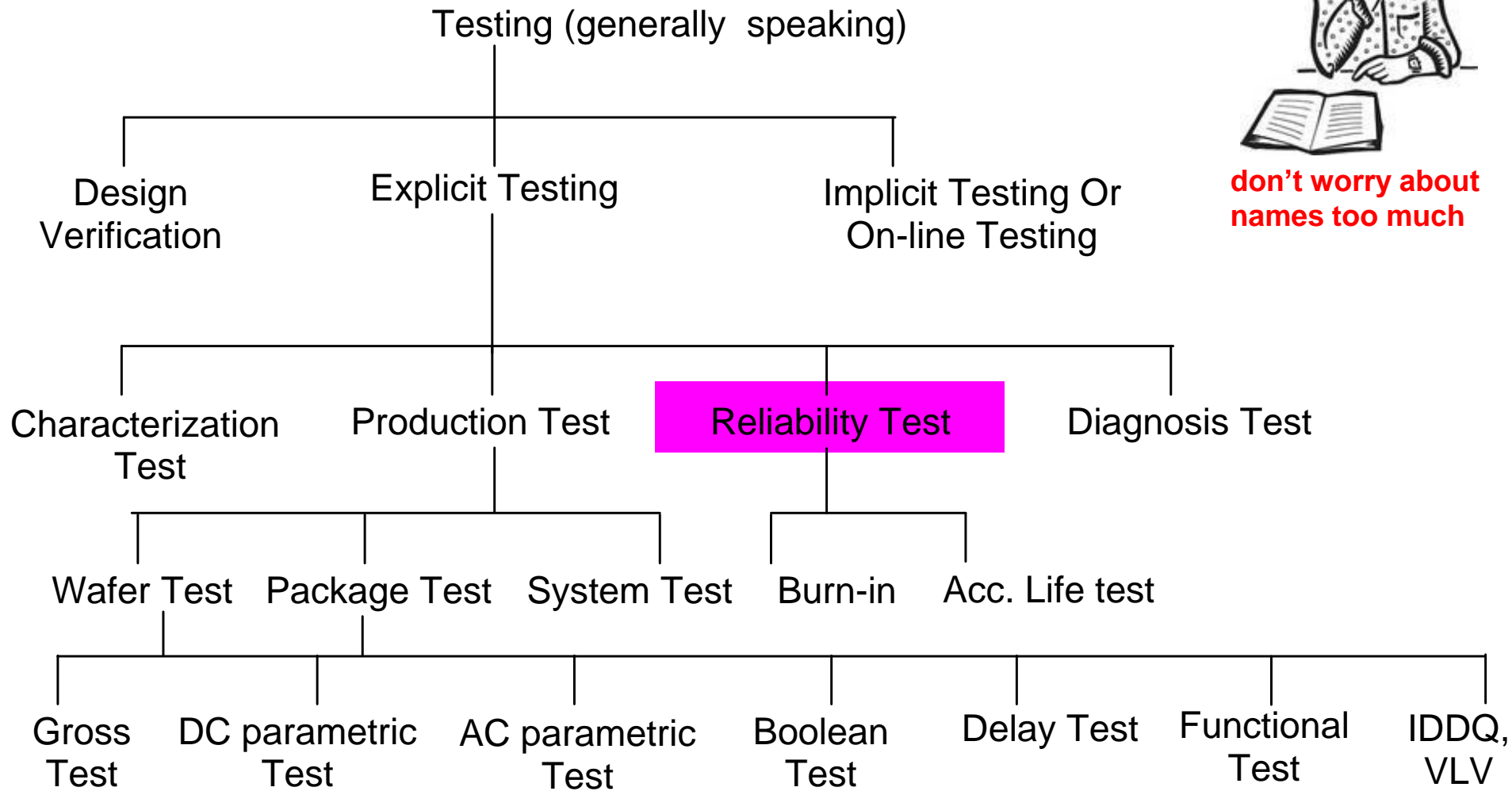- **Example: clock period vs. VDD**
  - ♦ **Green = PASS ; Red = FAIL**

National Taiwan University

Why Shmoo?

- **Funny shape resembles a cartoon character: shmoo**
  - ♦ **Youtube Video: 1979 NBC Cartoon**

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Reliability Tests

- **_Burn-in_**
  - ◆ **Goal: screen out _infant mortality_ (aka. _Early-life failure_)**
  - ◆ **Method: raised temperature and voltage for hours or days**
    - ∗ **cook IC in oven!**
  - ◆ **Very costly. Only applied to expensive IC**
- **_Accelerated life test_**
  - ◆ **Goal: estimate life time of IC**
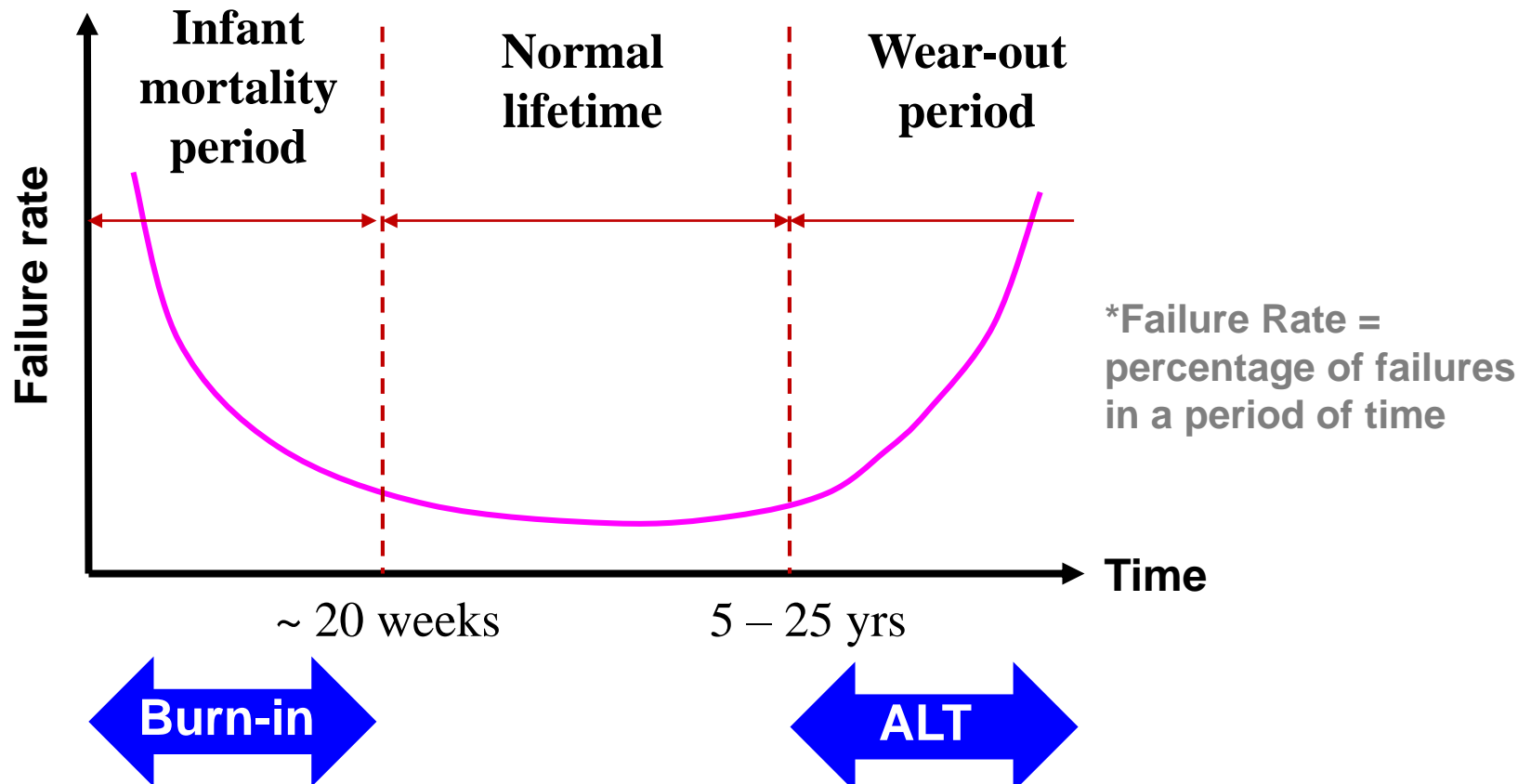 - ◆ **Method: burn-in until IC are dead**
  - ◆ **Only applied to sampled IC**
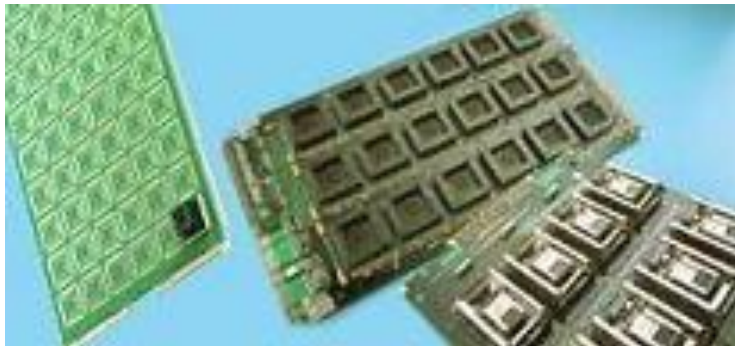
Burn-in board

Burn-in oven siliconfareast.com

Bathtub Curve

- **IC's *failure rate*[*] resembles a bathtub**
  - ♦ ***Infant mortality*: fail early in life, due to *reliability defects***
  - ♦ ***Wear out*: normal life time, due to *aging***

Infant mortality period

Normal lifetime

Wear-out period

Failure rate

*Failure Rate = percentage of failures in a period of time

Time

~ 20 weeks

5 – 25 yrs

Burn-in

ALT

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**These Topics Are NOT in This Course**

Explicit Testing ≠ Verification

- *Verification*
  - ♦ **Purpose : check if design correctly implements specified behavior**
  - ♦ **Done *before* manufacture to catch design errors (*bugs*)**
  - ♦ **Approaches: simulation, formal verification, …**
- *Explicit testing*
  - ♦ **Purpose: check if IC is functioning correct or defective**
  - ♦ **Done *after* manufacture to catch *defects***
  - ♦ **Approaches: apply test patterns by tester, …**

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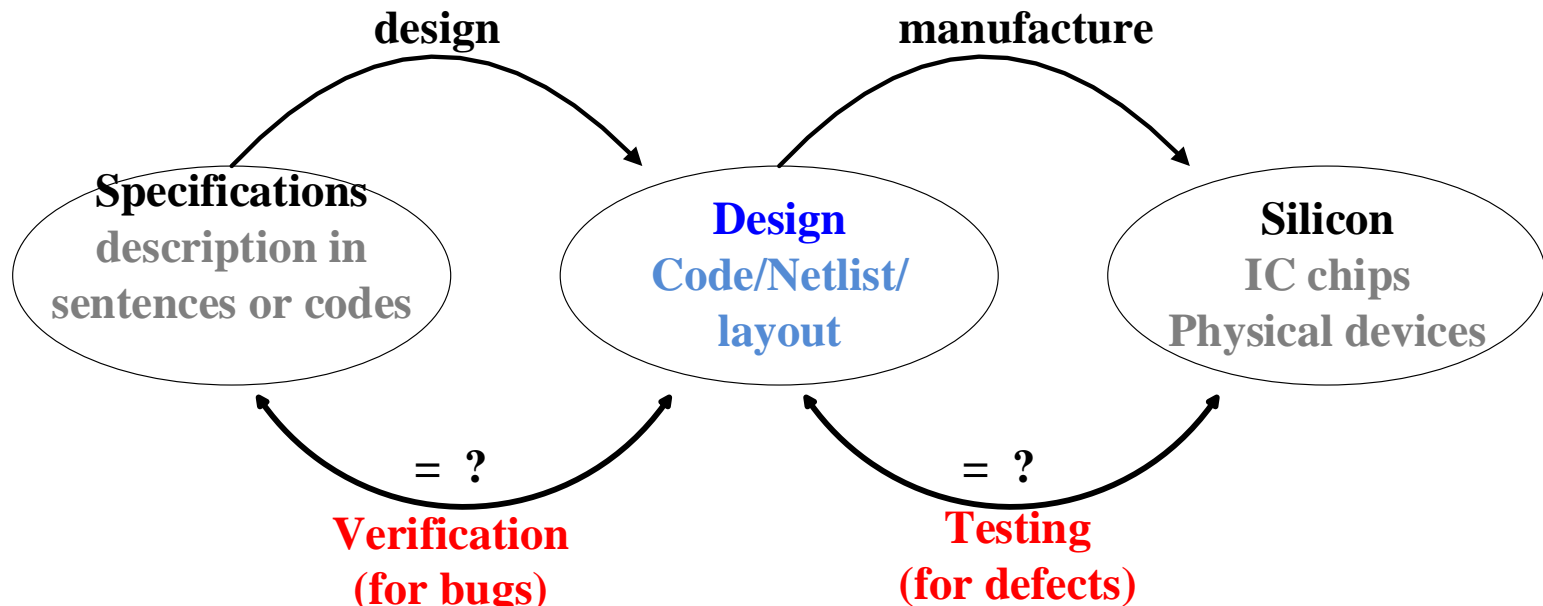
Implicit Testing

- **Purpose**
  - **Check IC output correctness during normal operation**
- **Also known As (aka):**
  - ***Concurrent Error Detection* (CED)**
  - ***On-line testing***

- **Important for mission critical systems**
  - **Airplanes, satellites, mainframe computers**

- **Techniques**
  - **Circuit level techniques**
    - ***Error Correction Code* (ECC) protection of memory**
  - **System level techniques**
    - ***Watch dog timer***

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Summary

- **Focus of this course: explicit testing**
  - ♦ **Off-line IC testing on a specialized tester**
  - ♦ **Explicit testing ≠ verification ≠ on-line testing**
- **Many different type of tests for different**
  - ♦ **Purposes**
  - ♦ **Stages**
  - ♦ **Techniques**

Testing (generally speaking)

Design Verification — Explicit Testing — Implicit Testing Or On-line Testing

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