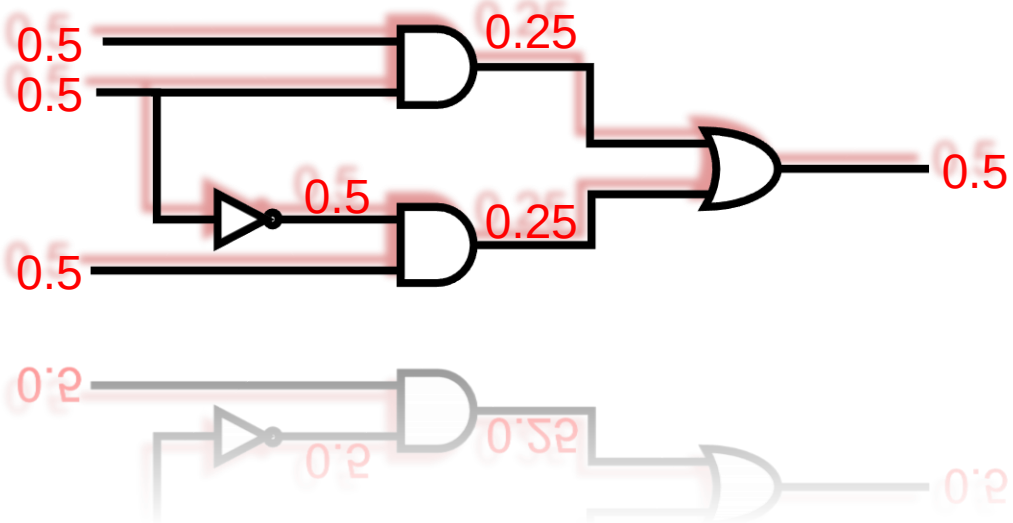
Testability Measure

- Introduction
- SCOAP
- COP
- High-level testability measures
  - (NOT in EXAM)

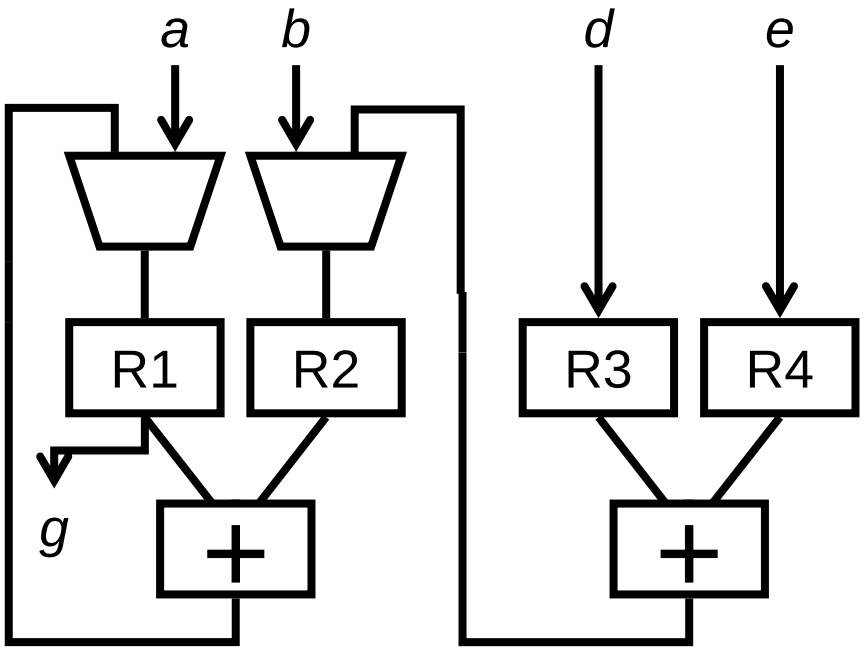


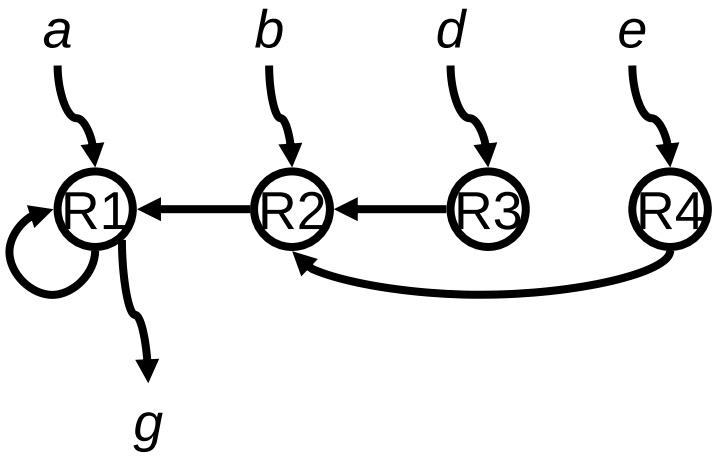
High-Level Testability Analysis

- **Based on behavioral level circuit model.**
- **Usually part of the behavior synthesis program.**
  - **To improve the testability at earlier design stage.**

Data Flow Graph (DFG)

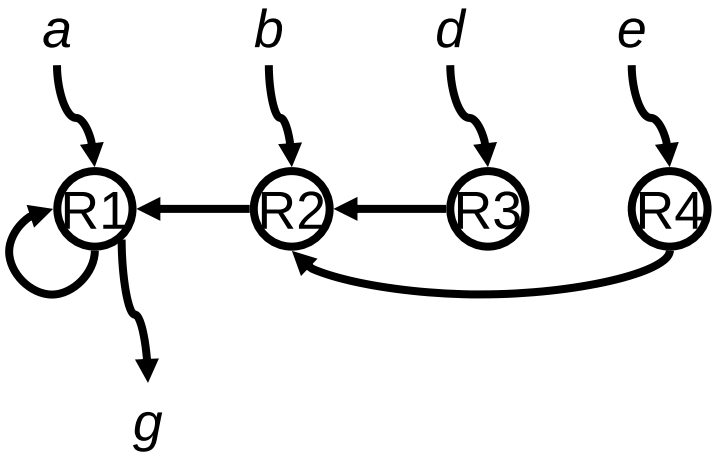
- **Each node corresponds to a register.**
- **Each arc represents a combinational path between two registers.**





A High-Level Testability Measure – *Sequential Depth*

- **The length of a sequential path between two registers is the number of arcs along the path.**
- **The sequential depth between a pair of registers is the length of the shortest path between them.**



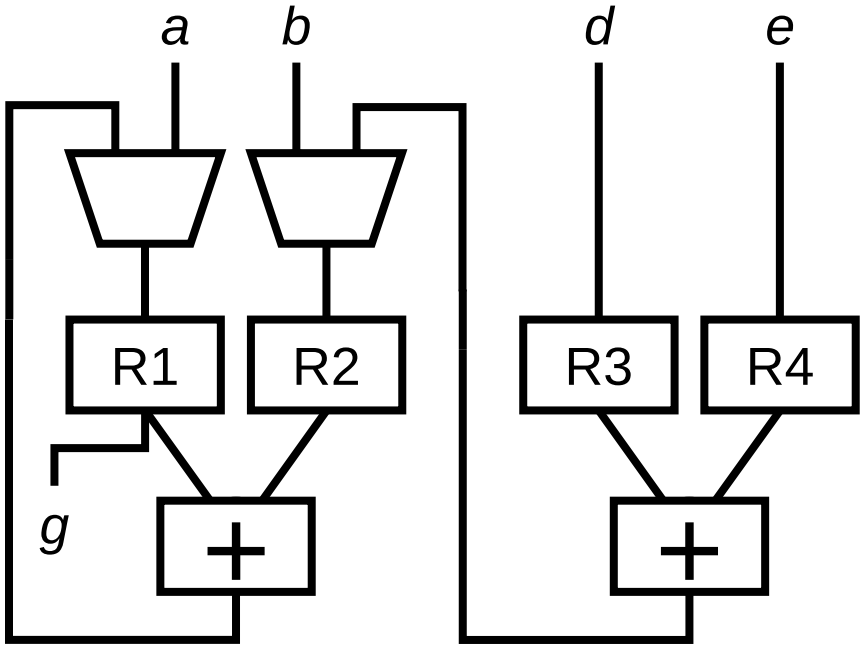
R1 → R1 : 0
R2 → R1 : 1
R3 → R1 : 2
R4 → R1 : 2

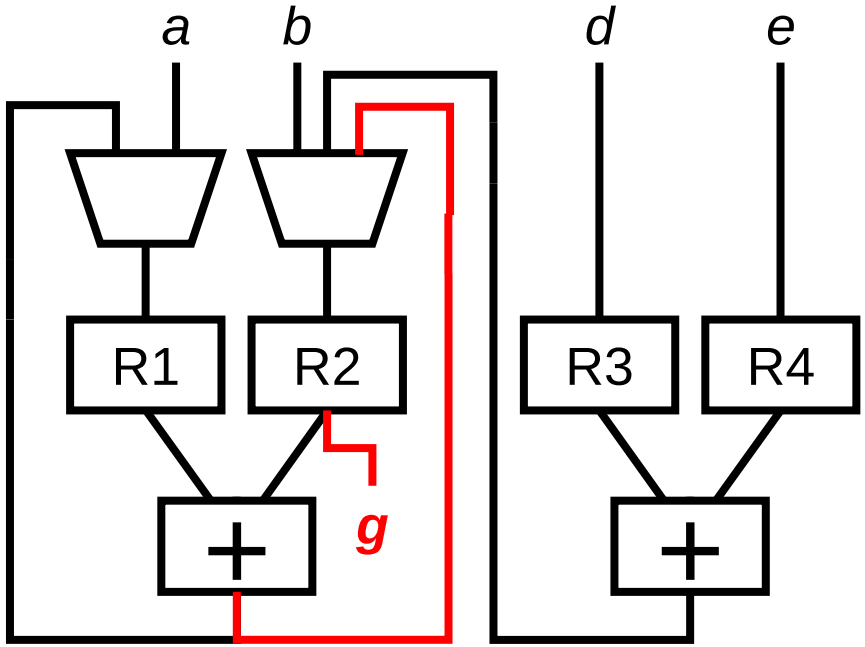
a → *g* : 2
b → *g* : 3
d → *g* : 4
e → *g* : 4

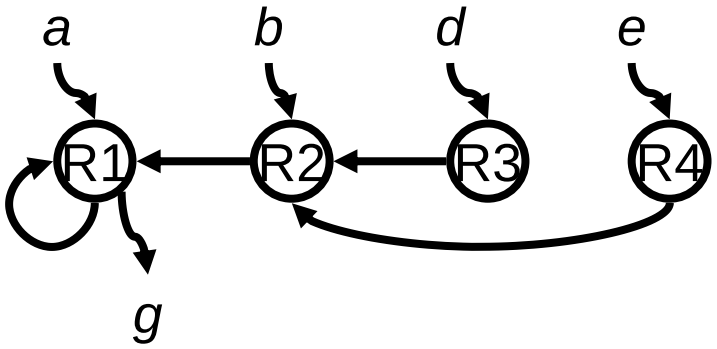
Testability Enhancement

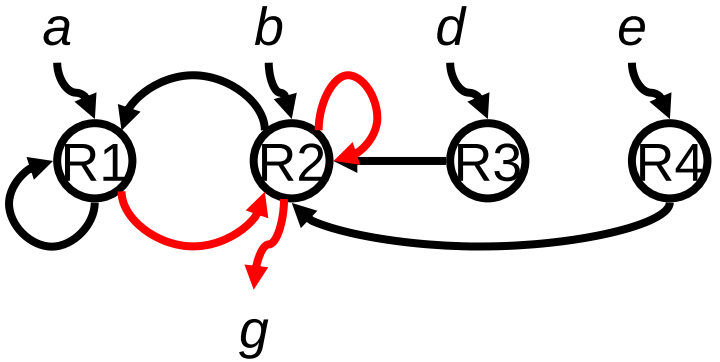
- Improve controllability and observability of registers.
  - Whenever possible, allocate a register to at least one PI or PO.
- Reduce the sequence depth between a controllable and an observable registers.

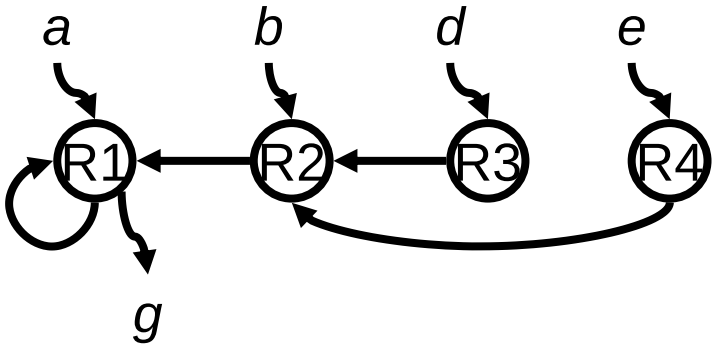
An Example

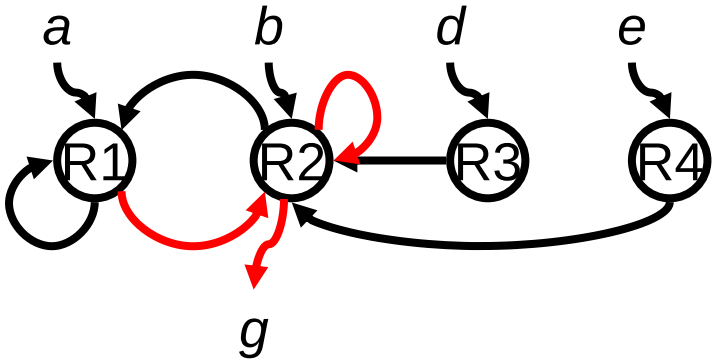






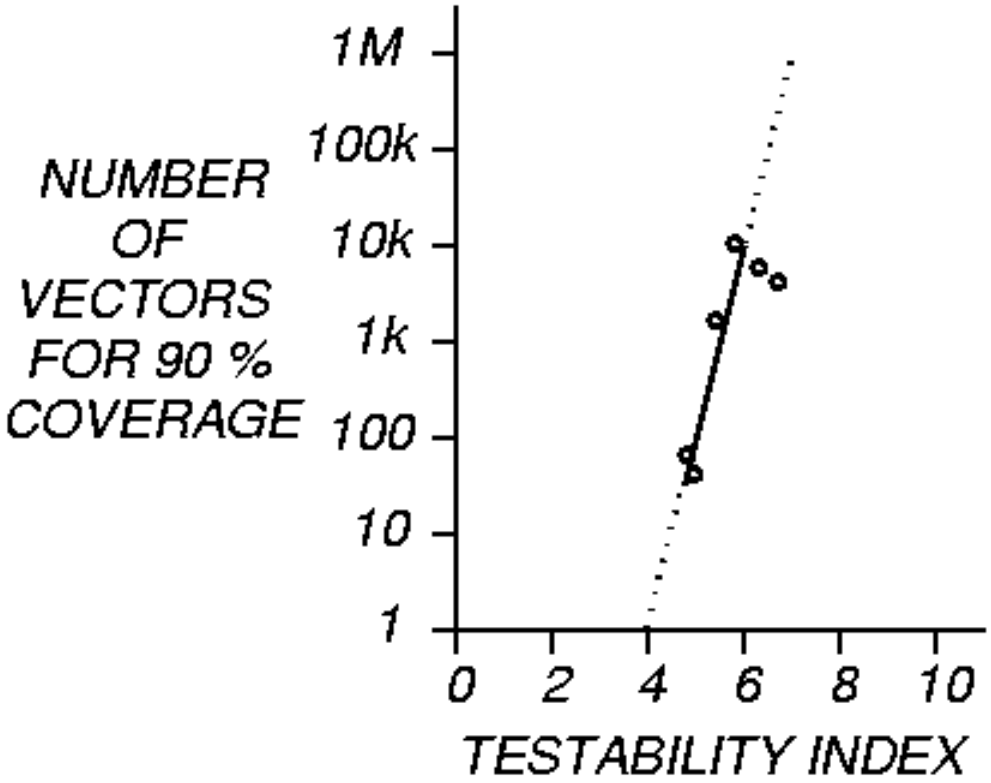






R1 → R1 : 0
R2 → R1 : 1
R3 → R1 : 2
R4 → R1 : 2

R1 → R2 : 1
R2 → R2 : 0
R3 → R2 : 1
R4 → R2 : 1



References

- [Brglez 84] F. Brglez, P. Pownall and R. Hum, "Application of testability analysis: from ATPG to critical delay path tracing," Int'l Test Conf., 1984.
- [Goldstein1979] L. H. Goldstein E. L. Thigpen, SCOAP: Sandia controllability/observability analysis program, Design Automation conference , 1979.