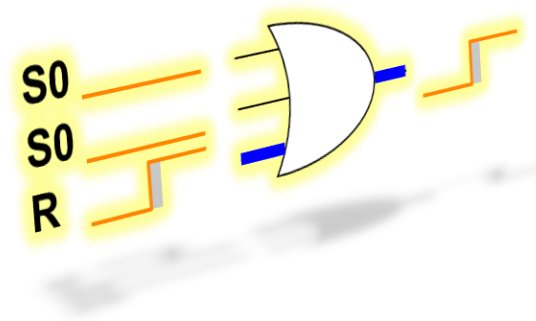
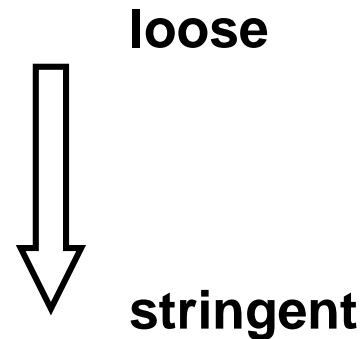


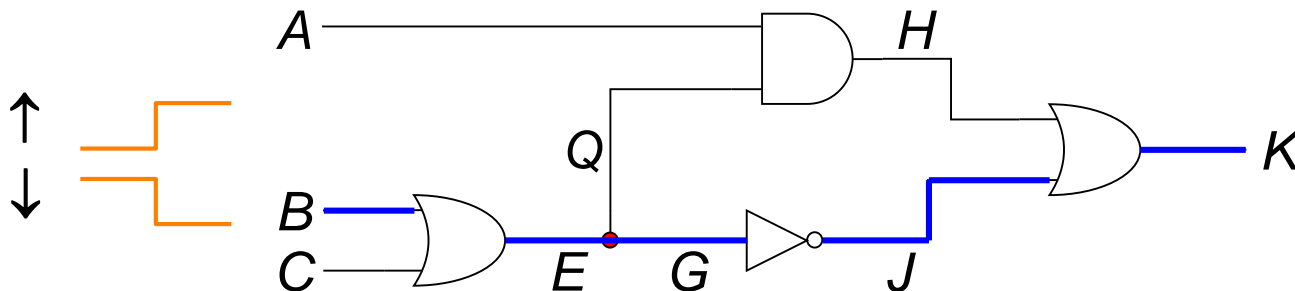
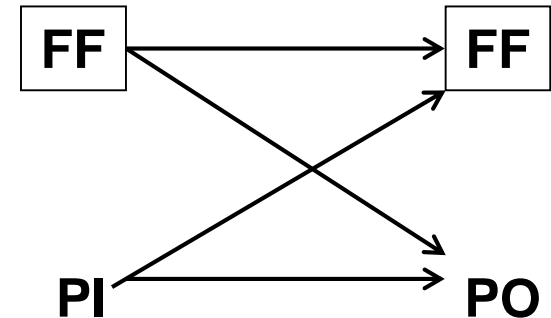
Delay Test

- Introduction and delay fault models
- Path Delay Fault
 - ◆ Path Sensitization
 - * Nonrobust
 - * Robust
 - * Hazard-free
 - ◆ Fault Simulation
 - ◆ Test Generation
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- Issues of Delay Tests* (not in exam)
- Conclusions



Path / Path Delay Fault

- What is a **path**?
 - ♦ A serial connection of combinational gates
 - * Begins from a primary input or FF/latch
 - * Ends at a primary output or FF/latch
- Two **path delay faults** for each path
 - ♦ Rising (notation \uparrow)
 - ♦ Falling (notation \downarrow)
- Example: BEGJK is a path
 - ♦ 2 PDF: \downarrow BEGJK, \uparrow BEGJK

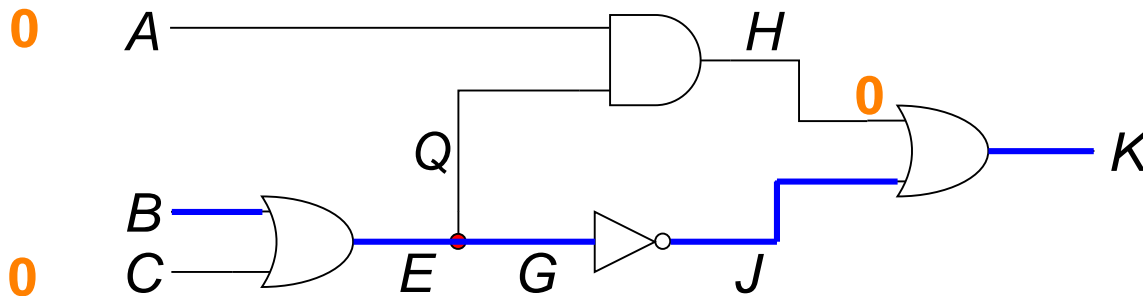


Testable Path

- A path is **testable** if a transition can propagate from input to output along the path under certain **sensitization criteria (condition)**
 - ♦ testable path is also called a **true path**
- If such a test pattern does not exist, the path is **untestable**
 - ♦ Also known as (aka.) **false path**
- Note: there are many different **sensitization criteria**
 - ♦ untestable under criterion A may be testable under criterion B

Static Sensitization Criterion

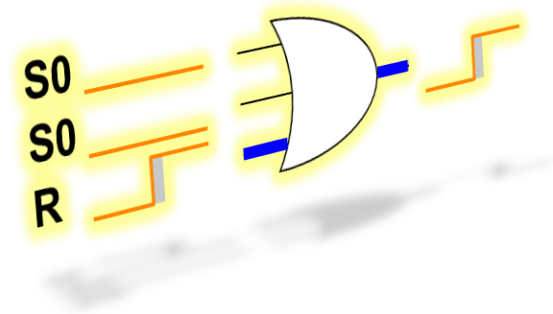
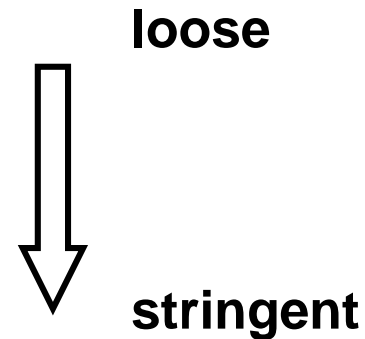
- For a given **target path**
 - ♦ **On-path** signals: on target path (aka. **on-input** to the gate)
 - ♦ **Off-path** signals: not on target path but feed gates on target path (aka. **side-input**, **off-input** to the gate)
- A path is **statically sensitized** if
 - ♦ All off-path signals assume **non-controlling** values
 - ♦ Any signal change on a statically sensitized path is observed
- Example: target path BEGJK is statically sensitized
 - ♦ BEGJK: on-path signals
 - ♦ C, H: off-path signals. They are non-controlling



- **NOTE:** static sensitization is for one single test pattern only

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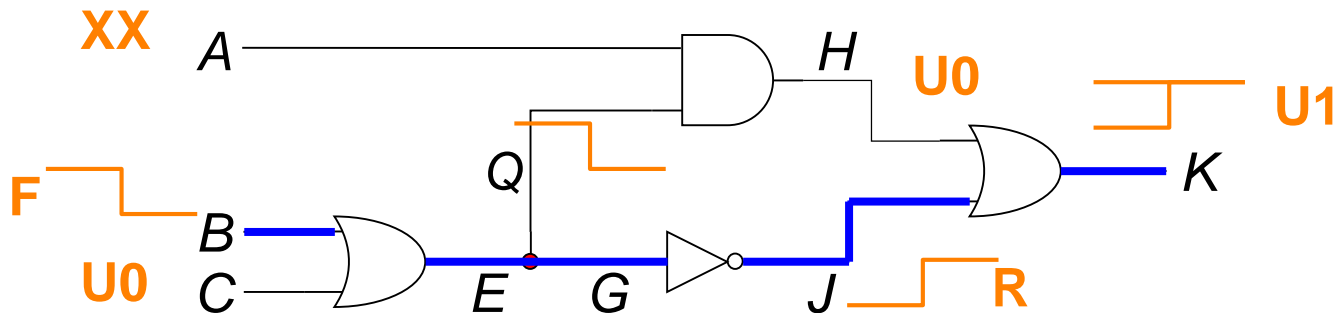


9-valued Logic

- **9-valued logic** for two-pattern test
 - ◆ R: rising $0 \rightarrow 1$
 - ◆ F: falling $1 \rightarrow 0$
 - ◆ U0: $X \rightarrow 0$
 - ◆ U1: $X \rightarrow 1$
 - ◆ S0: static zero , $0 \rightarrow 0$
 - ◆ S1: static one, $1 \rightarrow 1$
 - ◆ 0*: static 0-hazard , $0 \rightarrow 1 \rightarrow 0$
 - ◆ 1*: static 1-hazard, $1 \rightarrow 0 \rightarrow 1$
 - ◆ XX: unknown for both patterns $X \rightarrow X$
- NOTE: there are many different logic systems
 - ◆ More logic values, handles timing more accurately
 - ◆ But more difficult for ATPG

How to Sensitize Path by 2 Patterns?

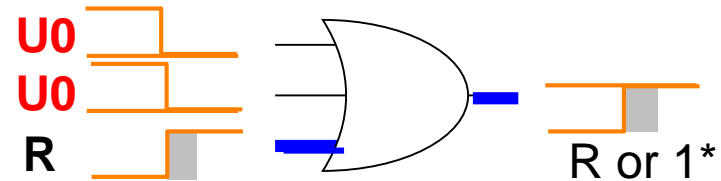
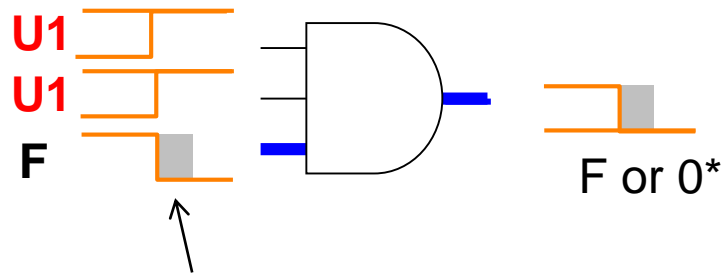
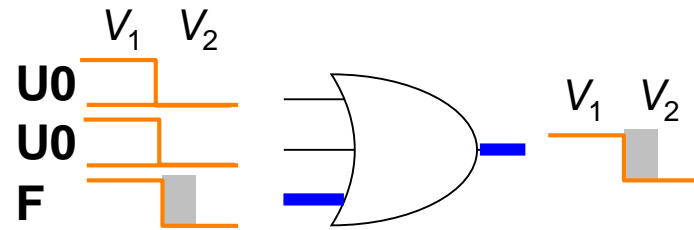
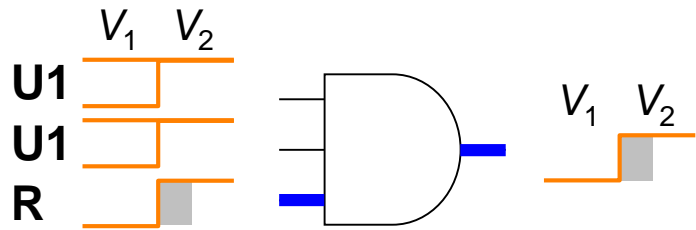
- PDF requires 2-pattern test
- How to sensitize target path in 2-pattern test?
 - ♦ Simple idea: **all off-input hold non-controlling (NC) in 2nd pattern**
- Example: PDF ↓ BEGJK
 - ♦ C is U0; H is U0



- Q: K may not have transition?
 - ♦ ANS: a non-robust test may NOT cause gate output transition
 - ♦ When A=0X, K =rising. This is called a *strong* non-robust test.
 - ♦ When A=1X, K =static-1 hazard. This is called a *weak* non-robust test. (not in exam)

Non-Robust Sensitization Criterion

- Non-robust sensitization Criterion: all off-inputs are $x \rightarrow nc$
- Example: target path in blue

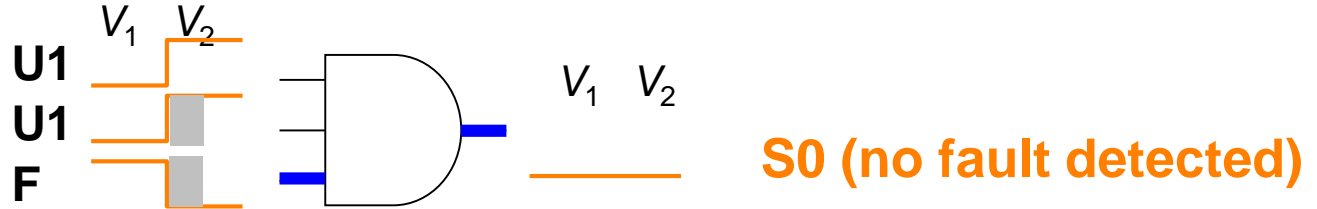


Gray area represents delay fault effect

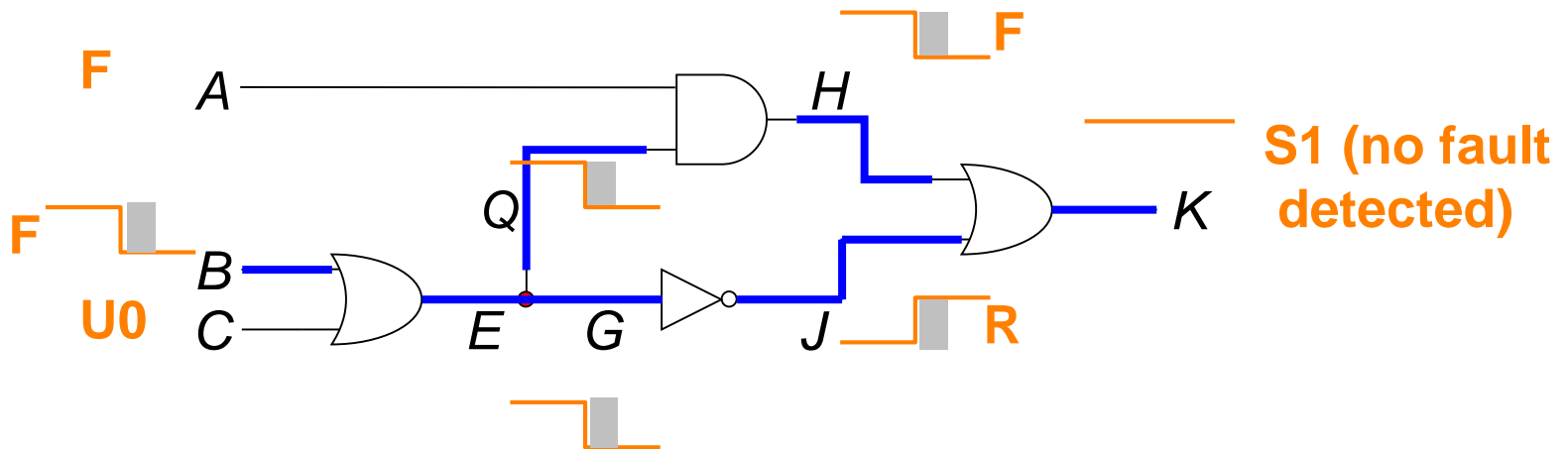
NR Sensitization: off-input is NC in 2nd pat.

Why Non-Robust?

- Non-robust path delay test **CANNOT guarantee** to detect target PDF
 - ♦ test effectiveness depends on other path delay
 - ♦ Test escape when **multiple PDF** exist simultaneously
- Example: if off-input also has delay fault, NR test is **invalidated**



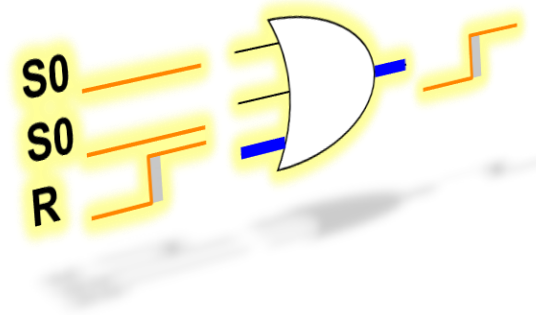
- Example 2: \downarrow BEQHK can invalidate NR test for \downarrow BEGJK



Delay Test

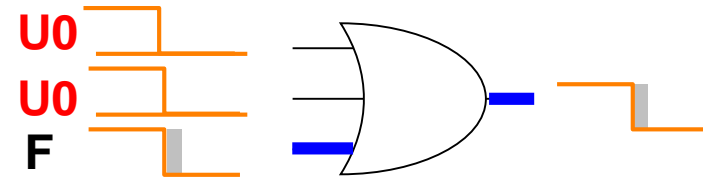
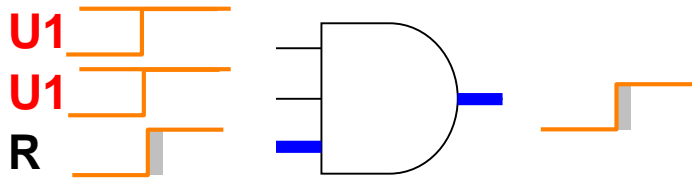
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Need more stringent sensitization criterion than NR!

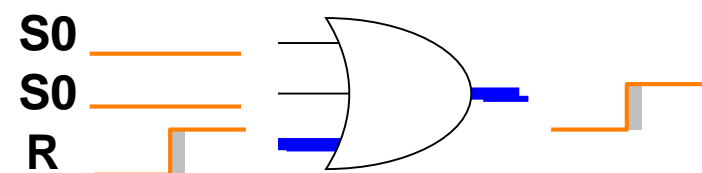
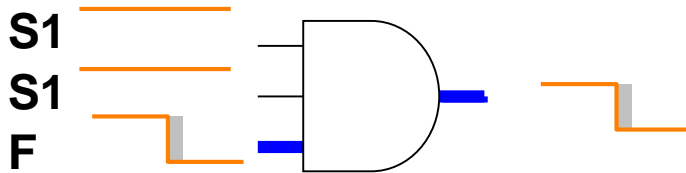


Robust Sensitization Criterion

- Idea
 - ♦ Output *cannot* change *before* the on-input change
- Robust Sensitization Criterion: (NC=*non-controlling*, C = *controlling*)
 - ♦ (1) when on-input is $C \rightarrow NC$, off-inputs $X \rightarrow NC$ (same before)



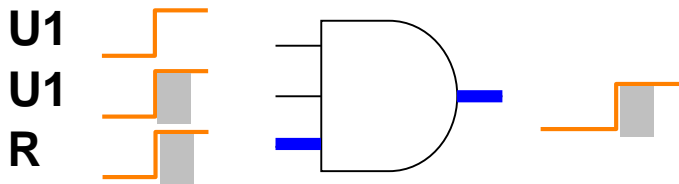
- ♦ (2) when on-input is $NC \rightarrow C$, off-inputs **MUST** remain $NC \rightarrow NC$



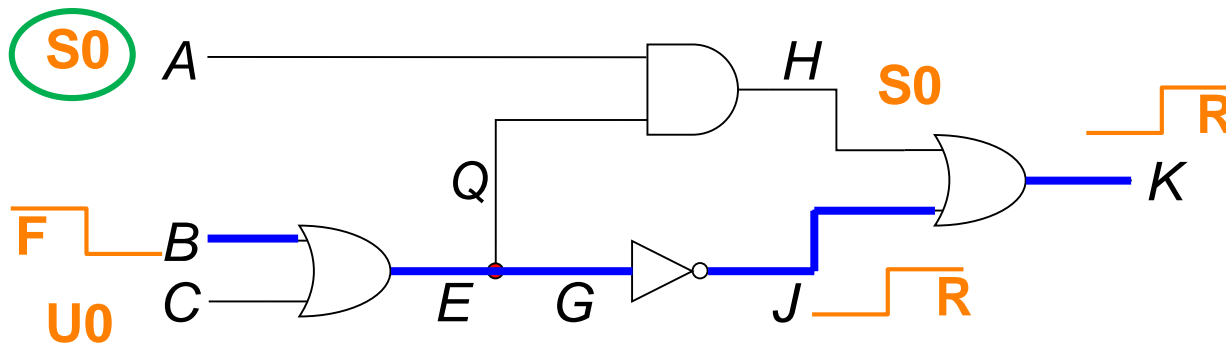
Robust: on-input $NC \rightarrow C$, off-input keep NC

Why Robust?

- A robust path delay test **guarantees** to detect target PDF,
 - ◆ regardless of other path delay
 - ◆ Because output cannot change before on-input change
- Example: even if both inputs have delay faults, still a valid test



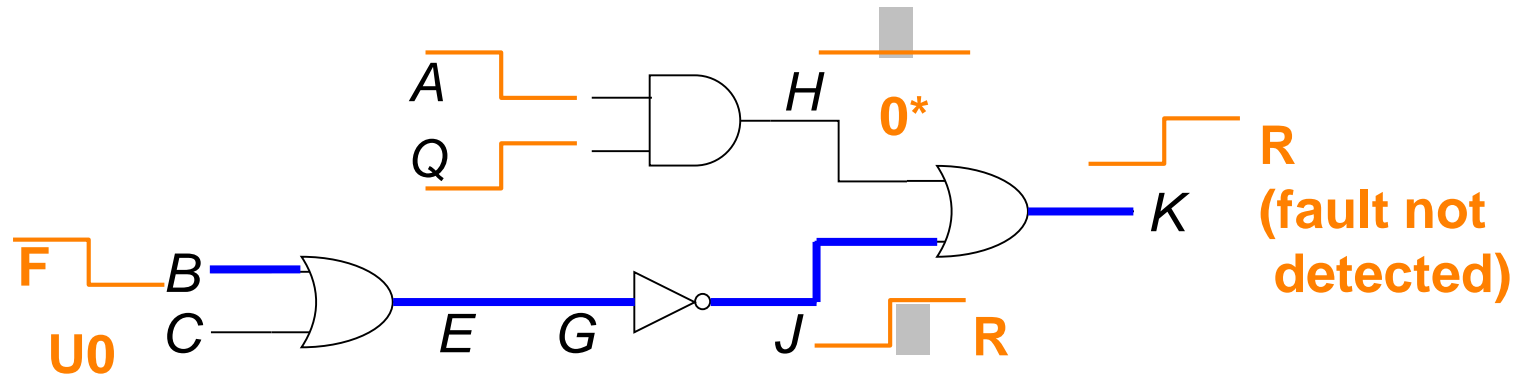
- **Example 2: PDF ↓BEQHK now can't invalidate robust test for ↓BEGJK**
 - ◆ **A is now S0, instead of XX**



Robust test has better quality than NR test

Robust Test Still not Perfect ...

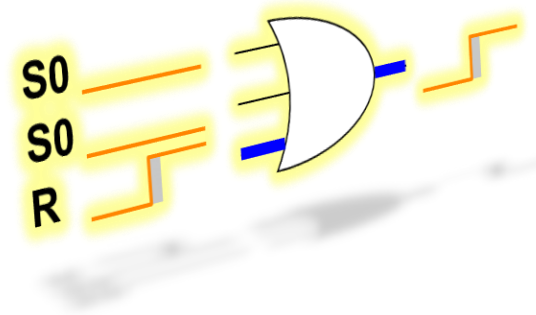
- **Hazard** can still invalidate a robust test
- Example: robust test for PDF ↓BEGJK
 - ◆ But target PDF not detected due to hazard



Delay Test

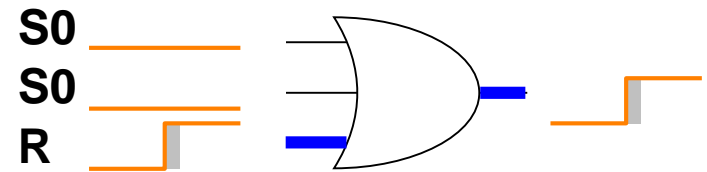
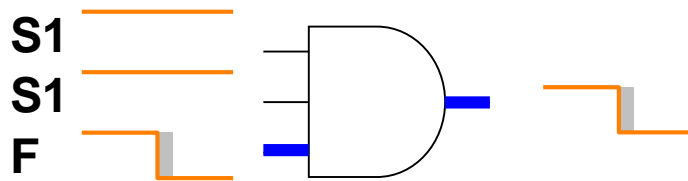
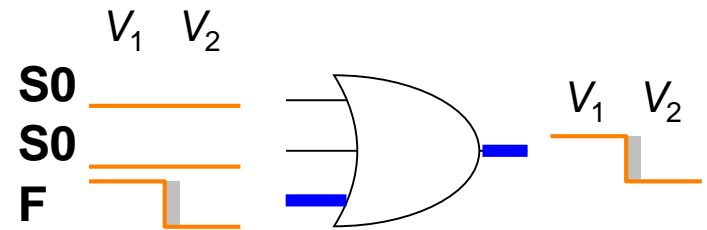
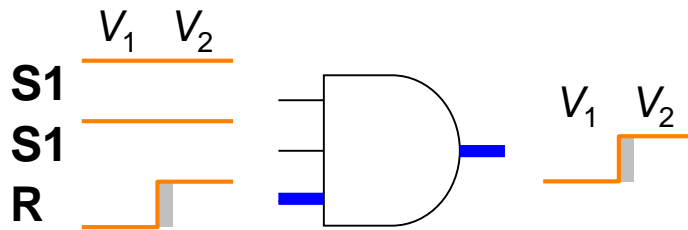
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Need more stringent sensitization criterion than robust!



Hazard-free Sensitization Criterion

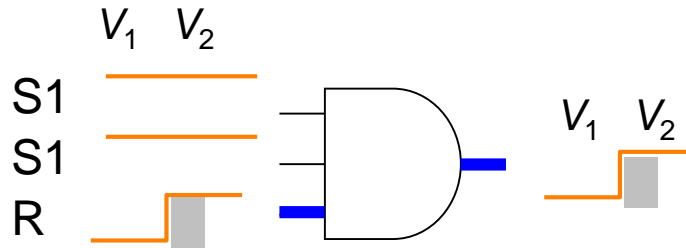
- Criterion: off-inputs are **stable non-controlling NC** \rightarrow NC
 - ♦ Regardless on-input values
- Example: target path is blue



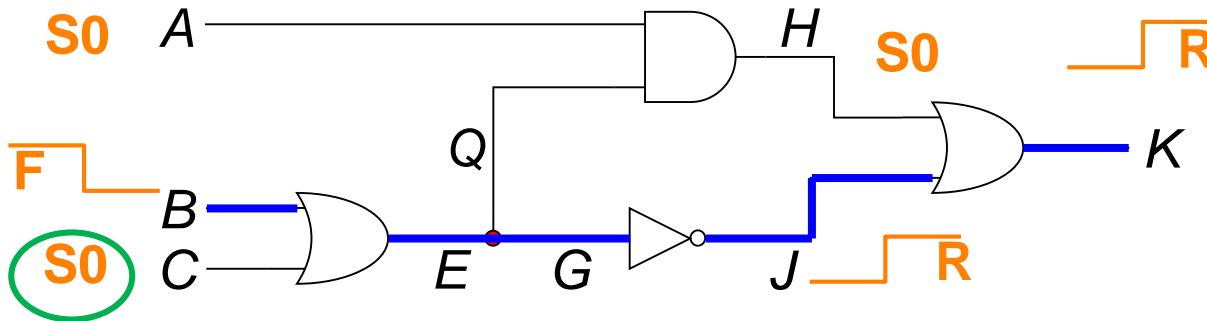
HF test requires off-inputs are stable NC

Hazard-free Path Delay Test

- **A hazard-free path delay test guarantees to detect target PDF**
 - ◆ **regardless of other PDF and hazard**
- **Example:**

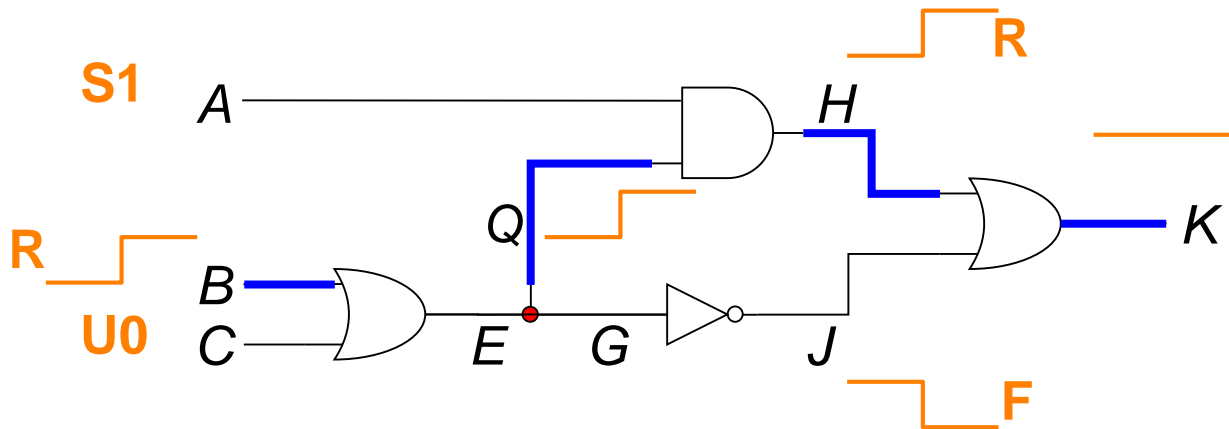


- **Example: hazard-free path delay test for PDF ↓BEGJK**
 - ◆ **C is now S0, instead of U0**



Hazard-free Test is Good, but...

- Only a small number of PDF have hazard-free test
- Example: no hazard-free test for PDF \downarrow BEQHK



HF tests are good but very few

18

The diagram shows a logic circuit with the following components and connections:

- AND Gate:** Inputs are A and Q . Output is H .
- OR Gate:** Inputs are B and C . Output is E .
- NOT Gate:** Input is E . Output is J .
- Final OR Gate:** Inputs are H and J . Output is K .

Waveforms are provided for inputs A , B , C and outputs H , K . The waveform for Q is also shown, representing the state of the circuit at each time step.

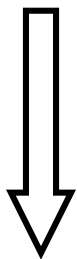
[illegible]

3 Types Path Delay Tests

- A PDF is *hazard-free testable* if a test exists such that
 - ◆ all gates on that path are hazard-free sensitized
 - ◆ If no such test, it is *hazard-free untestable*
- A PDF is *robustly testable* if a test exists such that
 - ◆ all gates on that path are robustly (including hazard-free) sensitized
 - ◆ If no such test, it is *robustly untestable*
- A PDF is *non-robustly testable* if a test exists such that
 - ◆ at least one gates on the path is non-robustly sensitized
 - ◆ the other gates on the path are robustly/hazard-free sensitized
 - ◆ If no such test, it is *non-robustly untestable*

Summary

loose

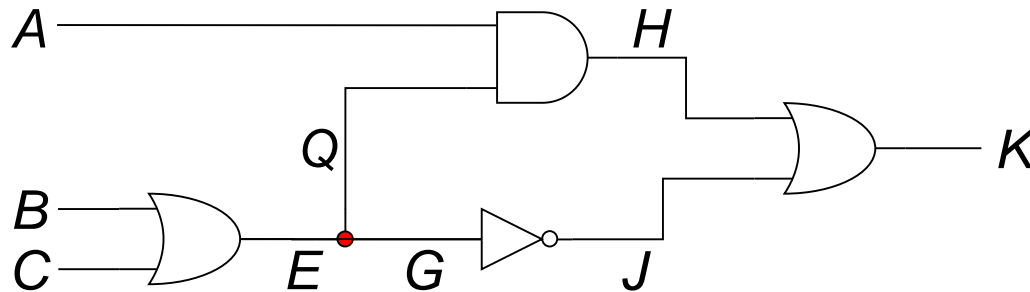


Type	On-input	Off-input	good👍	bad👎
Non-robust	C → NC NC → C	X → NC X → NC	Easy to find	Invalidate by other PDF
Robust	C → NC NC → C	X → NC NC → NC	Effective even other PDF	Invalidated by hazard Few
Hazard-free	C → NC NC → C	NC → NC NC → NC	Effective	Very few

stringent

FFT

- Q1: How many PDF in this circuit?
- Q2: Please show if $\uparrow\text{BEQHK}$ is non-robust, robust or HF testable



PDF	Non-robustly Testable?	Robustly testable?	Hazard-free testable
$\downarrow\text{BEGJK}$	Y	Y	Y
$\uparrow\text{BEQHK}$			

FFT2

- Q: How can we detect fault if output K is S1?

