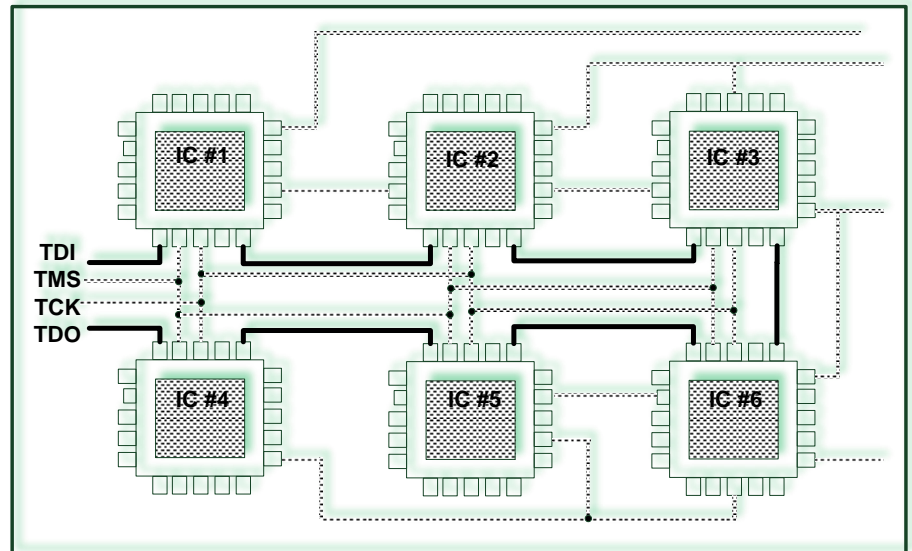


# DFT – Part 2

- Introduction
- JTAG Architecture and Components
- **JTAG Instructions**
  - ◆ Mandatory Instructions
  - ◆ Optional Instructions
- Conclusion



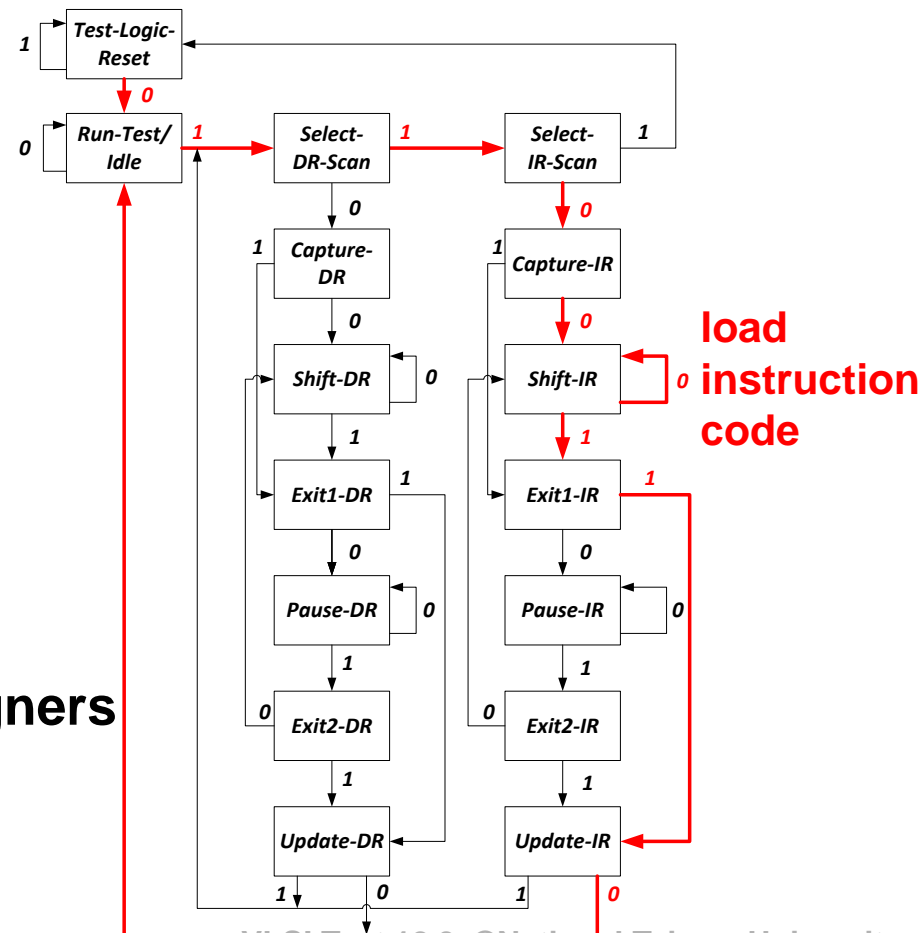
# JTAG Instructions

- Three Mandatory instructions: must implement
- Others are optional: up to designer's decision

Instruction	M/O
<b>EXTEST</b>	<b>Mandatory</b>
<b>BYPASS</b>	<b>Mandatory</b>
<b>SAMPLE / PRELOAD</b>	<b>Mandatory</b>
<b>INTTEST</b>	<b>Optional</b>
<b>RUNBIST</b>	<b>Optional</b>
<b>CLAMP</b>	<b>Optional</b>
<b>IDCODE</b>	<b>Optional</b>
<b>USERCODE</b>	<b>Optional</b>
<b>HIGHZ</b>	<b>Optional</b>

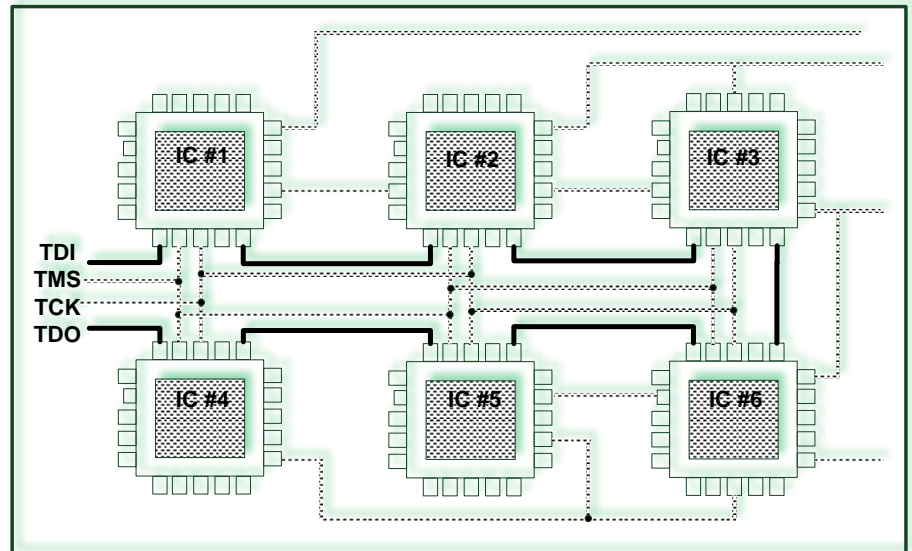
# How to Load Instruction?

- Apply **TMS** sequence
  - ♦ **Initialize JTAG**: 1→1→1→1→1
  - ♦ **Load instruction**: 0→1→1→0→0→0.....0→1→1→0
- Number of zeros =
  - ♦ **Total length of Instruct. Reg.**
  - ♦ of all chips on board
- **Instruction code** is
  - ♦ shifted in via **TDI**
- JTAG specified Instruction codes
  - ♦ EXTEST=000...(all zeros)
  - ♦ BYPASS=111...(all ones)
  - ♦ Other codes specified by designers



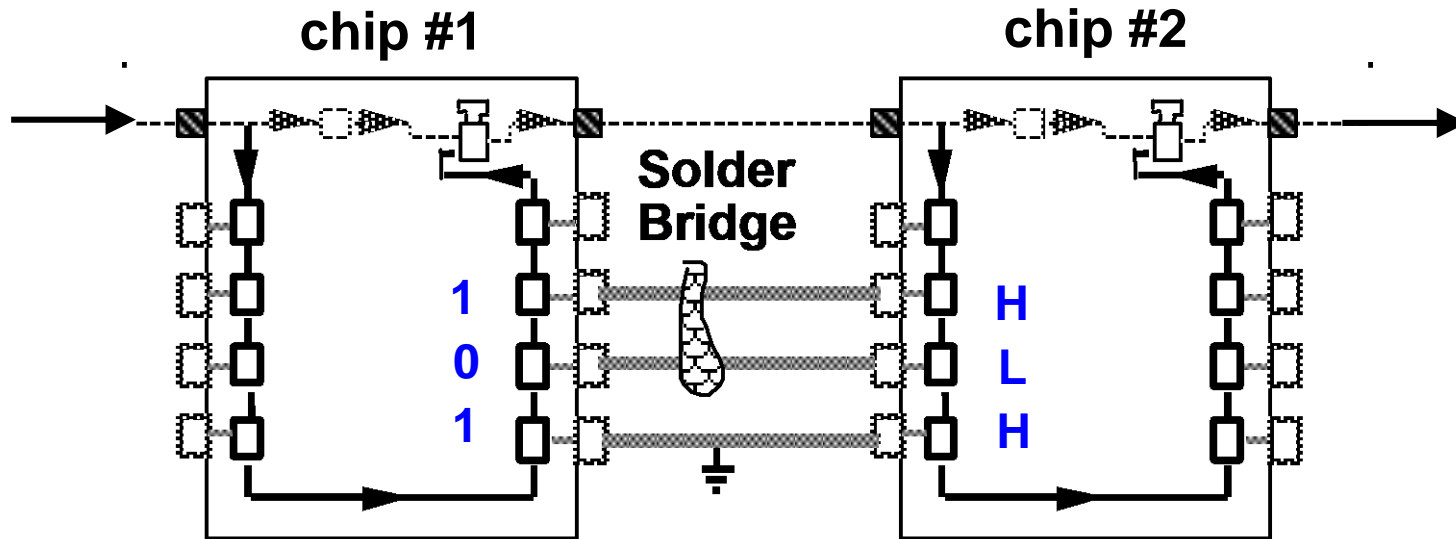
# DFT – Part 2

- Introduction
- JTAG Architecture and Components
- **JTAG Instructions**
  - ◆ **Mandatory Instructions**
    - \* **EXTEST**
    - \* **BYPASS**
    - \* **SAMPLE/PRELOAD**
  - ◆ **Optional Instructions**
- Conclusion



# EXTEST(1)

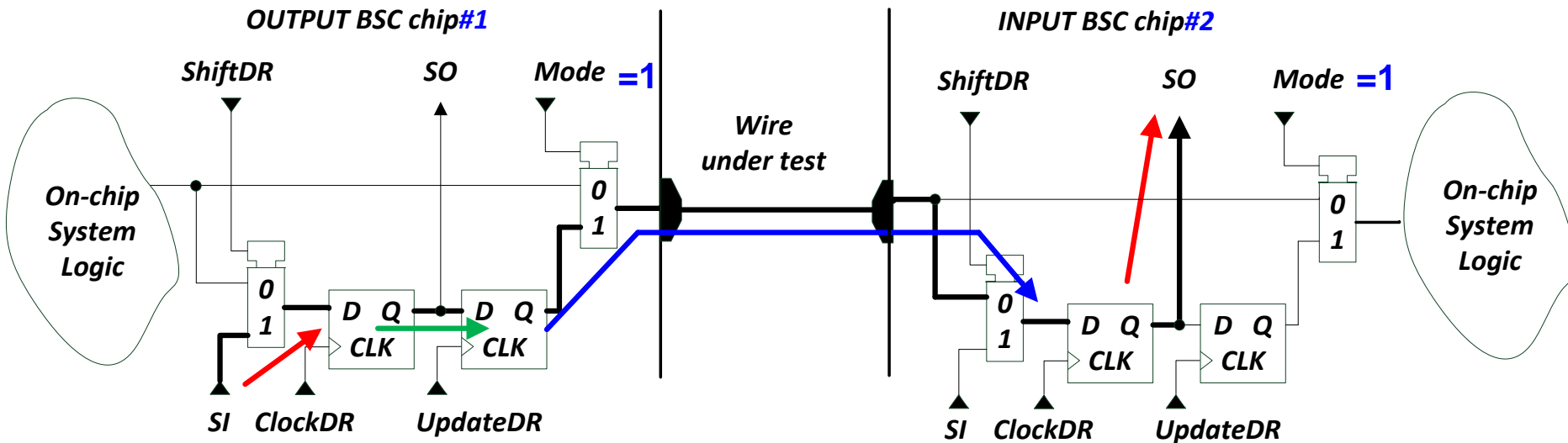
- Purpose: External test
  - ◆ Test **external** off-chip wire interconnections among chips



**EXTEST Test Wires Among Chips**

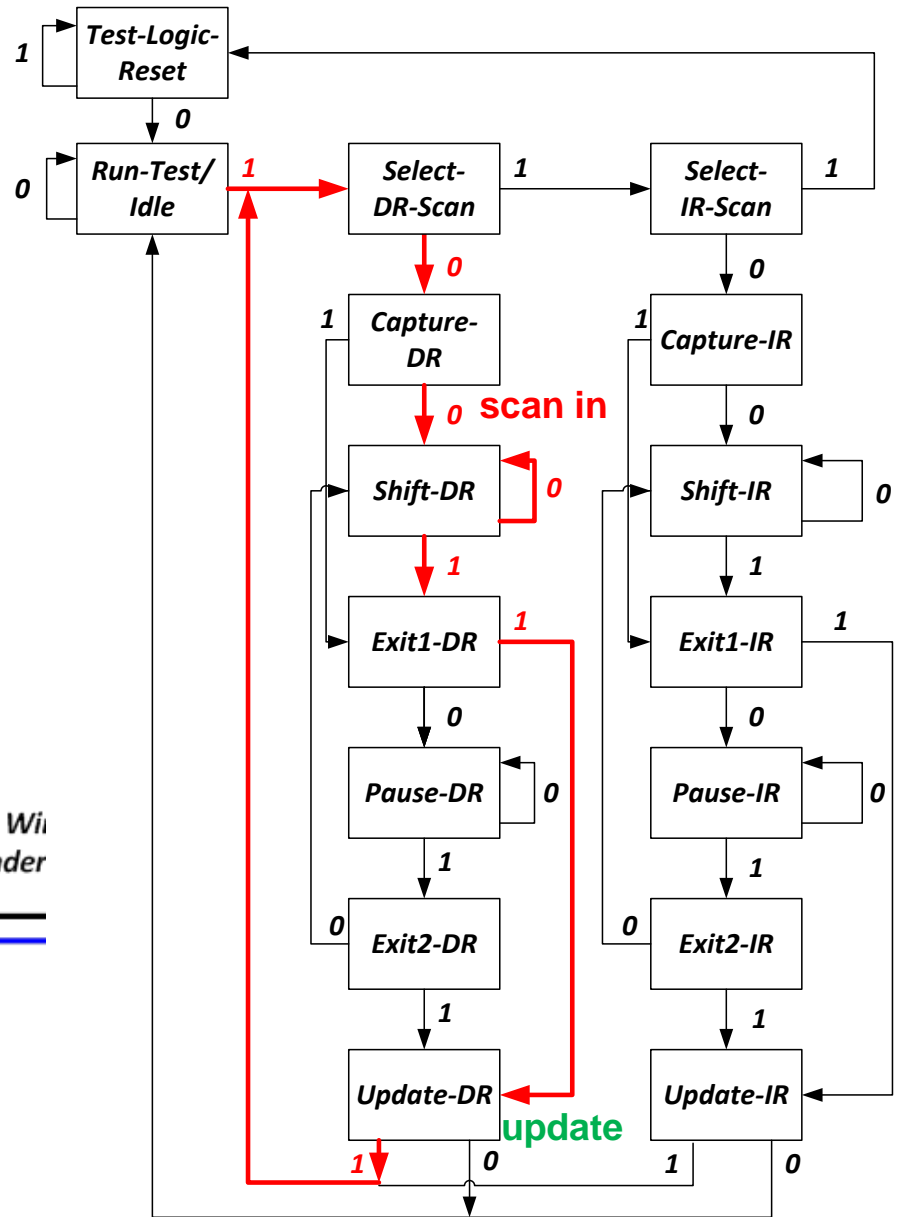
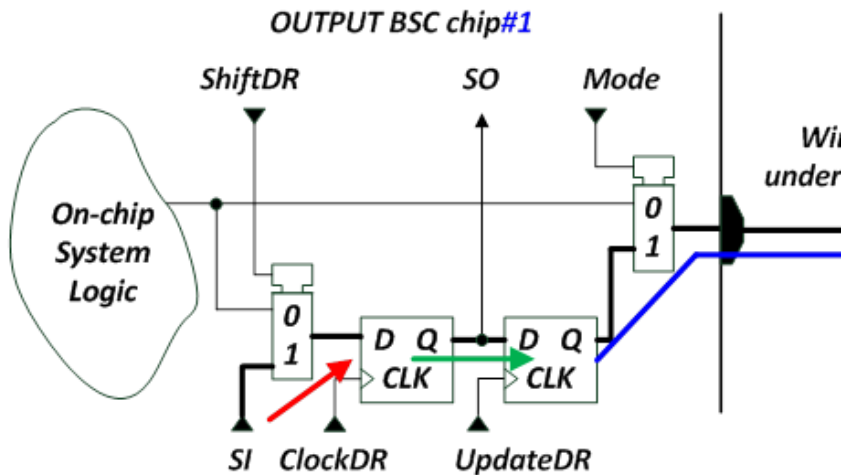
# EXTEST (2)

- Step1: **Scan in chip#1**: shiftDR=1, clockDR...
- Step2: **Update chip#1**: updateDR
- Step3: **Capture chip#2**: shiftDR=0, clockDR
- Step4: **Scan out chip#2**: shiftDR=1, clockDR...
- Mode always = 1



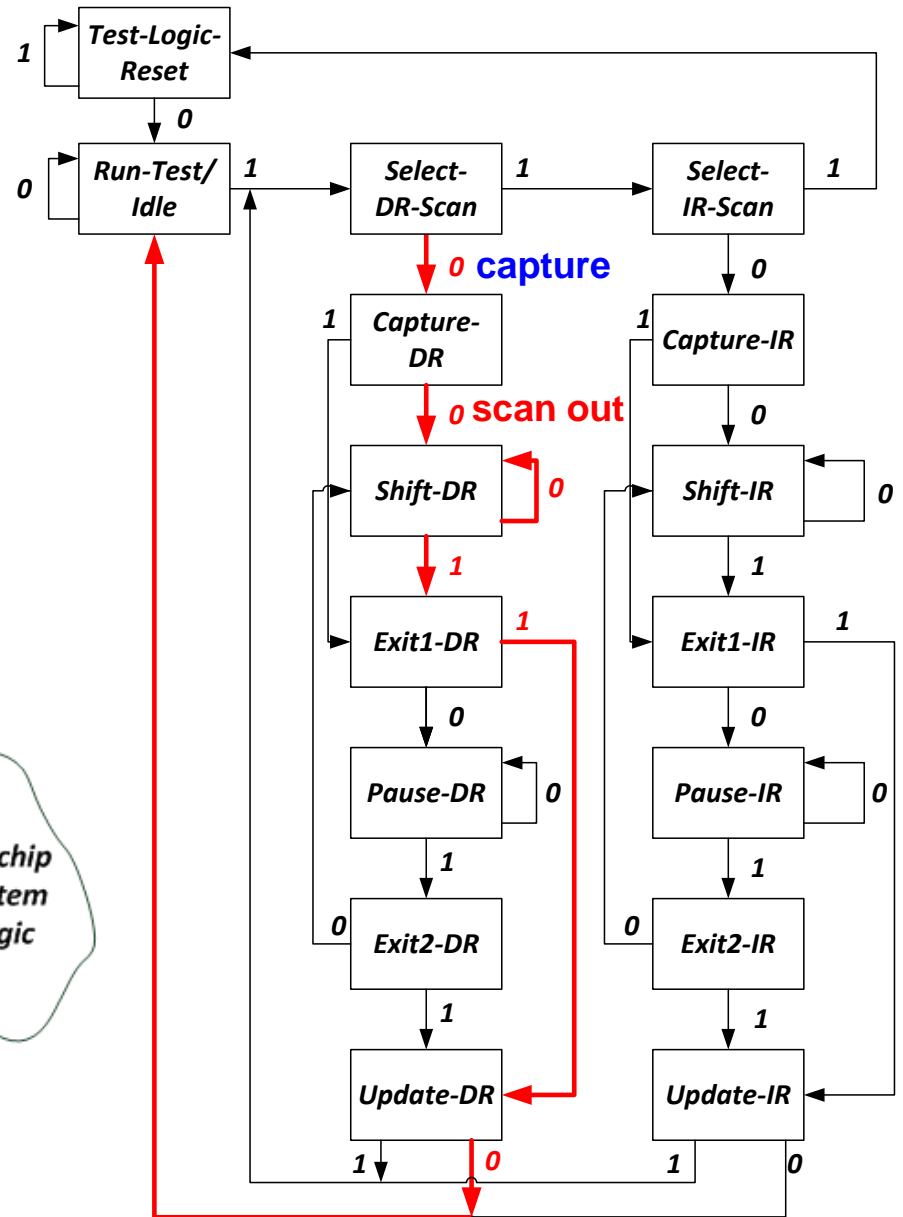
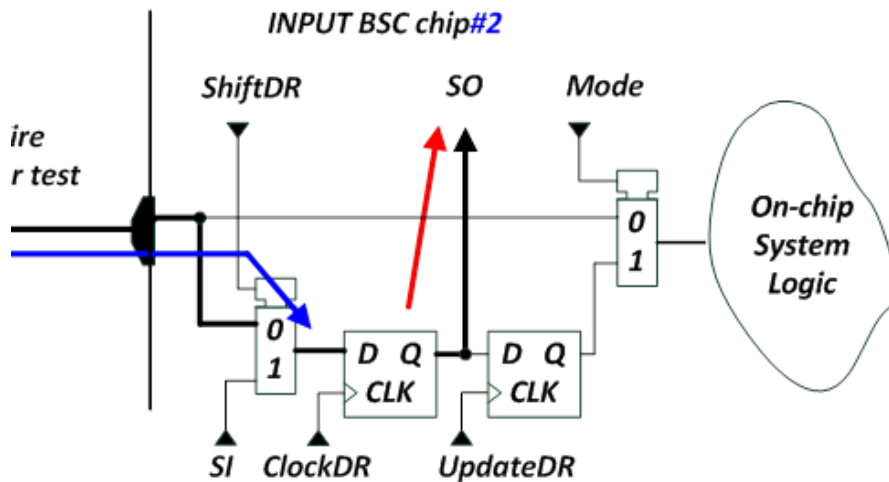
# BSC and TAP Controller (1)

- (after instruction code loaded)
- $TMS = 1 \rightarrow 0 \rightarrow 0 \rightarrow 0 \dots 0 \rightarrow 1 \rightarrow 1 \rightarrow 1$
- Number of zeros =
  - ◆ Total length of Data Reg.
  - ◆ NOTE: BSR, BR



# BSC and TAP Controller (2)

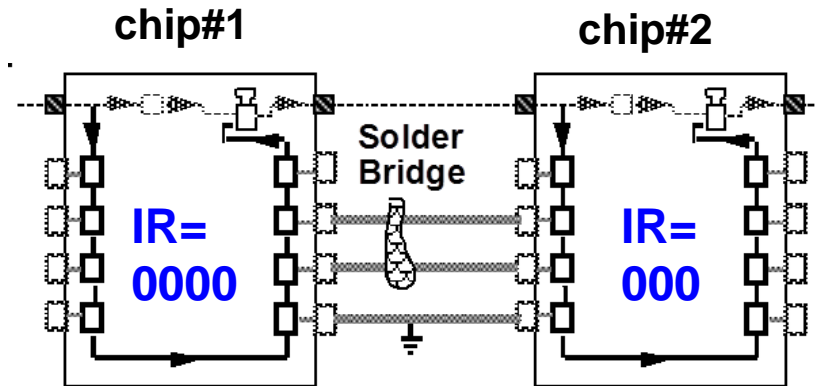
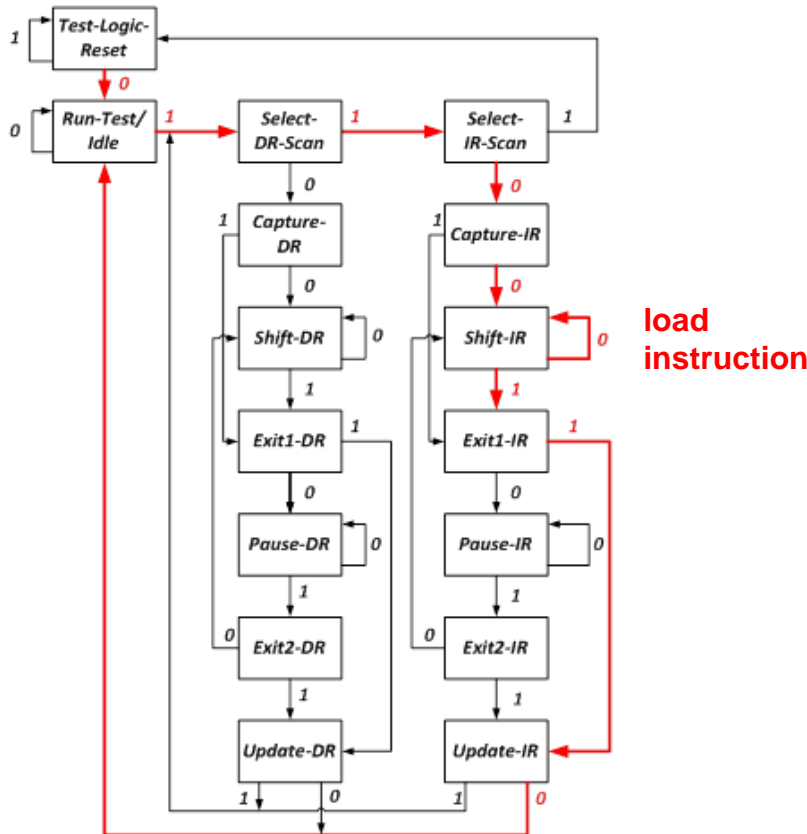
- TMS = 0→0→0...0→1→1→0





# Load Instruction

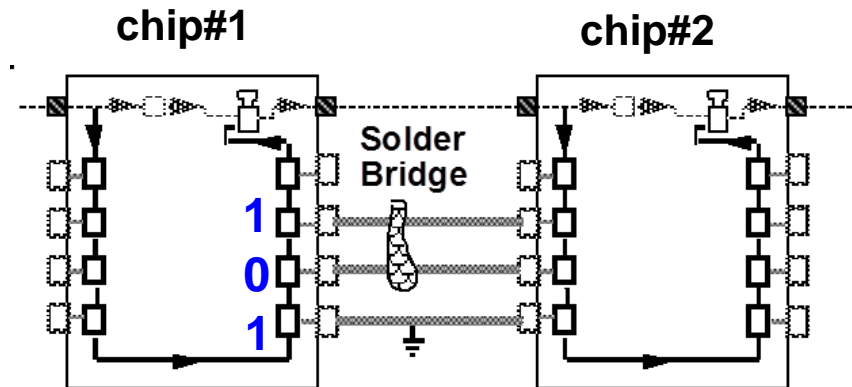
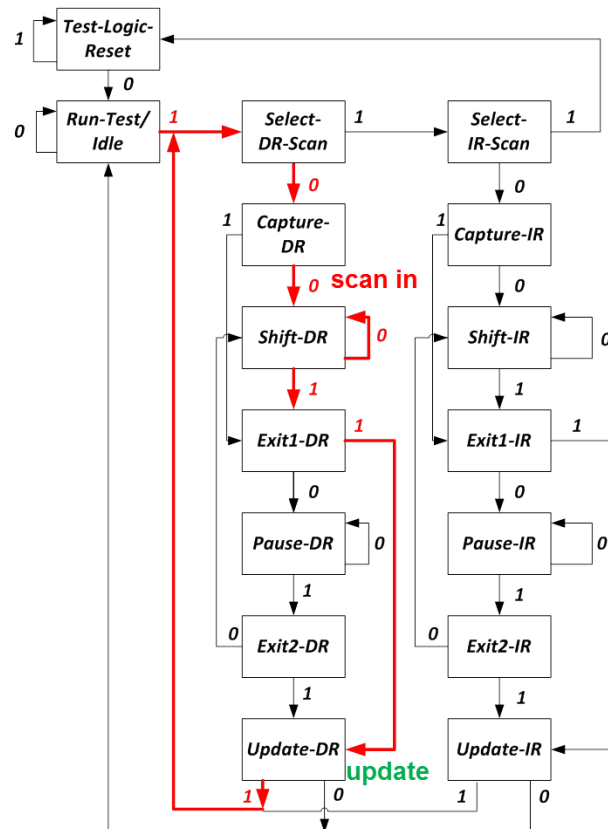
	Initialize TAP		load instruction	
TMS	11111	01100*	000 0000**	110
TDI			000 0000	
TDO				
Final state	test logic-reset		Shift-IR	Run-test/Idle



- \* left bit shifted in first
- \*\*chip#1 IR has 4 bits
- chip#2 IR has 3 bits
- total length of IR = 7

# Example (2/3) Scan-In-Update

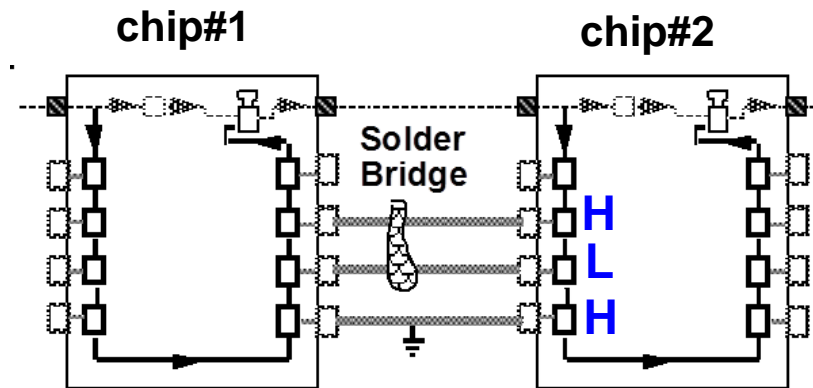
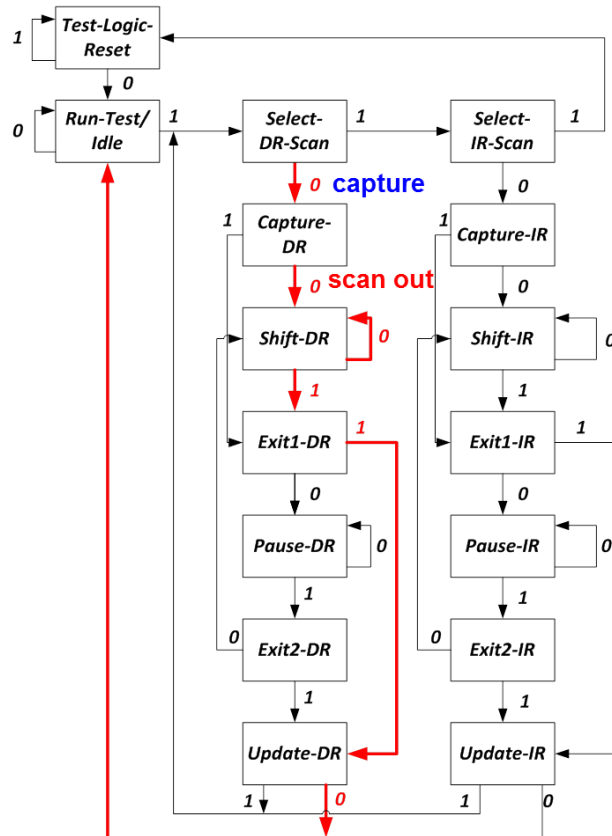
		Scan in		Update	
TMS	100	0000 0000 0000 0000	1	1	1
TDI		XXXX XXXX X <b>101</b> XXXX *			
TDO					
Final state		Shift-DR		update-DR	select-DR-scan



\* left bit shifted in first  
chip#1 DR has 8 bits  
chip#2 DR has 8 bits  
total length of DR = **16**

# Example (3/3) Capture-Scan-Out

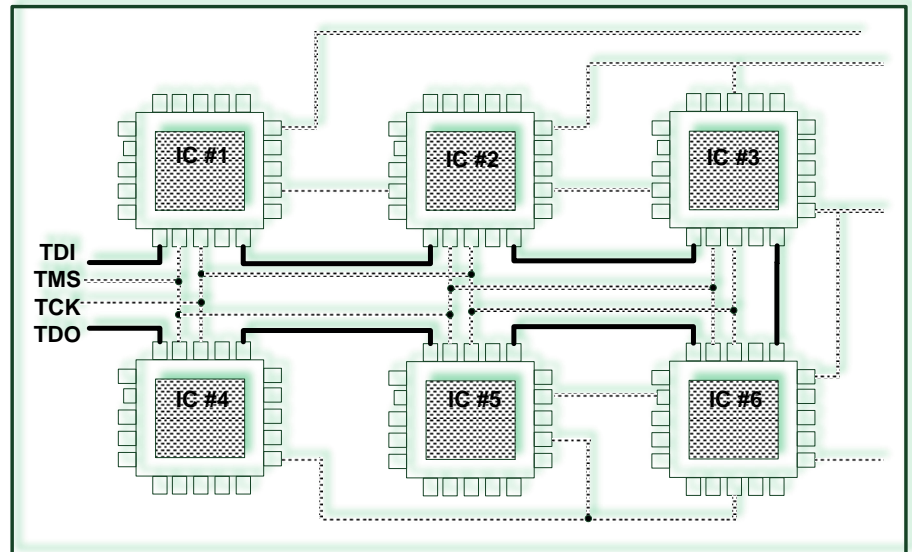
	Capture		Scan out	
<b>TMS</b>	0	0	0000 0000 0000 0000	110
<b>TDI</b>				
<b>TDO</b>			XXXX <b>HLH</b> X XXXX XXXX *	
<b>Final state</b>	Capture-DR		Shift-DR	run-test/Idle



\* left bit shifted out first  
 chip#1 DR has 8 bits  
 chip#2 DR has 8 bits  
 total length of DR = 16

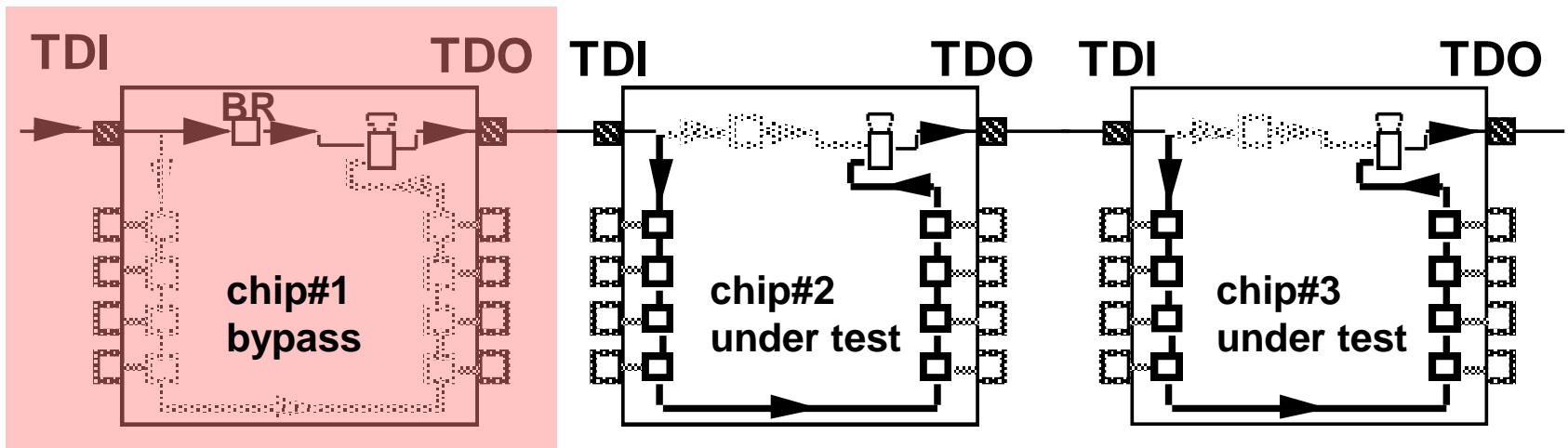
# DFT – Part 2

- Introduction
- JTAG Architecture and Components
- JTAG Instructions
  - ◆ Mandatory Instructions
    - \* **EXTEST**
    - \* **BYPASS**
    - \* **SAMPLE/PRELOAD**
  - ◆ Optional Instructions
- Conclusion



# Bypass Instruction

- Purpose: bypass scan data from TDI to TDO of a chip
  - ♦ Through **bypass register (BR, one bit)**
- Example:
  - ♦ Go through chip#1: 24 clocks
  - ♦ Bypass chip#1:  $1+8+8=17$  clocks



**Bypass Saves Test Time**

# Quiz

**Q: Suppose we add chip#1 to our board. We want to apply EXTEST to chip#2 and chip#3. Please modify TMS/TDI/TDO sequence to bypass chip#1.**

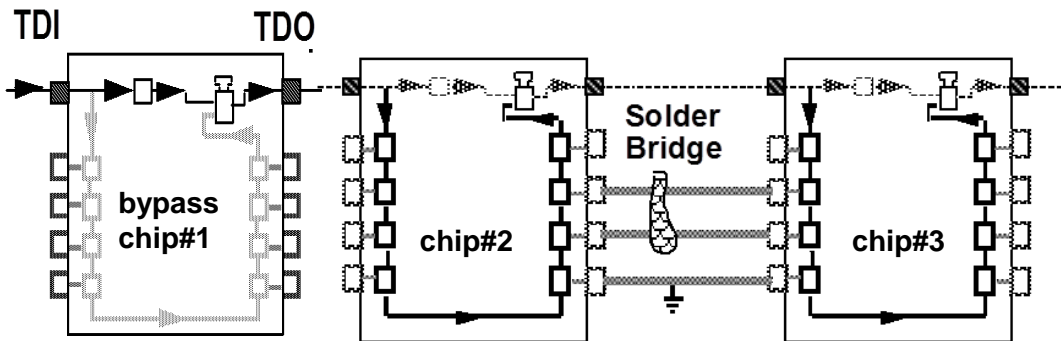
**NOTE:**

**BYPASS instruction code for chip#1 = '11'**  
**EXTEST instruction code '000' and '0000'**

	Init. TAP		load instruction	
TMS	11111	01100	000 0000	110
TDI			000 0000	
TDO				
state	reset		Shift-IR	Idle

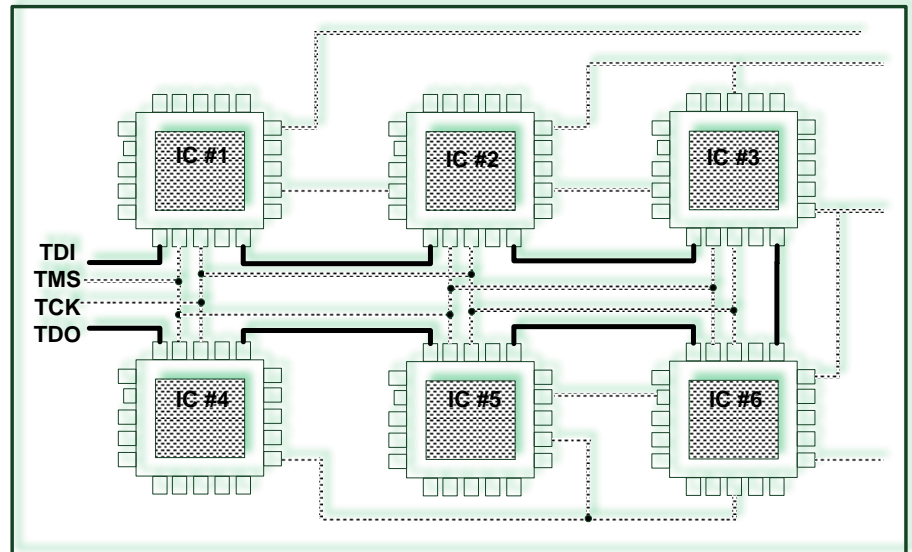
	Scan in	update
100	0000 0000 0000 0000	111
	xxxx xxxx x101 xxxx	
	Shift-DR	

Capture	Scan out	
00	0000 0000 0000 0000	110
	xxxx HLHx xxxx xxxx	
Capture-DR	Shift-DR	Idle



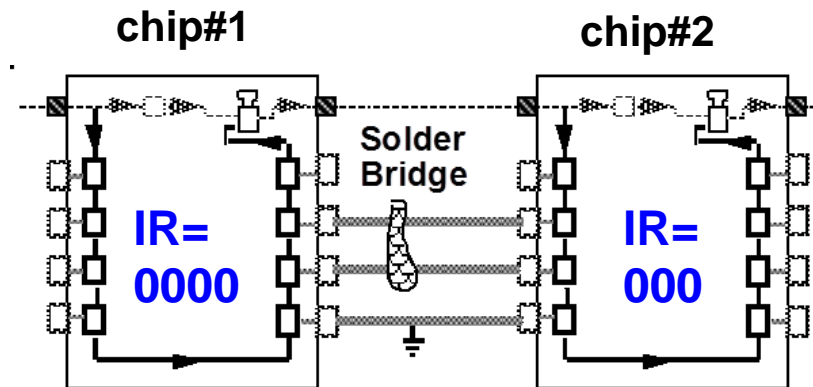
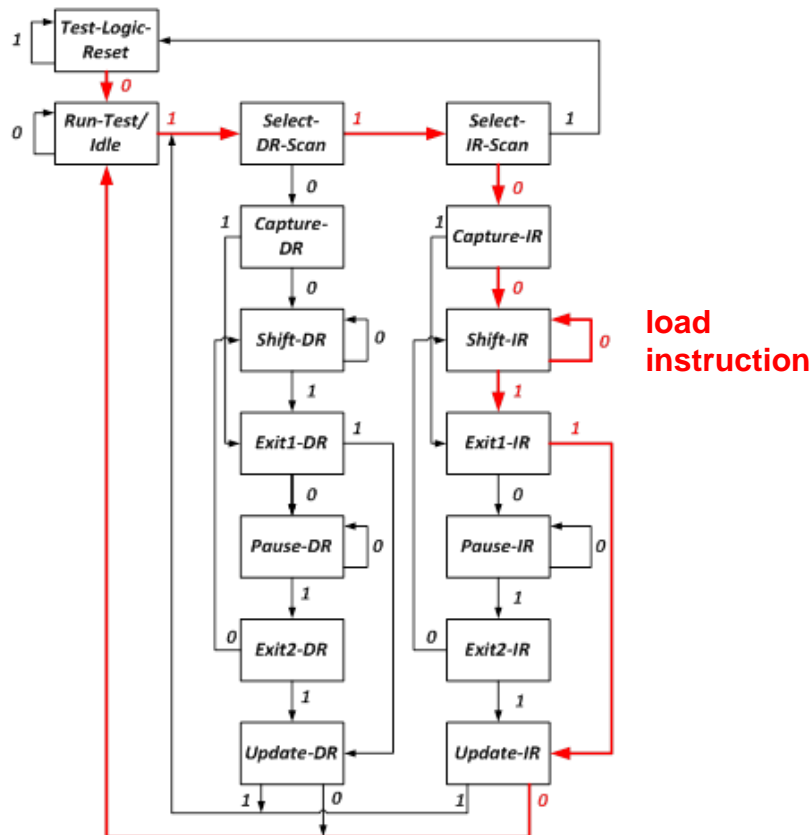
# Summary

- Two mandatory instructions
  - ◆ **EXTEST** (000...0)
    - \* Test wires among chips
    - \* scan-in, update, capture, scan-out
  - ◆ **BYPASS** (111...1)
    - \* Bypass chips to save test time



# FFT: Why Different IR Lengths?

	Initialize TAP		load instruction	
<b>TMS</b>	11111	01100*	000 0000**	110
<b>TDI</b>			<b>000 0000</b>	
<b>TDO</b>				
<b>Final state</b>	test logic-reset		Shift-IR	Run-test/Idle



- \* left bit shifted in first
- \*\*chip#1 IR has 4 bits  
chip#2 IR has 3 bits  
total length of IR = 7