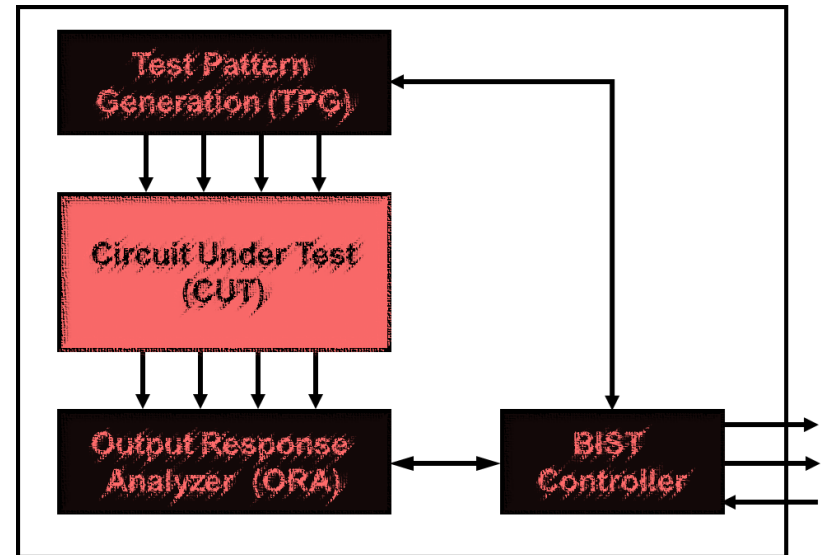


# BIST Part 2

- Output Response Analysis
- BIST Architecture
  - ◆ Test Per Clock
    - \* BILBO (1979)
  - ◆ Test Per Scan
    - \* STUMPS (IBM, 1982)
- Issues with BIST
- Conclusions



# BIST Architectures [McCluskey 85]

- Classified by hardware
  - ◆ *Separate BIST*
    - \* TPG/ORA outside of CUT
  - ◆ *Embedded BIST*
    - \* Reuse CUT's FF/latches as TPG/ORA
- Classified by clocking scheme
  - ◆ *Test-per-Clock*
    - \* Apply a test every clock cycle
  - ◆ *Test-per-Scan*
    - \* Apply a test in between scan in/out

# Test Per Clock – Combinational CUT

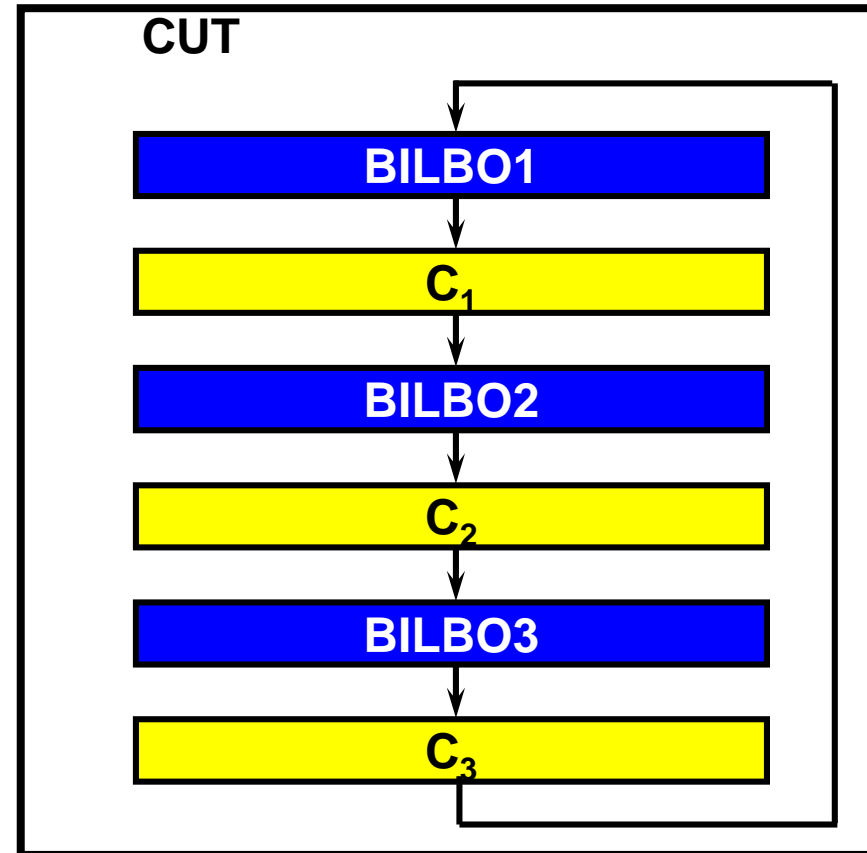
- Separate BIST
- Test per clock
  - ♦ At each clock: apply a test pattern, observe output



**How about Sequential CUT?**

# Test Per Clock – Sequential CUT

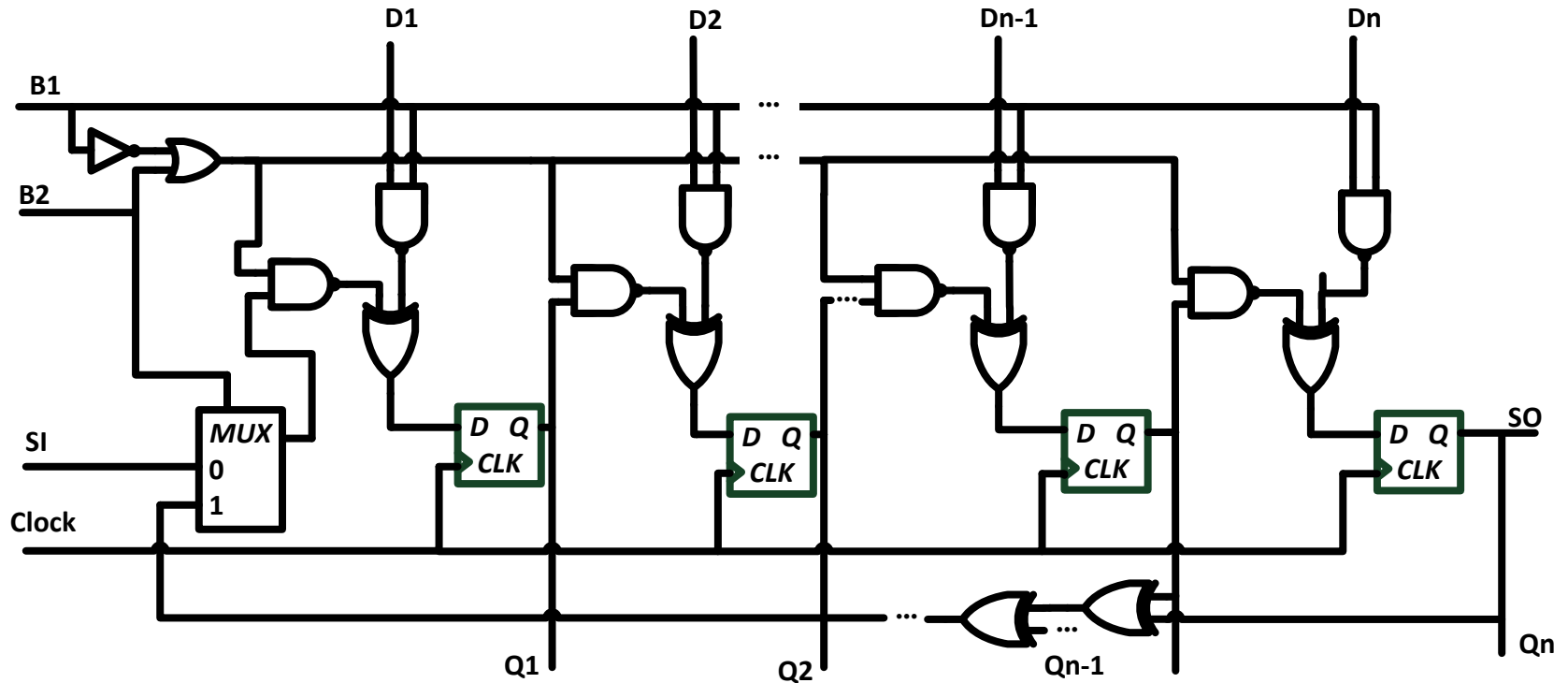
- **BILBO = Built-in Logic Block Observer** [Könemann 79]
  - ♦ Serve as TPG and ORA
- When testing C1
  - ♦ BILBO1 is TPG, BILBO2 is ORA
- When testing C2
  - ♦ BILBO2 is TPG, BILBO3 is ORA
- When testing C3
  - ♦ BILBO3 is TPG; BILBO1 is ORA
- Embedded BIST
  - ♦ Reuse CUT's FF as BILBO



Yellow blocks are comb. logic

# Built-in Logic Block Observer, BILBO

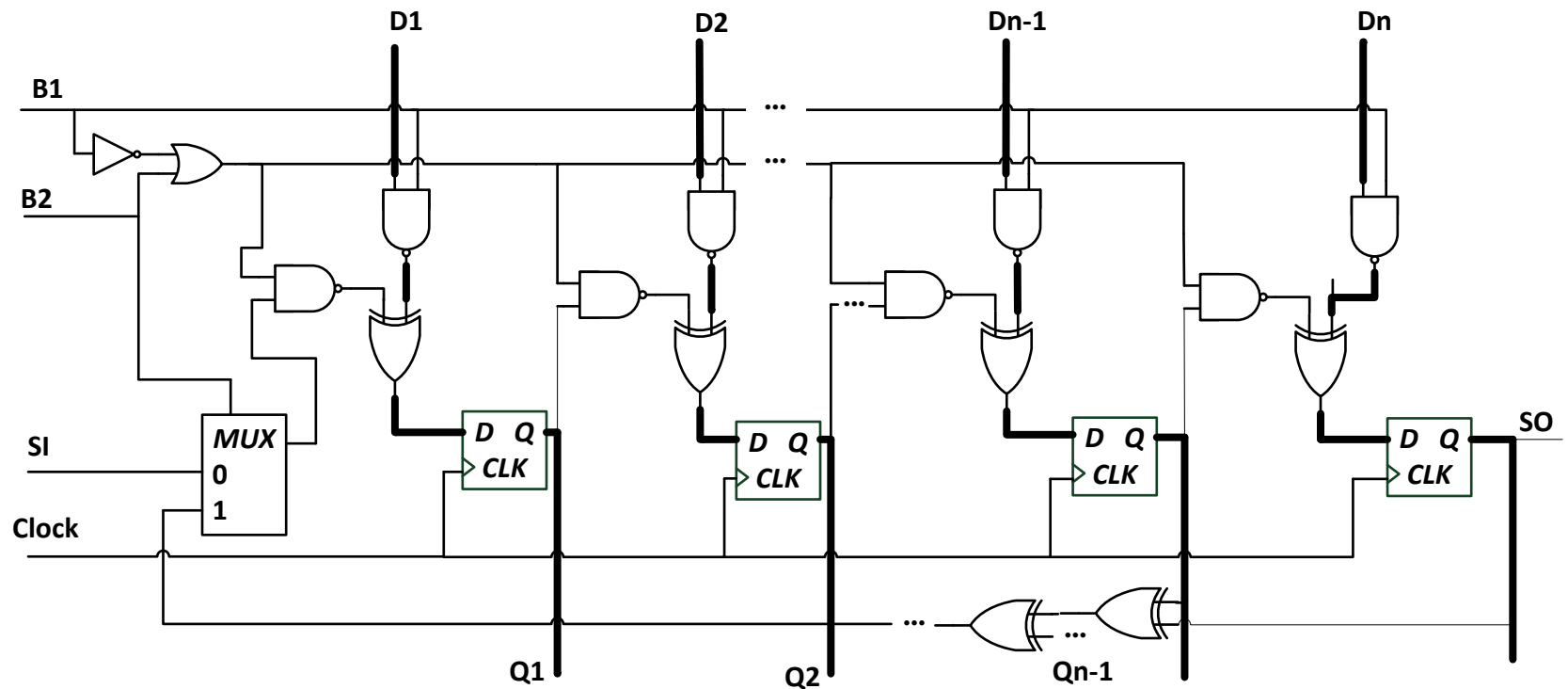
- $B_1$   $B_2$  control four modes of operation



$B_1$	$B_2$	operation mode
0	0	shift register (scan chain)
1	0	normal operation
1	1	MISR (ORA)
0	1	LFSR (TPG)

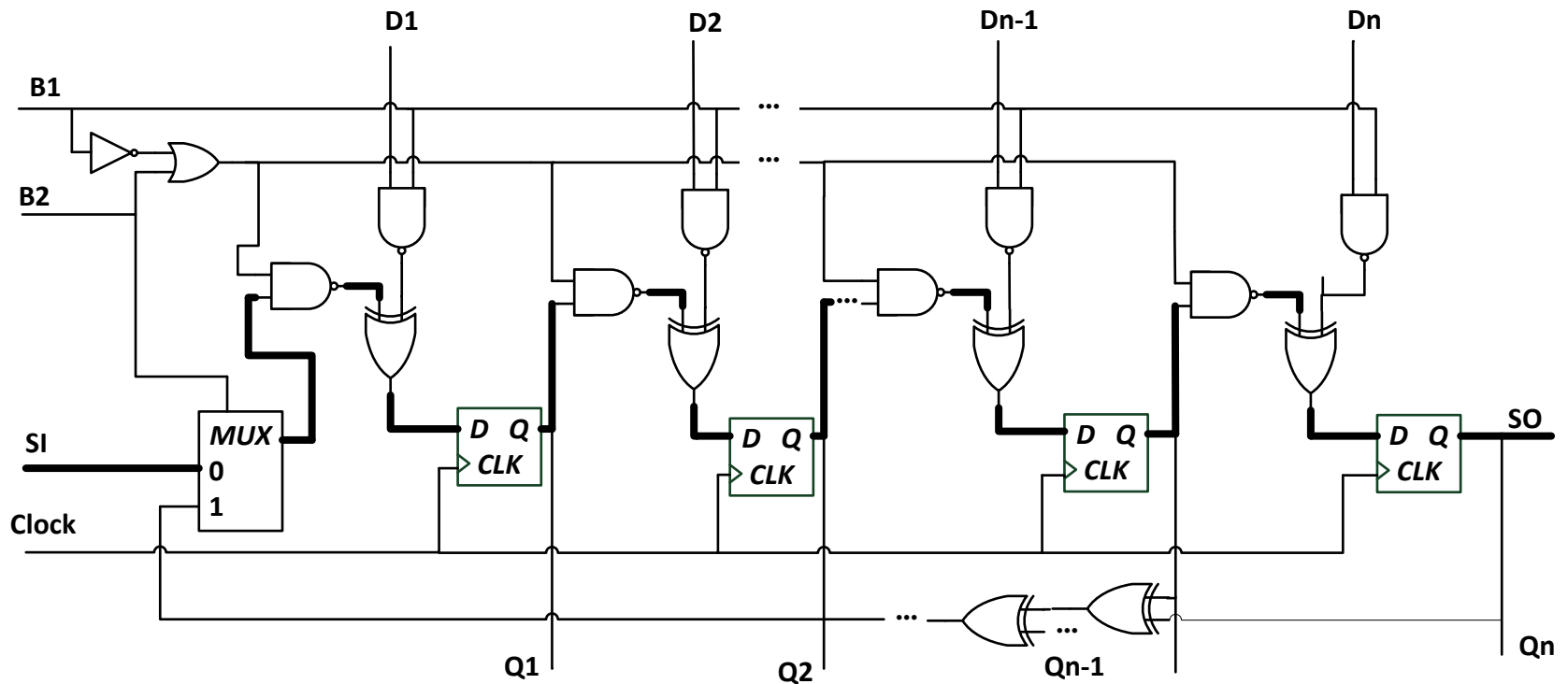
# Normal Operation Mode

- $B1=1, B2=0$



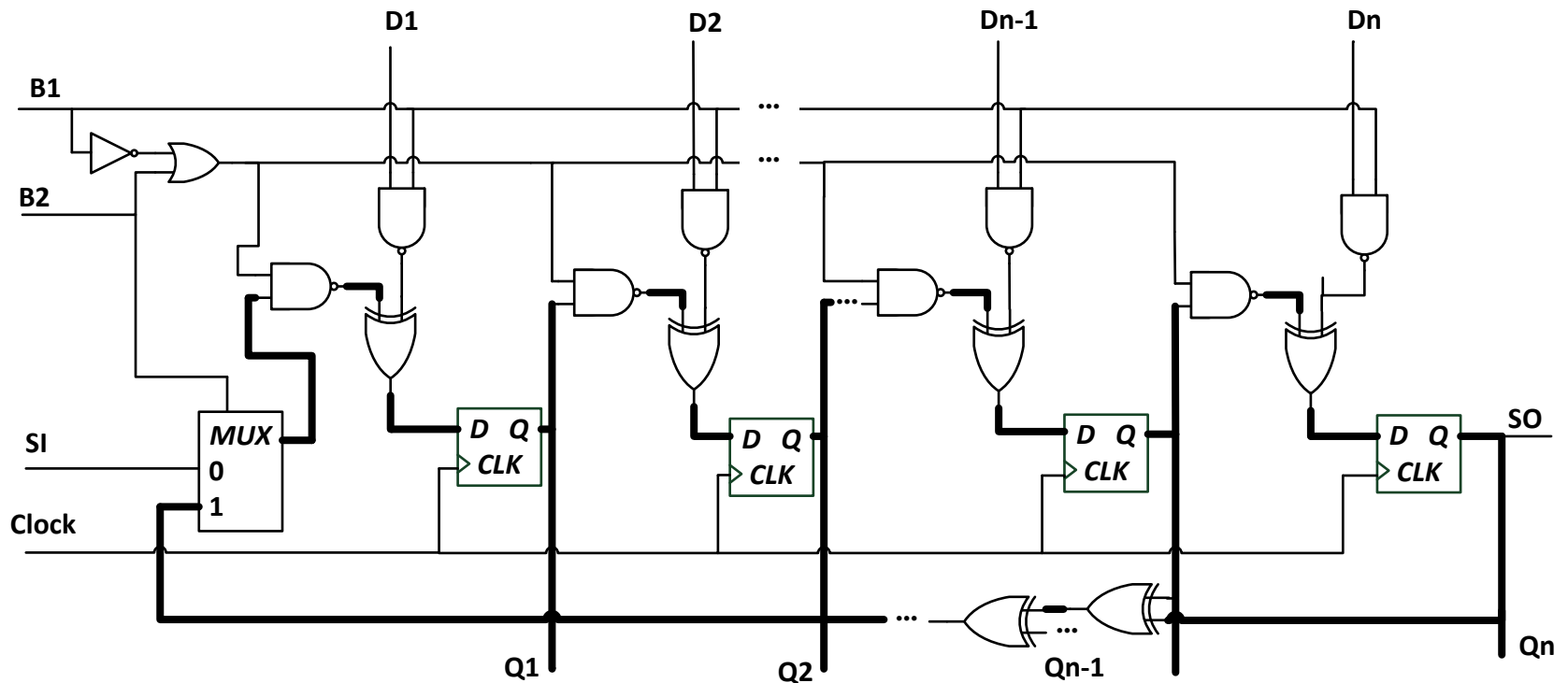
# Scan Chain Mode

- $B1=B2=0$



# LFSR Mode

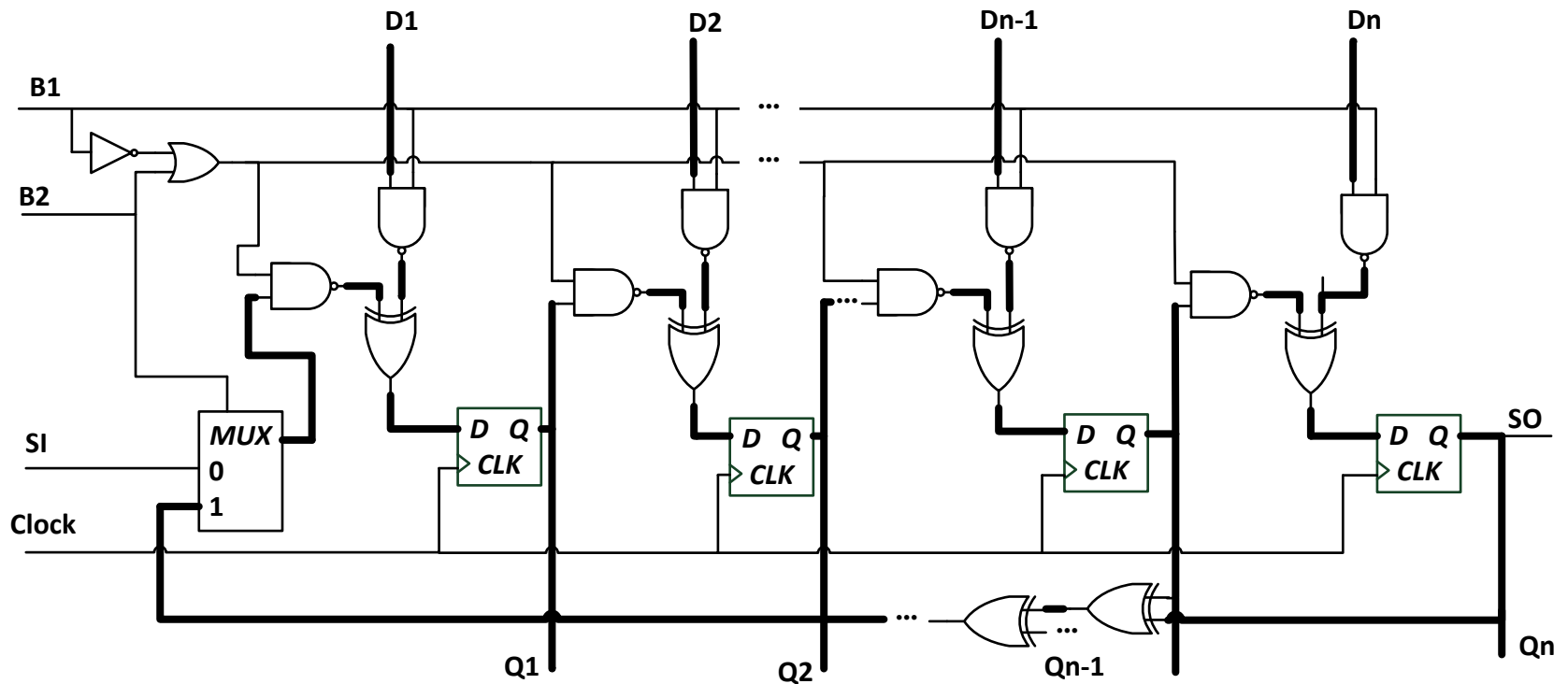
- $B1=0, B2=1$
- Type 1 LFSR





# MISR Mode

- **B1=1, B2=1**



# Pros and Cons of BILBO

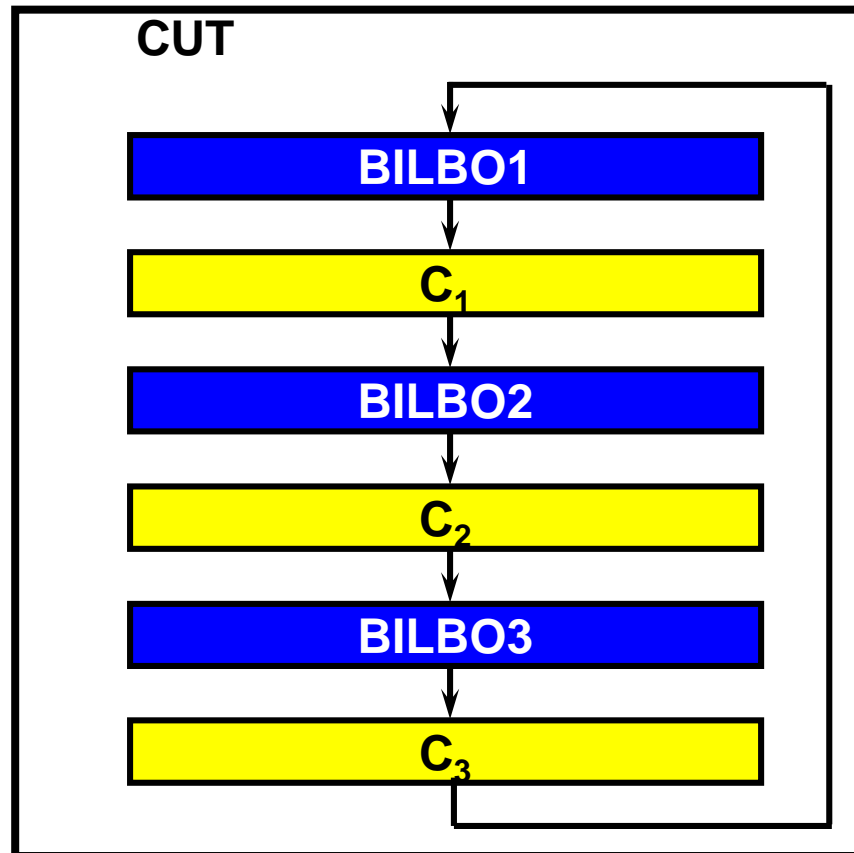
- **Pro**
  - ◆ **At-speed testing**
- **Cons**
  - ◆ **Area too large**
  - ◆ **Performance penalty**

**Not Really Useful due to Overhead**

# Quiz

**Q: BILBO belongs to separate BIST or embedded BIST?**

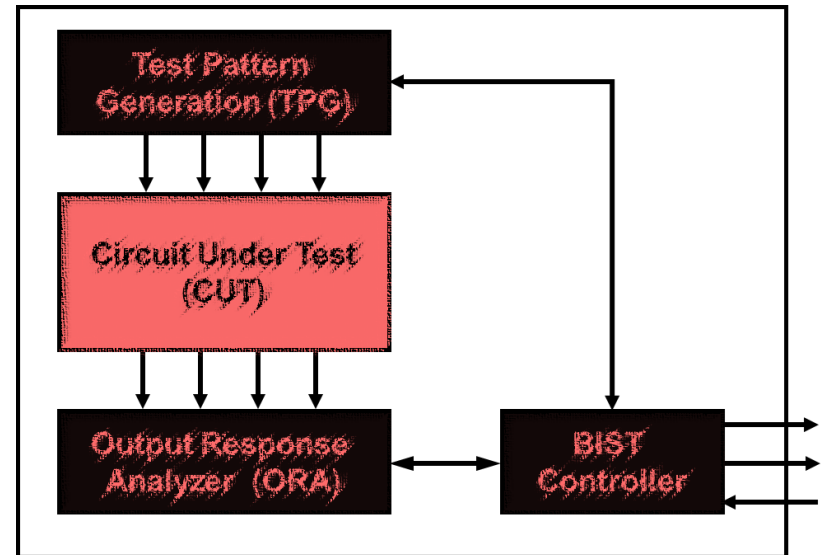
**ANS:**



Yellow blocks are comb. logic

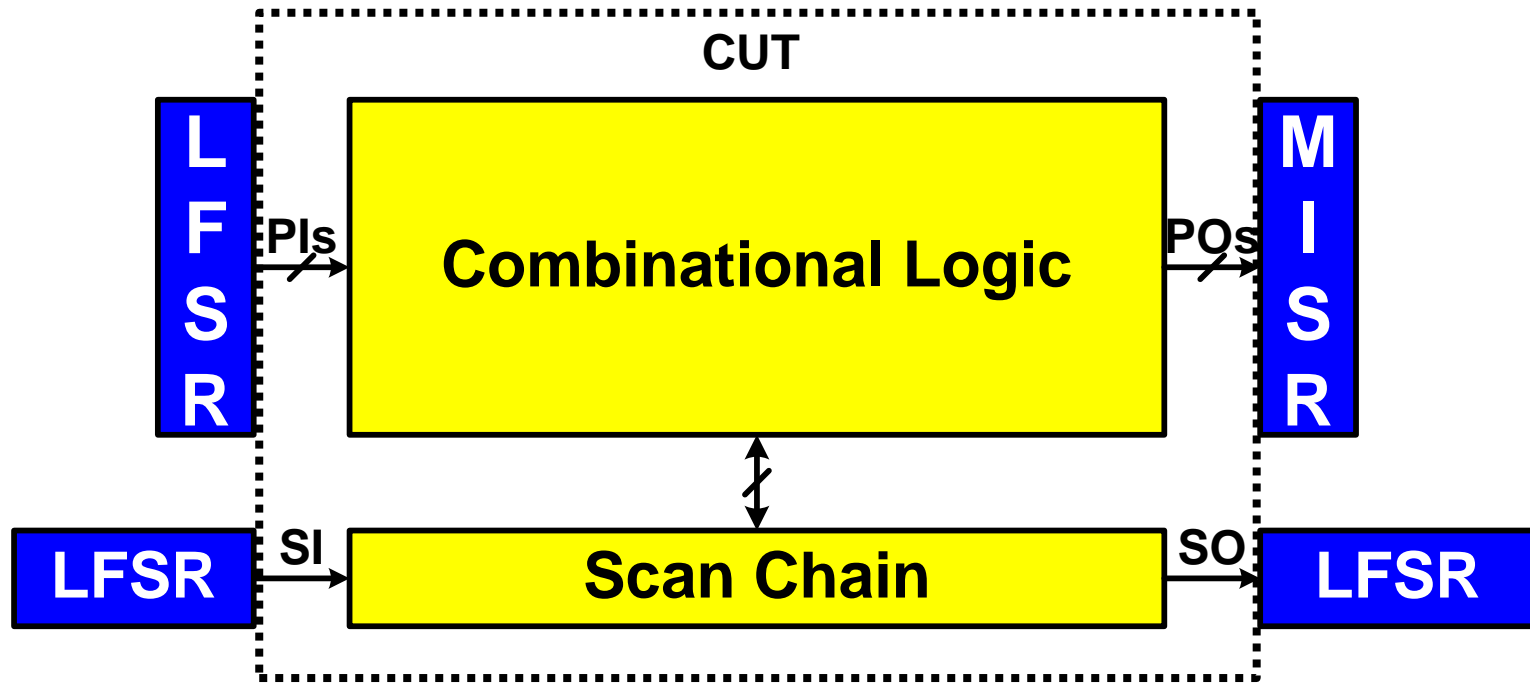
# BIST Part 2

- Output Response Analysis
- BIST Architecture
  - ◆ Test Per Clock
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- Conclusions



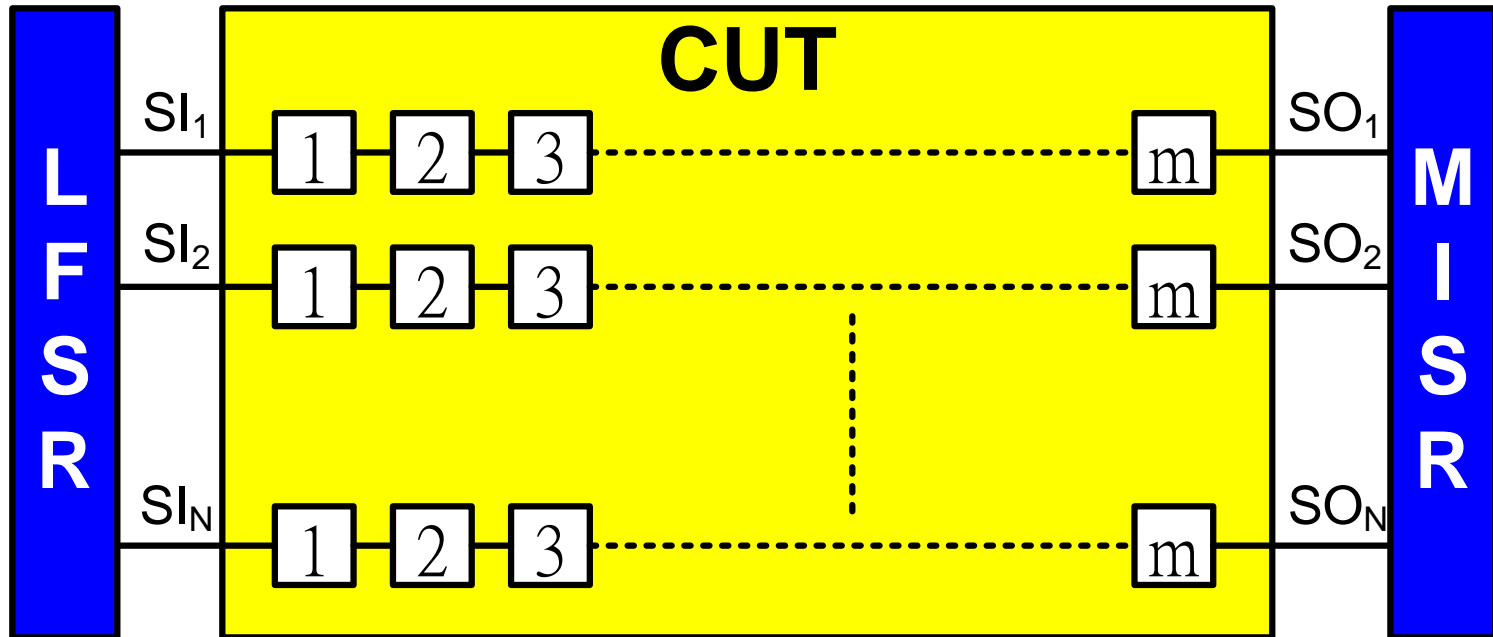
# Test Per Scan – Single Chain

- Test per Scan; Separate BIST
- Problem: not scalable.



**How about Multiple Chains?**

# STUMPS [Bardell McAnney 82]



- ***STUMPS = Self-Test Using a MISR and Parallel Shift register***
- Test per scan; separate BIST
- Small area, good for multiple chains

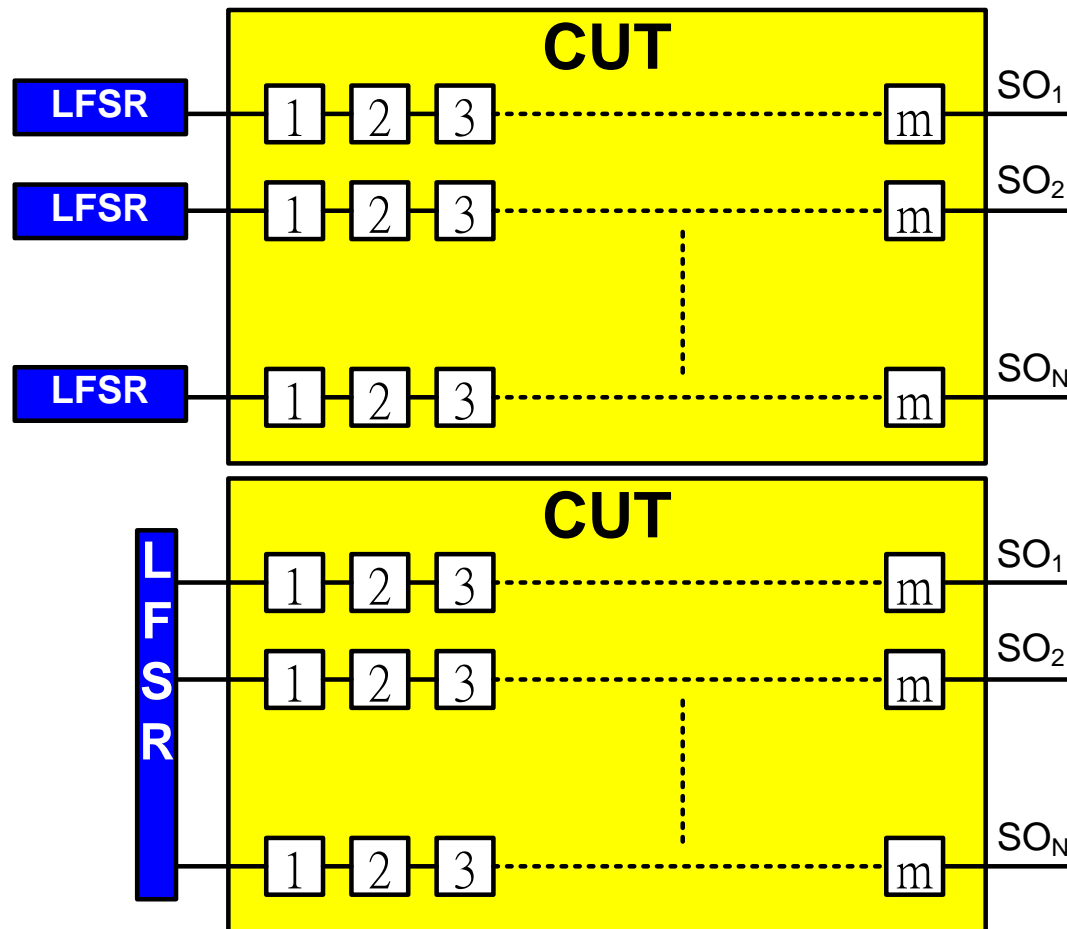
**STUMPS is Very Popular Architecture**

# Quiz

Suppose CUT has 50 scan chains. Each chains is 100 bit long. How many total bits of LFSR do we need?

Q1: if we use one LFSR for each scan chain? Each LFSR 25 bits.

Q2: if we use STUMPS?



# Pros and Cons of STUMPS

- **Advantages**
  - ◆ Low area overhead
  - ◆ Simple control
- **Disadvantages**
  - ◆ Longer test time (than test per clock)
  - ◆ Structure dependency
    - \* Need phase shifter (see next video)



# Summary

- Output Response Analysis
- BIST Architecture
  - ◆ Test Per Clock: **BILBO** (1979)
    - \* Large overhead
  - ◆ Test Per Scan: **STUMPS** (IBM, 1982)
    - \* Very useful
- Issues with BIST
- Conclusions

