

\*A. 256 KB RAM (Read & Write) Consists of 128KB and 32KB => 256 KB = 1. (128 KB RA4) + 4. (32 KB RA4) = So we need 5 chips - 1 chip of 128 KB 32 KB II | 38000H - 3FFFFH 30000H - 37FFFH 256 KB 32 KB IC 28000H - 2FFFFH 32 KB IC Inside The 8088 Hemoly 20000H - 27FFFH 32 KB IC From ODOOOH 128 KB IC 00000H-1FFFH

## (\*) Chip #1: 128 KB

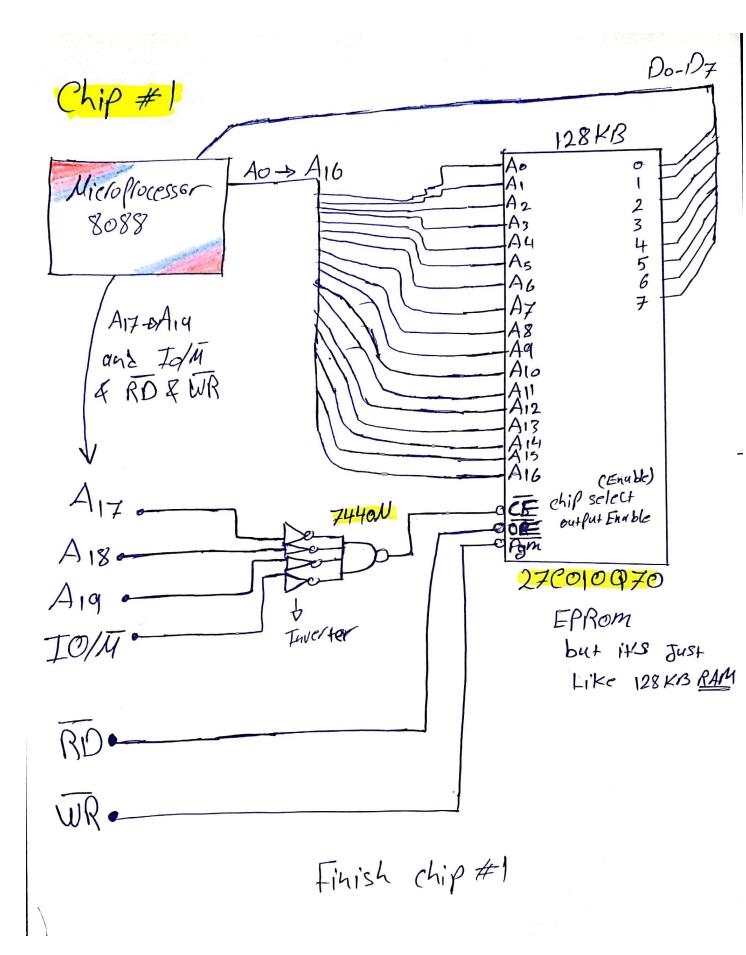
128 KB = 217	"Laux Advos"	7,	
Which Heans There			
is 131072] different Address	ses	0	
To Write or Read On it.			
Start: 0 0000 0000 0000 0000			
End: 1 11 11 111 1111	00000H <- \\ "First A22100		Mendy

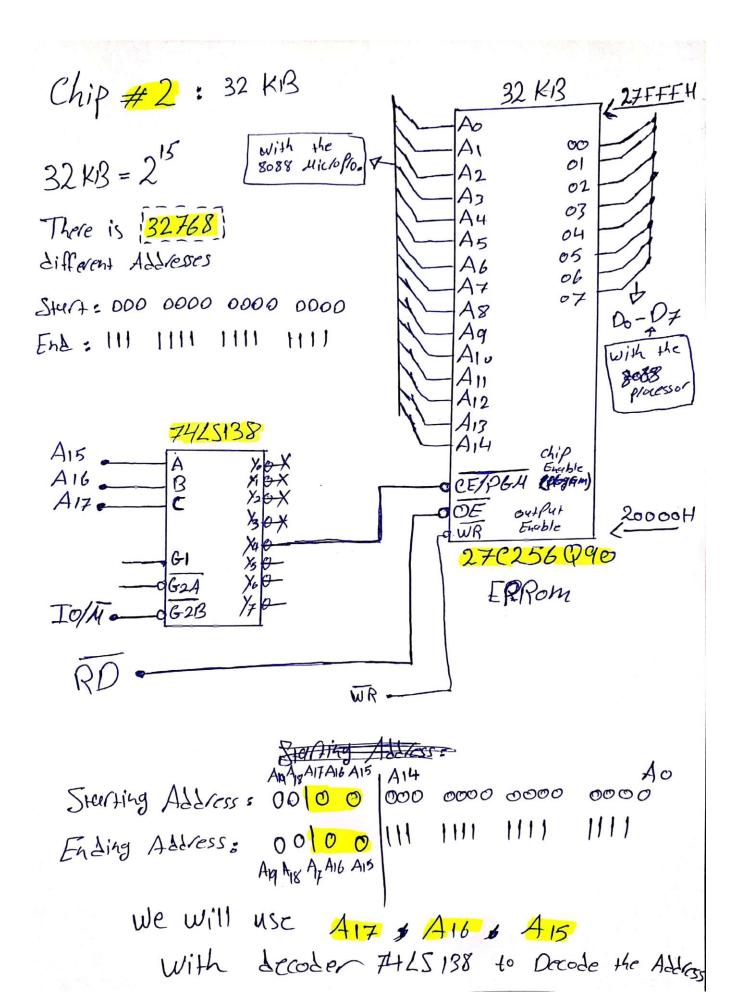
We will use Address Pins Ao A 16 to locate the Address of the Data we need to write or read with The Memory.

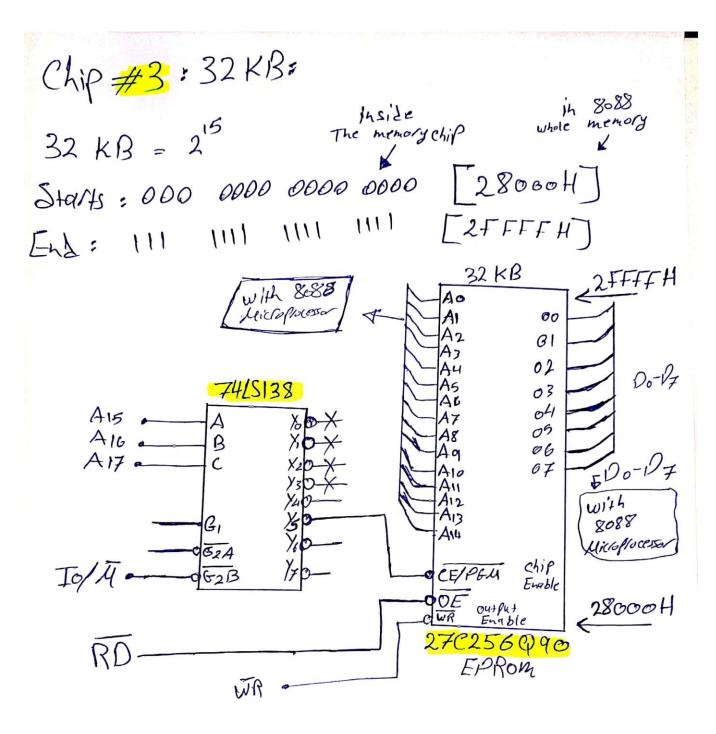
We will use Address Pins [A17 + A19] to decode The Address of the chip we need to use.

\*NAND-InPuts = A19. A18. A17

\*\*Enabling Signals: IO/4 and RD and WR

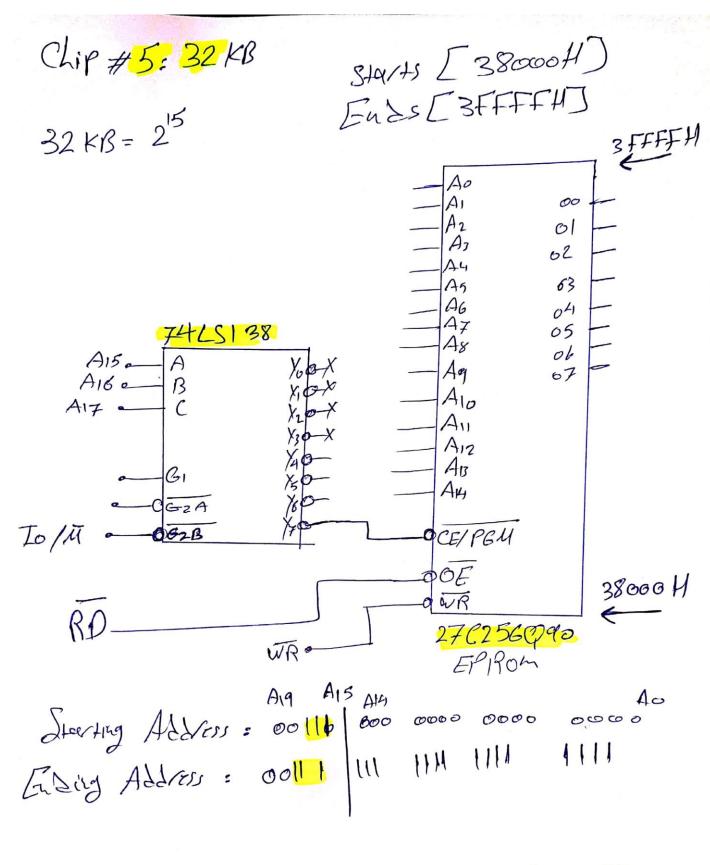






Chip#4 : 32 KB: 32 K13 = 215 Starts: 000 0000 0000 0000 [30000H] [37/FFU] +111 End = (11 1111 1111 37 FFF M 00 Do-P7 01 02 07 04 74LS138 05 06 OF GI GZA GZB CE/PGM 30000 H 270256990 WB. EPROM Stell ting Address 8 0011 0 000 0000 0000 Ending Address: 00110 111 1111 1111

we will use the same 7425138 decade

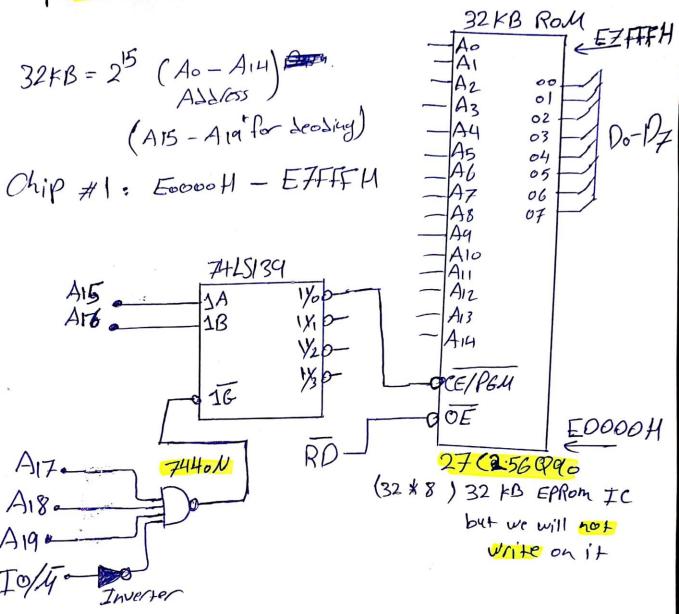


WE WIN use The Same 74LS138 Decoder

## #B. 128KB ROH (Read Only) Ends at FFFFFH

128 K13 ROM = 4. (32 KB RAM dip)

(FFFF)H = (1048575)10/128KB = 217 = (131072)10 (1048575)10 - (131072)10 = (917503)10 = (DFFF)H So: Steerting Address of the 128 KB ROM (Which means the first 32 KB Rom chip) is EDDOOH Chip#1: 32 KB ROLL



Starting Address: 11100 000 0000 0000 0000 0000 Ending Address: 11100 1111 1111 1111

for Address secoding with 7425139

## Chip#2: 32KB Rom

