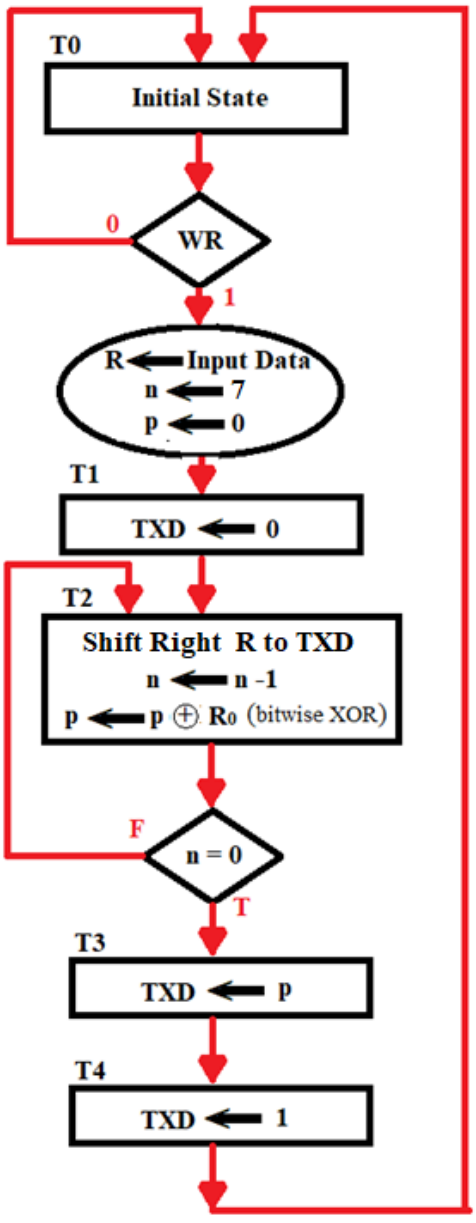
An-Najah National University
Faculty of Engineering and Information Technology
Computer Engineering Department

Digital Circuit Design II (10636321)
05/12/2020

HW2: (ILOs: **III**)	Points:**20**

Given the following ASM chart



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Write a complete **VHDL** code to implement the architecture **using 3 processes**.
(Use a positive edge **clk** and a low level asynchronous **Reset**)

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
Entity Parallel_To_Serial is
      port(         CLK, RESET, WR: in std_logic;
                    Data : in std_logic_vector(6 downto 0)
                    TXD : out std_logic);
End Parallel_To_Serial;

architecture BEHAVIOR of Parallel_To_Serial is
```

You have to submit two files:

1. A VHDL code to implement your ASM.
2. A testbench file to simulate and test your design. You should cover the following cases:

Cases:	Reset	Data	WR	Duration
Reset: Activation	0	-	0	5 clock cycles
Reset: Deactivation	1	-	0	3 clock cycles
Parallel Load	1	1010100	1	2 clock cycles
	1	1010100	0	15 clock cycles
Parallel Load	1	1011100	1	2 clock cycles
	1	1011100	0	15 clock cycles
Parallel Load	1	0000000	1	2 clock cycles
	1	0000000	0	15 clock cycles
Parallel Load	1	1111111	1	2 clock cycles
	1	1111111	0	15 clock cycles
Reset: Activation	0	-		5 clock cycles

`