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Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

B.Tech Degree S3 (R, S) / S1 (PT) (S, FE) Examination December 2023 (2019 Scheme)

Course Code: ECT203

Course Name: LOGIC CIRCUIT DESIGN

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions. Each question carries 3 marks Marks

1	Convert $(202.625)_{10}$ to binary.	(3)
2	With an example explain Binary Coded Decimals.	(3)
3	State De Morgan's theorem	(3)
4	Simplify the following Boolean expression, F = ABC + A'B + ABC', to a minimum number of literals using algebraic methods alone.	(3)
5	Design a 2-bit decoder	(3)
6	Write verilog code for a 1x4 demux.	(3)
7	Differentiate between Flip Flop and Latch	(3)
8	Implement a T Flip Flop using D Flip Flop	(3)
9	With an example explain transition time.	(3)
10	Give the names (full form) of 3 logic families.	(3)

PART B

Answer any one full question from each module. Each question carries 14 marks

Module 1

11	(a) Represent 543.125 using signed 32-bit floating point representation (8-bit exponent)	(8)
	(b) Convert $(123B)_{16}$ to binary and octal.	(6)
12	(a) Compute $(232)_{10} - (325)_{10}$ by using 2's complement method.	(9)
	(b) Explain the operators in Verilog.	(5)

Module 2

13	(a) Minimise the following function into SoP form. $F(w, x, y, z) = \Sigma m(0,6,8,13,14) + d(2,4,10)$	(6)
	(b) Draw the circuit diagram for the minimised expression.	(3)

(c) Write a Verilog code to implement the same (5)

14 (a) Minimise the following function into PoS form. (6)

$$F(w, x, y, z) = \Pi(1, 3, 6, 9, 11, 12, 14)$$

(b) Draw the circuit diagram for the minimised expression (3)

(c) Write a Verilog code to implement the same. (5)

Module 3

15 (a) Implement the boolean function $F(A, B, C, D) = \Sigma(0, 1, 2, 3, 6, 10, 11, 14)$ using an 8X1 mux. (8)

(b) Write the verilog code to implement the boolean function $F(A, B, C, D) = \Sigma(0, 1, 2, 3, 6, 10, 11, 14)$ using an 8X1 mux.(Code should contain seperate modules for implementing the mux and the function) (6)

16 (a) Design a Half Adder (3)

(b) Design a Full Adder by taking the Half Adder designed in (a) as the building block (4)

(c) Design and implement a BCD Adder. (7)

Module 4

17 (a) Design synchronous 3 bit UP counter using JK Flipflop. (8)

(b) Design and implement 4 bit Johnson counter. (6)

18 (a) Explain the operation of Master Slave JK Flip flop. (7)

(b) Design a mod-10 asynchronous counter. (7)

Module 5

19 (a) Compare TTL & CMOS logic families in terms of logics levels, noise margin, fan-out, propagation delay, transition time, power consumption and power-delay product. (7)

(b) List the applications of CMOS and TTL logic families. Justify their use in those applications based on the comparison given above. (7)

20 Draw the circuit diagram and explain the working of the following:

a) CMOS NOR gate (7)

b) TTL inverter (7)

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