ECT 203	LOGIC CIRCUIT DESIGN	CATEGORY	L	T	P	CREDIT
		PCC	3	1	0	4

Preamble: This course aims to impart the basic knowledge of logic circuits and enable students to apply it to design a digital system.

Prerequisite: EST130 Basics of Electrical and Electronics Engineering

Course Outcomes: After the completion of the course the student will be able to

CO 1	Explain the elements of digital system abstractions such as digital representations of information, digital logic and Boolean algebra
CO 2	Create an implementation of a combinational logic function described by a truth table using and/or/inv gates/ muxes
CO 3	Compare different types of logic families with respect to performance and efficiency
CO 4	Design a sequential logic circuit using the basic building blocks like flip-flops
CO 5	Design and analyze combinational and sequential logic circuits through gate level Verilog models.

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12
CO 1	3	3										
CO 2	3	3	3									
CO 3	3	3										
CO 4	3	3	3									
CO 5	3	3	3		3							

Assessment Pattern

Bloom's Category	Continuous Assessment Tests		End Semester Examination
	1	2	
Remember	10	10	10
Understand	20	20	20
Apply	20	20	70
Analyse			
Evaluate			
Create			

Mark distribution

Total Marks	CIE	ESE	ESE Duration
150	50	100	3 hours

Continuous Internal Evaluation Pattern:

Attendance	: 10 marks
Continuous Assessment Test (2 numbers)	: 25 marks
Course project	: 15 marks

It is mandatory that a *course project* shall be undertaken by a student for this subject. The course project can be performed either as a hardware realization/simulation of a typical digital system using combinational or sequential logic. Instead of two assignments, two evaluations may be performed on the course project along with series tests, each carrying 5 marks. Upon successful completion of the project, a brief report shall be submitted by the student which shall be evaluated for 5 marks. The report has to be submitted for academic auditing. A few samples projects are given below:

Sample course projects:

1. M-Sequence Generator Psuedo random sequences are popularly used in wireless communication. A sequence generator is used to produce pseudo random codes that are useful in spread spectrum applications. Their generation relies on irreducible polynomials.A maximal length sequence generator that relies on the polynomial P (D) = $D^7 + D^3 + 1$, with each D represent delay of one clock cycle.

- An 8-bit shift register that is configured as a ring counter may be used realize the above equation.
- This circuit can be developed in verilog, simulated, synthesized and programmed into a tiny FPGA and tested in real time.
- Observe the M-sequnce from parallel outputs of shift register for one period . Count the number of 1s and zeros in one cycle.
- Count the number of runs of 1s in singles, pairs, quads etc. in the pattern.

2. BCD Subtractor

- Make 4 -bit parallel adder circuit in verilog.
- Make a one digit BCD subtracter in Verilog, synthesize and write into a tiny FPGA.
- Test the circuit with BCD inputs.

3. Digital Thermometer

- Develop a circuit with a temperature sensor and discrete components to measure and dispaly temperature.
- Solder the circuit on PCB and test it.

4. Electronic Display

- This display should receive the input from an alphanumeric keyboard and display it on an LCD diplay.
- The decoder and digital circuitry is to developed in Verilog and programmed into a tiny FPGA.

5. Electronic Roulette Wheel

- 32 LEDs are placed in a circle and numbered that resembles a roulette wheel.
- A 32-bit shift register generates a random bit pattern with a single 1 in it.
- When a push button is pressed the single 1 lights one LED randomly.
- Develop the shift register random pattern generator in verilog and implement on a tiny FPGA and test the circuit.

6. Three Bit Carry Look Ahead Adder

- Design the circuit of a three bit carry look ahead adder.
- Develop the verilog code for it and implement and test it on a tiny FPGA. item Compare the performance with a parallel adder.

End Semester Examination Pattern: There will be two parts; Part A and Part B. Part A contain 10 questions with 2 questions from each module, having 3 marks for each question. Students should answer all questions. Part B contains 2 questions from each module of which student should answer any one. Each question can have maximum 2 sub-divisions and carry 14 marks. The questions on verlog modelling should not have a credit more than 25% of the whole mark.

Course Level Assessment Questions

Course Outcome 1 (CO1) : Number Systems and Codes

1. Consider the signed binary numbers A = 01000110 and B = 11010011 where B is in 2's complement form. Find the value of the following mathematical expression (i) A + B (ii) A – B
2. Perform the following operations (i)$D9CE_{16}$-$CFDA_{16}$ (ii) 6575_8-5732_8
3. Convert decimal 6,514 to both BCD and ASCII codes. For ASCII, an even parity bit is to be appended at the left.

Course Outcome 2 (CO2) : Boolean Postulates and combinational circuits

1. Design a magnitude comparator to compare two 2-bit numbers A = A_1A_0 and B = B_1B_0B
2. Simplify using K-map F(a,b,c,d) = Σ m (4,5,7,8,9,11,12,13,15)
3. Explain the operation of a 8x1 multiplexer and implement the following using an 8x1 multiplexer F(A, B, C, D) = Σ m (0, 1, 3, 5, 6, 7, 8, 9, 11, 13, 14)

Course Outcome 3 (CO3) : Logic families and its characteristics

1. Define the terms noise margin, propagation delay and power dissipation of logic families. Compare TTL and CMOS logic families showing the values of above mentioned terms.
2. Draw the circuit and explain the operation of a TTL NAND gate
3. Compare TTL, CMOS logic families in terms of fan-in, fan-out and supply voltage

Course Outcome 4 (CO4) : Sequential Logic Circuits

1. Realize a T flip-flop using NAND gates and explain the operation with truth table, excitation table and characteristic equation
2. Explain a MOD 6 asynchronous counter using JK Flip Flop
3. Draw the logic diagram of 3 bit PIPO shift register with LOAD/SHIFT control and explain its working

Course Outcome 5 (CO5) : Logic Circuit Design using HDL

1. Design a 4-to-1 mux using gate level Verilog model.
2. Design a verilog model for a hald adder circuit. Make a one bit full adder by connecting two half adder models.
3. Compare concurrent signal assignment versus sequential signal assignment.

Syllabus

Module 1: Number Systems and Codes:

Binary and hexadecimal number systems; Methods of base conversions; Binary and hexadecimal arithmetic; Representation of signed numbers; Fixed and floating point numbers; Binary coded decimal codes; Gray codes; Excess 3 code. Alphanumeric codes: ASCII. Basics of verilog -- basic language elements: identifiers, data objects, scalar data types, operators.

Module 2: Boolean Postulates and Fundamental Gates

Boolean postulates and laws – Logic Functions and Gates De-Morgan's Theorems, Principle of Duality, Minimization of Boolean expressions, Sum of Products (SOP), Product of Sums (POS), Canonical forms, Karnaugh map Minimization. Modeling in verilog, Implementation of gates with simple verilog codes.

Module 3: Combinatorial and Arithmetic Circuits

Combinatorial Logic Systems - Comparators, Multiplexers, Demultiplexers, Encoder, Decoder. Half and Full Adders, Subtractors, Serial and Parallel Adders, BCD Adder. Modeling and simulation of combinatorial circuits with verilog codes at the gate level.

Module 4: Sequential Logic Circuits:

Building blocks like S-R, JK and Master-Slave JK FF, Edge triggered FF, Conversion of Flipflops, Excitation table and characteristic equation. Implementation with verilog codes. Ripple and Synchronous counters and implementation in verilog, Shift registers-SIPO, SISO, PISO, PIPO. Shift Registers with parallel Load/Shift, Ring counter and Johnsons counter. Asynchronous and Synchronous counter design, Mod N counter. Modeling and simulation of flipflops and counters in verilog.

Module 5: Logic families and its characteristics:

TTL, ECL, CMOS - Electrical characteristics of logic gates – logic levels and noise margins, fan-out, propagation delay, transition time, power consumption and power-delay product. TTL inverter - circuit description and operation; CMOS inverter - circuit description and operation; Structure and operations of TTL and CMOS gates; NAND in TTL and CMOS, NAND and NOR in CMOS.

Text Books

1. Mano M.M., Ciletti M.D., "Digital Design", Pearson India, 4th Edition. 2006
2. D.V. Hall, "Digital Circuits and Systems", Tata McGraw Hill, 1989

3. S. Brown, Z. Vranesic, “Fundamentals of Digital Logic with Verilog Design”, McGraw Hill

4. Samir Palnikar“Verilog HDL: A Guide to Digital Design and Syntheis”, Sunsoft Press

5. R.P. Jain, “Modern digital Electronics”, Tata McGraw Hill, 4th edition, 2009

Reference Books

1. W.H. Gothmann, “Digital Electronics – An introduction to theory and practice”, PHI, 2nd edition ,2006
2. Wakerly J.F., “Digital Design: Principles and Practices,” Pearson India, 4th 2008

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3. A. Ananthakumar ,”Fundamentals of Digital Circuits”, Prentice Hall, 2nd edition, 2016
4. Fletcher, William I., An Engineering Approach to Digital Design, 1st Edition, Prentice Hall India, 1980

Course Contents and Lecture Schedule

No	Topic	No. of Lectures
1	**Number Systems and Codes**:	
1.1	Binary, octal and hexadecimal number systems; Methods of base conversions;	2
1.2	Binary, octal and hexadecimal arithmetic;	1
1.3	Representation of signed numbers; Fixed and floating point numbers;	3
1.4	Binary coded decimal codes; Gray codes; Excess 3 code :	1
1.5	Error detection and correction codes - parity check codes and Hamming code-Alphanumeric codes:ASCII	3
1.6	Verilog basic language elements: identifiers, data objects, scalar data types, operators	2
2	**Boolean Postulates and Fundamental Gates:**	
2.1	Boolean postulates and laws – Logic Functions and Gates, De-Morgan’s Theorems, Principle of Duality	2
2.2	Minimization of Boolean expressions, Sum of Products (SOP), Product of Sums (POS)	2
2.3	Canonical forms, Karnaugh map Minimization	1
2.4	Gate level modelling in Verilog: Basic gates, XOR using NAND and NOR	2
3	**Combinatorial and Arithmetic Circuits**	
3.1	Combinatorial Logic Systems - Comparators, Multiplexers, Demultiplexers	2
3.2	Encoder, Decoder, Half and Full Adders, Subtractors, Serial and Parallel Adders, BCD Adder	3

3.3	Gate level modelling combinational logic circuits in Verilog: half adder, full adder, mux, demux, decoder, encoder	3
4	**Sequential Logic Circuits:**	
4.1	Building blocks like S-R, JK and Master-Slave JK FF, Edge triggered FF	2
4.2	Conversion of Flipflops, Excitation table and characteristic equation.	1
4.3	Ripple and Synchronous counters, Shift registers-SIPO.SISO,PISO,PIPO	2
4.4	Ring counter and Johnsons counter, Asynchronous and Synchronous counter design	3
4.5	Mod N counter, Random Sequence generator	1
4.6	Modelling sequential logic circuits in Verilog: flipflops, counters	2
5	**Logic families and its characteristics**:	
5.1	TTL,ECL,CMOS- Electrical characteristics of logic gates – logic levels and noise margins, fan-out, propagation delay, transition time, power consumption and power-delay product.	3
5.2	TTL inverter - circuit description and operation	1
5.3	CMOS inverter - circuit description and operation	1
5.4	Structure and operations of TTL and CMOS gates; NAND in TTL, NAND and NOR in CMOS.	2

Simulation Assignments (ECT203)

The following simulations can be done in QUCS, KiCad or PSPICE.

BCD Adder

- Realize a one bit paraller adder, simulate and test it.
- Cascade four such adders to form a four bit parallel adder.
- Simulate it and make it into a subcircuit.
- Develop a one digit BCD adder, based on the subcircuit, simulate and test it

BCD Subtractor

- Use the above 4 -bit adder subcircuit, implement and simulate a one digit BCD subtractor.
- Test it with two BCD inputs

Logic Implementation with Multiplexer

- Develop an 8 : 1 multiplexer using gates, simulate, test and make it into a subcircuit.
- Use this subcircuit to implement the logic function $f(A, B, C) = \sum m(1, 3, 7)$
- Modify the truth table properly and implement the logic function $f(A, B, C, D) = \sum m(1, 4, 12, 14)$ using one 8 : 1 multiplexer.

BCD to Seven Segment Decoder

- Develop a BCD to seven segment decoder using gates and make it into a subcircuit.
- simulate this and test it

Ripple Counters

- Understand the internal circuit of 7490 IC and develop it in the simulator.
- Make it into a subcircuit and simulate it. Observe the truth table and timing diagrams for mod-5, mod-2 and mod-10 operation.
- Develop a mod-40 (mod-8 and mod-5) counter by cascading two such subcircuits.
- Simulate and observe the timing diagram and truth table.

Synchronous Counters

- Design and develop a 4-bit synchronous counter using J-K flip-flops.
- Perform digital simulation and observe the timing diagram and truth table.

Sequence Generator

- Connect D flip-flops to realize and 8-bit shift register and make it into a subcircuit.
- sequence generator that relies on the polynomial $P(D) = D_7 + D_3 + 1$, with each D represent delay of one clock cycle
- Simulate and observe this maximal length pseudo random sequence.

Transfer Characteristics of TTL and CMOS Inverters

- Develop a standard TTL circuit and perform sweep simulation and observe the transfer characteristics. Compute the threshold voltage and noise margns.
- Develop and simulate standard CMOS inverter circuit and perform sweep simulation and observe the transfer characteristics. Compute the threshold voltage and noise margins.

Model Question Paper

A P J Abdul Kalam Technological University

Third Semester B Tech Degree Examination

Branch: Electronics and Communication

Course: ECT 203 Logic Circuit Design

Time: 3 Hrs **Max. Marks: 100**

PART A

Answer All Questions

1 Convert 203.52_{10} to binary and hexadecimal. (3) K_1

2 Compare bitwise and logical verilog operators (3) K_1

3 Prove that NAND and NOR are not associative. (3) K_2

4 Convert the expression $ABCD+AB\overline{C}+ACD$ to minterms. (3) K_2

5 Define expressions in Verilog with example. (3) K_2

6 Explain the working of a decoder. (3) K_1

7 What is race around condition? (3) K_1

8 Convert a T flip-flop to D flip-flop. (3) K_2

9 Define fan-in and fan-out of logic circuits. (3) K_2

10 Define noise margin and how can you calculate it? (3) K_2

PART B

Answer one question from each module. Each question carries 14 mark.

Module I

11(A) Subtract 46_{10} from 100_{10} using 2's complement arithmetic. (8) K_2

11(B) Give a brief description on keywords and identifiers in Verilog with example. (6) K_2

OR

12(A) Explain the floating and fixed point representation of numbers (8) K_2

12(A) Explain the differences between programming lanuguages and HDLs (6) K_2

Module II

13(A) Simplify using K-map (7) K_3

$$f(A, B, C, D) = \sum m(4, 5, 7, 8, 9, 11, 12, 13, 15)$$

using K-maps

13(B) Write a Verilog code for implementing above function (7) K_3

OR

14(A) Write a Verilog code to implement the basic gates. (7) K_3

14(B) Reduce the following Boolean function using K-Map and implement the simplified function using the logic gates (7) K_3

$$f(A, B, C, D) = \sum(0, 1, 4, 5, 6, 8, 9, 10, 12, 13, 14)$$

Module III

15(A) Design a 3-bit magnitude comparator circuit. (8) K_3

15(B) Write a Verilog description for a one bit full adder circuit. (6) K_3

OR

16(A) Write a verilog code to implement 4:1 multiplexer (6) K_3

16(B) Implement the logic function (8) K_3

$$f(A, B, C) = \sum m(0, 1, 4, 7)$$

using 8 : 1 and 4 : 1 multiplexers.

Module IV

17	Design MOD 12 asynchronous counter using T flip-flop.	(14)	K_3

OR

18(A)	Explain the operation of Master Slave JK flipflop.	(7)	K_3
18(B)	Derive the ouput Q_{n+1} in Terms of J_n, K_n and Q_n	(7)	K_3

Module V

19(A)	Explain in detail about TTL with open collector output configuration.	(8)	K_2
19(B)	Draw an ECL basic gate and explain.	(6)	K_2

OR

20(A)	Demonstrate the CMOS logic circuit configuration and characteristics in detail.	(8)	K_2
20(B)	Compare the characteristics features of TTL and ECL digital logic families	(6)	K_2