APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

LOGIC CIRCUIT DESIGN (ECT-203)

MODULE 5
NOTES

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MODULE 5
(TOPIC-1)

CLASSIFICATION AND CHARACTERISTICS OF LOGIC FAMILIES

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LOGIC FAMILY

- A Collection of different IC's that has similar circuit characteristics

(Or)

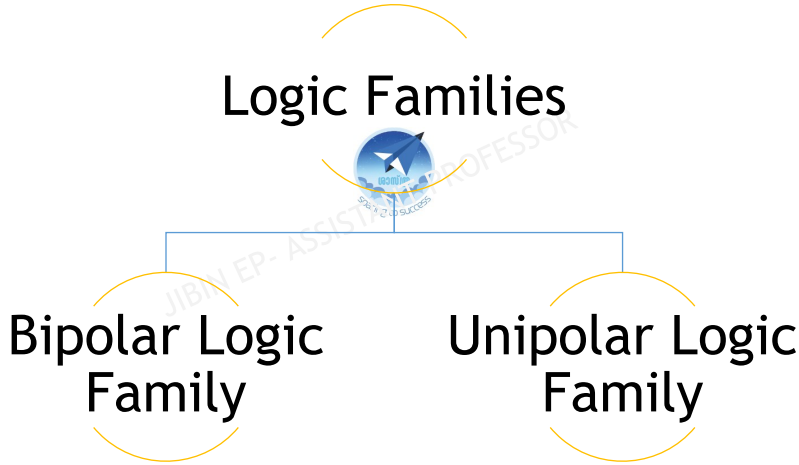
- A Group of Compatible IC's with same logic levels and supply voltages fabricated for performing various logic functions referred to as a Logic Family

INTEGRATION LEVELS

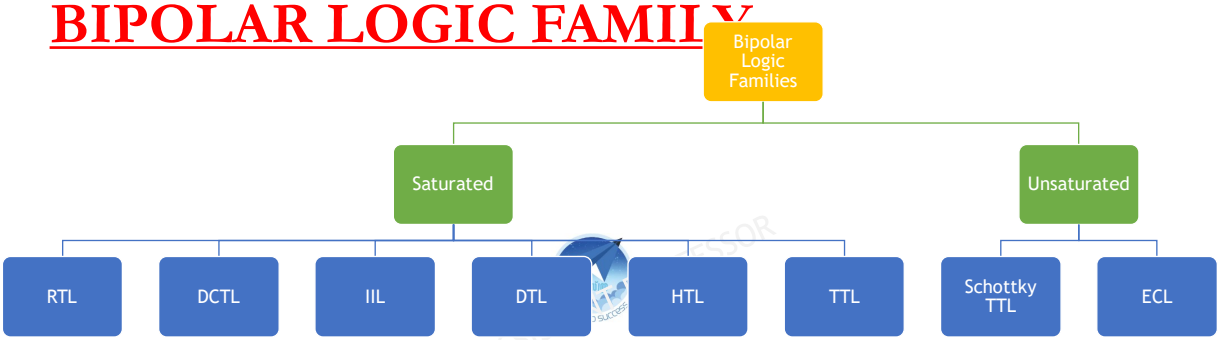
SSI (SMALL SCALE INTEGRATION)	12 Gates/ Chip
MSI (MEDIUM SCALE INTEGRATION)	100 Gates/ Chip
LSI (LARGE SCALE INTEGRATION)	1K Gates/ Chip
VLSI (SMALL SCALE INTEGRATION)	10K Gates/Chip
ULSI (SMALL SCALE INTEGRATION)	100K Gates/ Chip

CLASSIFICATION OF LOGIC FAMILIES

(BASED OF DIRECTION OF CURRENT)



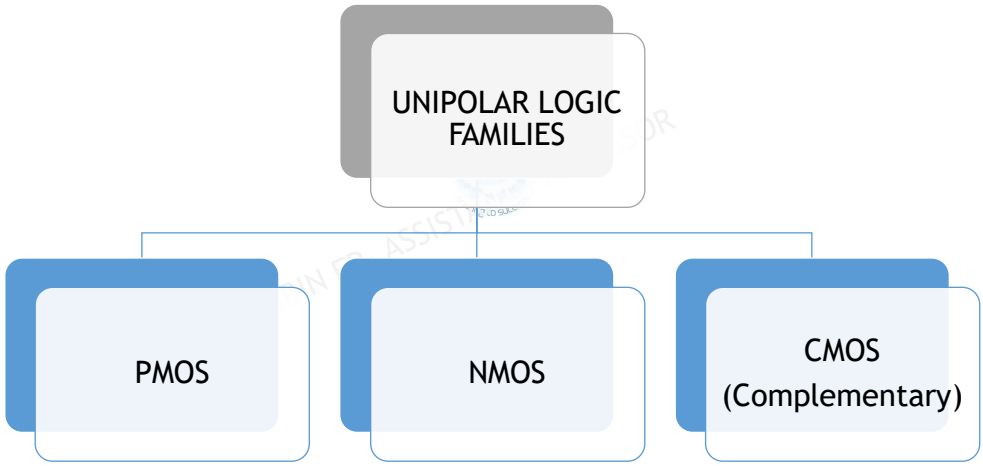
BIPOLAR LOGIC FAMILY



RTL- Resistor Transistor Logic
IIL- Integration Injection Logic
HTL- High Threshold Logic
ECL- Emitter Coupled Logic

DCTL- Directly Coupled Transistor Logic
DTL- Diode Transistor Logic
TTL- Transistor Transistor Logic

UNIPOLAR LOGIC FAMILY



Characteristics of Logic Families

1-Speed

Determined by the time between the application of input and change in output

2-Fan-out

The Number of loads that the output of gate can drive

3-Fan-in

The Maximum number of inputs that can be applied to a Logic Gate

Characteristics of Logic Families

4-Power Dissipation

Power Consumed per gate

5-Propogation Delay

The average delay time for the signal to propagate input to output

6-Noise Margin

It is the limit of noise voltage that can be present without disturbing proper operation of the circuit

Characteristics of Logic Families

7-Figure of Merit (Power Delay Product)

Product of Propagation Delay and Power Dissipation

8-Logic Swing

Difference Between Two Output Voltages ($V_{OH} - V_{OL}$)

9-Noise Immunity

Maximum rate that a circuit can withstand without changing the Output

MODULE 5
(TOPIC-2)

CMOS
Complementary Metal Oxide Semiconductor

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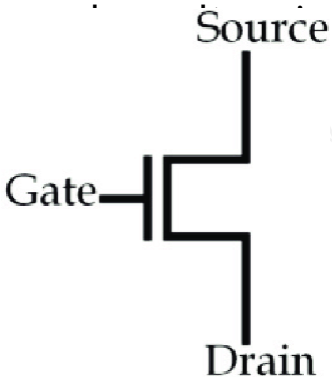
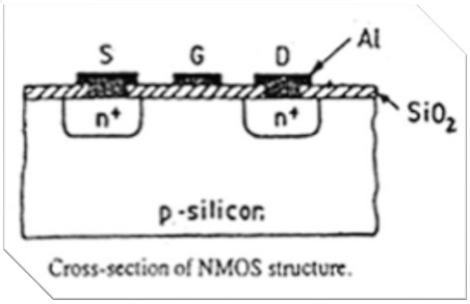
CMOS

- The term CMOS stands for “Complementary Metal Oxide Semiconductor”.
- This is one of the most popular technology in the computer chip design industry and it is broadly used today to form integrated circuits in numerous and varied applications.
- This technology makes use semiconductor devices of both P channel and N channel

NMOS

- NMOS is built on a p-type substrate with n-type source and drain diffused on it.
- In NMOS, the majority of carriers are electrons.
- When a high voltage is applied to the gate, the NMOS will conduct.
- W[illegible] applied to the gate, NMOS will not conduct.

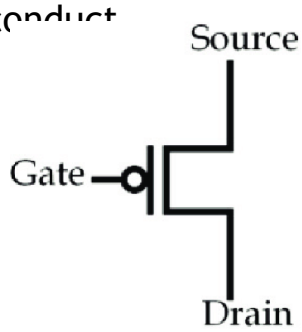


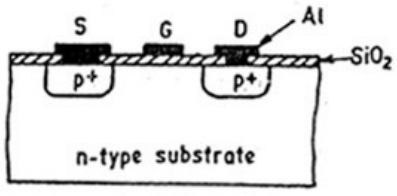


Cross-section of NMOS structure.

PMOS

- P- channel MOSFET consists of P-type Source and Drain diffused on an N-type substrate.
- The majority of carriers are holes.
- When a high voltage is applied to the gate, the PMOS will not conduct. When a low voltage is applied to the gate, the PMOS will conduct

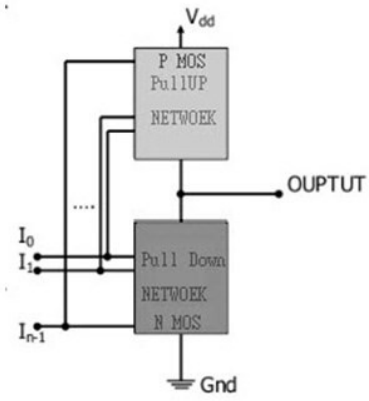




Cross-section of PMOS structure.

CMOS WORKING PRINCIPLE

- In CMOS technology, both N-type and P-type transistors are used to design logic functions.
- The same signal which turns ON a transistor of one type is used to turn OFF a transistor of the other type.
- In CMOS logic gates a collection of n-type MOSFETs is arranged in a pull-down network between the output and the low voltage power supply rail (Vss or quite often ground).
- Instead of the load resistor of NMOS logic gates, CMOS logic gates have a collection of p-type MOSFETs in a pull-up network between the output and the higher-voltage rail (often named Vdd).



CMOS INVERTER

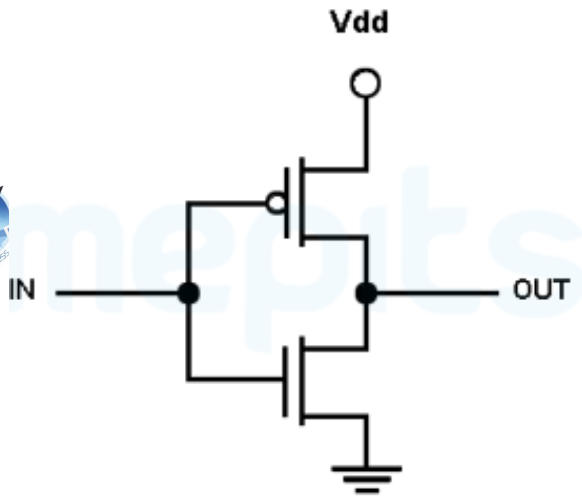
Refer Video

INPUT	OUTPUT
0 (0 V)	1 (Vdd)
1 (Vdd)	0 (0 V)

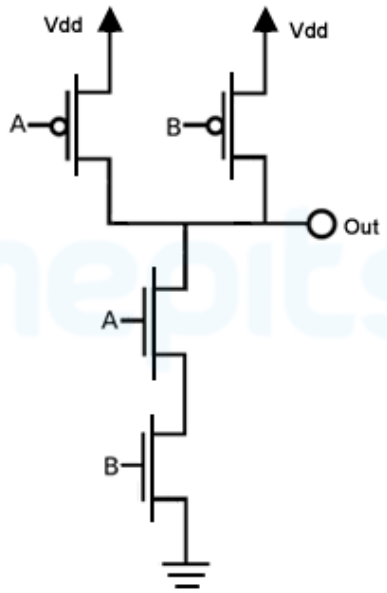
JIBIN EP- ASSISTANT PROFESSOR

CMOS INVERTER

- It consists of PMOS and NMOS FET.
- The input A serves as the gate voltage for both transistors.
- The NMOS transistor has input from Vss (ground) and the PMOS transistor has input from Vdd. The terminal Y is output.
- When a high voltage (~ Vdd) is given at input terminal (A) of the inverter, the PMOS becomes an open circuit, and NMOS switched OFF so the output will be pulled down to Vss.
- When a low-level voltage (<Vdd, ~0v) applied to the inverter, the NMOS switched OFF and PMOS switched ON. So the output becomes Vdd or the circuit is pulled up to Vdd



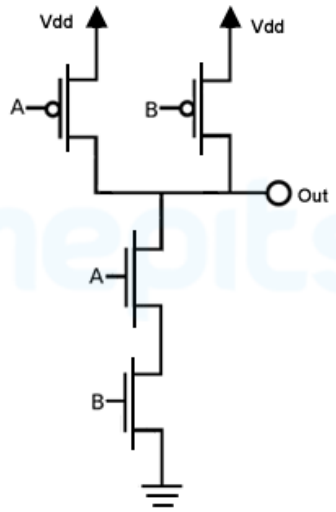
CMOS NAND GATE



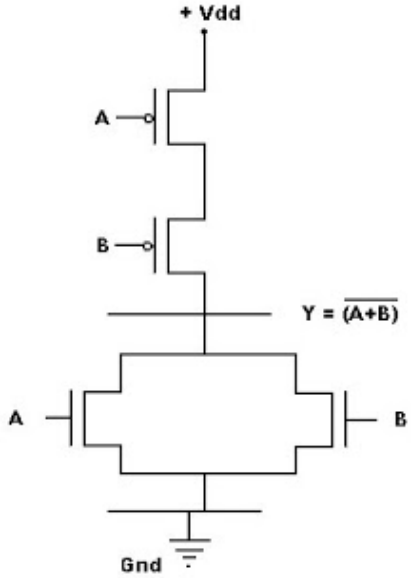
INPUT A	INPUT B	OUTPUT
0	0	1
0	1	1
1	0	1
1	1	0

CMOS NAND GATE

- When both inputs of a CMOS NAND gate are at high, then transistors T1, T2 will be ON and transistors T3, T4 will be OFF. Now there is a direct connection between output and ground through transistor T3 and T4. Output is pulled down to zero.
- When any of the input is low, either transistor T3 or T4 will be off. This breaks the connection between output terminal and ground. At the same time, one of the PMOS transistors is ON, so there is connection between output and power supply. Now output is pulled up to logic high.



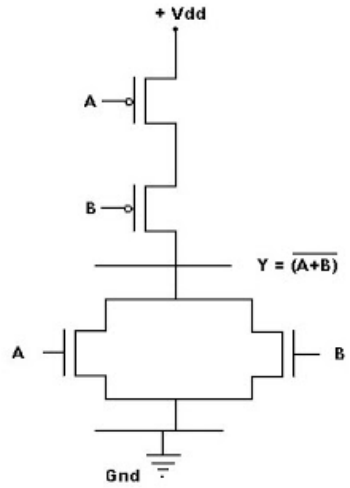
CMOS NOR GATE



INPUT A	INPUT B	OUTPUT
0	0	1
0	1	0
1	0	0
1	1	0

CMOS NOR GATE

- When both the inputs are low, the pmos devices are on as well as both the nmos devices are off. Hence output becomes logic high.
- When either of the inputs is high, i.e. A/B is at high logic, the nmos device mn1/mn2 turns on and the pmos mp1/mp2 turns off, hence the output Y is at logic low.
- When both the inputs are high, both the nmos devices conduct. As both the pmos devices are off; output becomes logic low.



MODULE 5
(TOPIC-3)

TTL
TRANSISTOR TRANSISTOR LOGIC

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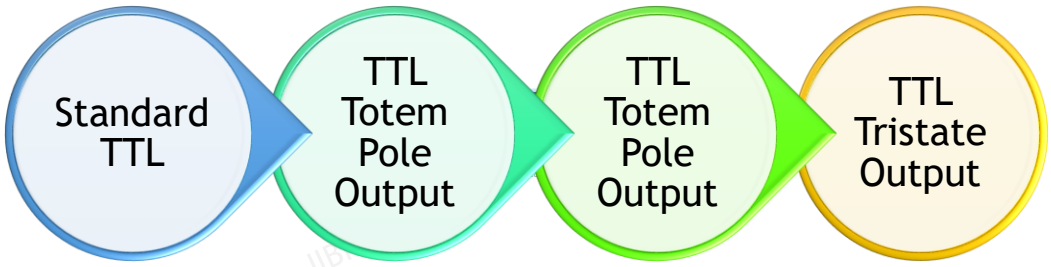
TTL

- The Transistor Tranistor Logic , TTL is named for its dependence on transistors alone to perform basic logic operations
- TTL offers higher speed compared to RTL and DTL
- The First version also known as standard TTL , was developed in 1965

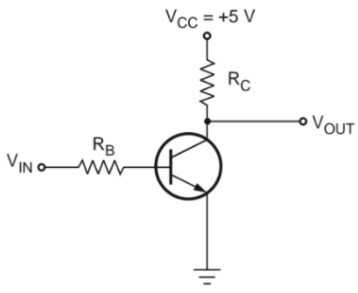
TTL CLASSIFICATIONS



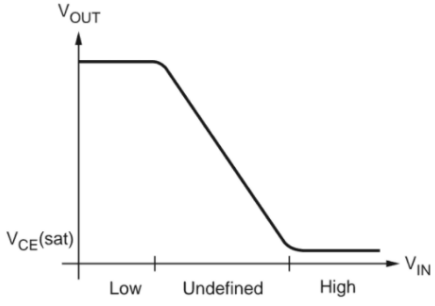
TTL INVERTER

TTL INVERTER

- We have seen that when the input voltage is LOW, the output voltage is HIGH and Vice versa
- Therefore we can make a logic inverter from an NPN Transistor in the common emitter configuration



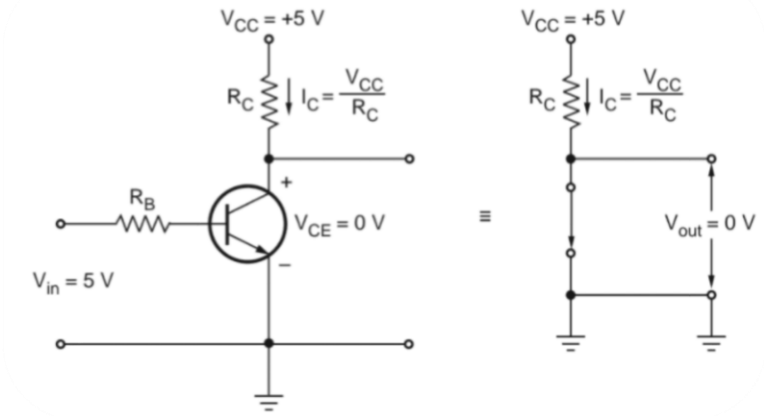
(a) Circuit diagram



(b) Transfer characteristics

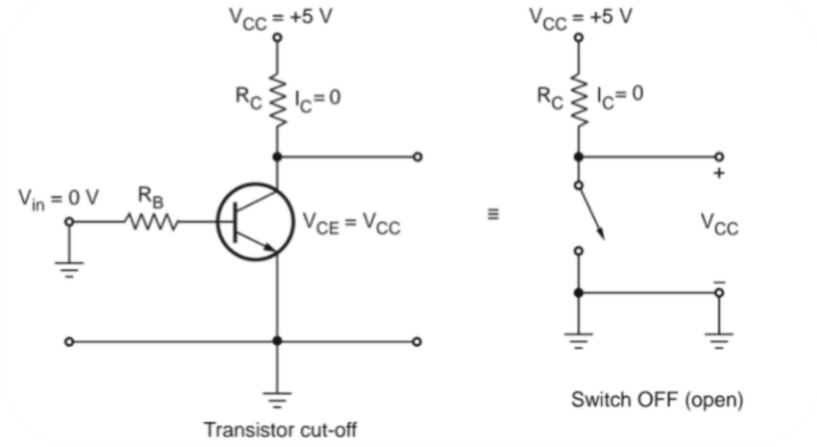
TTL INVERTER

- Figure shows the operation of transistor inverter for HIGH Input (Logic 1)
- When the input is HIGH, The output generated will be LOW (Logic 0)



TTL INVERTER

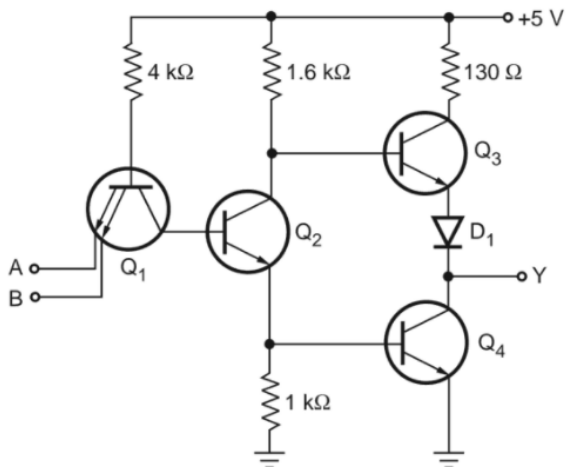
- Figure shows the operation of transistor inverter for LOW Input (Logic 0)
- When the input is LOW, The output generated will be HIGH (Logic 1)



2 INPUT TTL NAND GATE (Totem Pole)

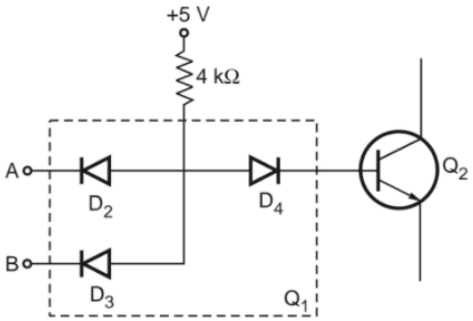
TOTEM POLE TTL NAND GATE (TWO INPUTS)

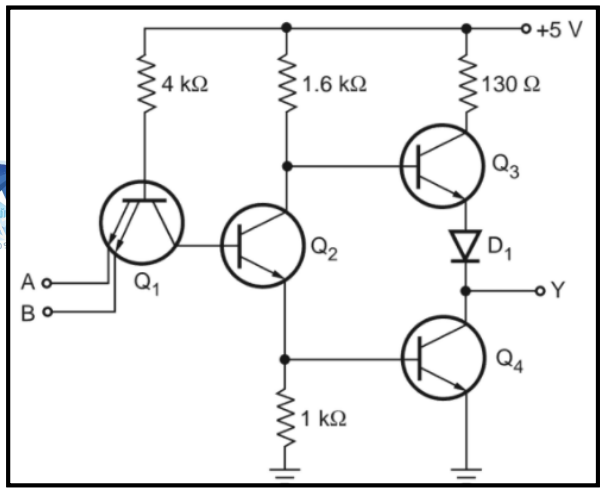
- Figure shows the circuit diagram of two input NAND Gate
- Its input structure consist of multiple-Emitter transistor and Output structure consist of **Totem Pole Output**
- Here Q1 is NPN Transistor having two emitters , one for each input to the gate



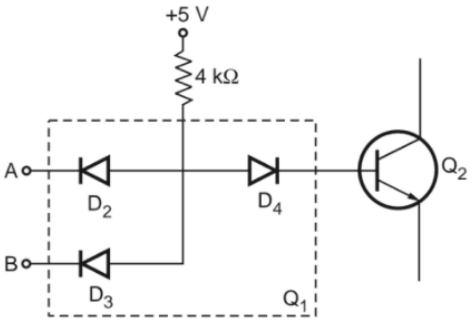
TOTEM POLE TTL NAND GATE (TWO INPUTS)

- The Diode Equivalent Circuit of Q1 is shown in figure
- The diode D2 and D3 represent two E-B Junctions of Q1 and D4 is the collector base Junction

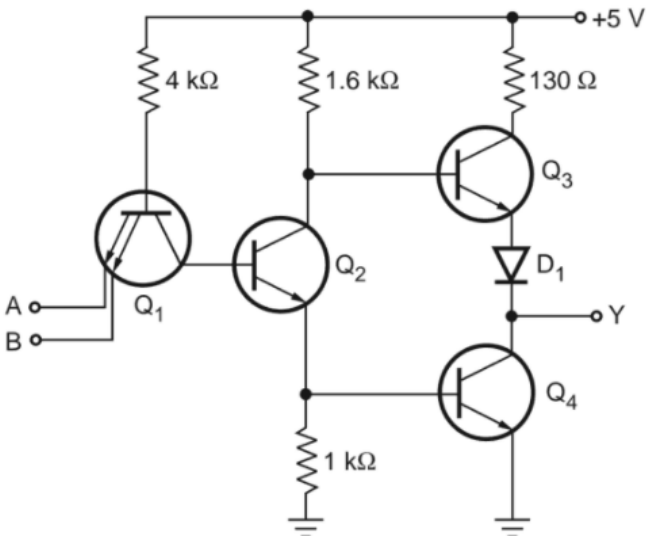




TOTEM POLE TTL NAND GATE (TWO INPUTS)

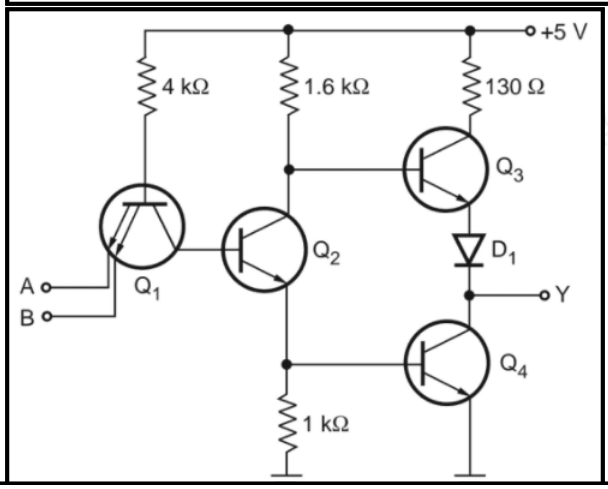


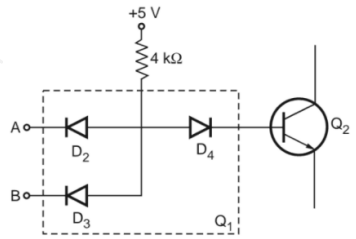
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0



CASE 1

- If either A or B or both are low, the corresponding diode conducts and the base of Q_1 is pulled down to approximately 0.7 V. This reduces the base voltage of Q_2 to almost zero. Therefore, Q_2 cuts off. With Q_2 open , Q_4 goes into cut-off and the Q_3 base is pulled HIGH. Since Q_3 acts as an emitter follower, the Y output is pulled up to a HIGH voltage.

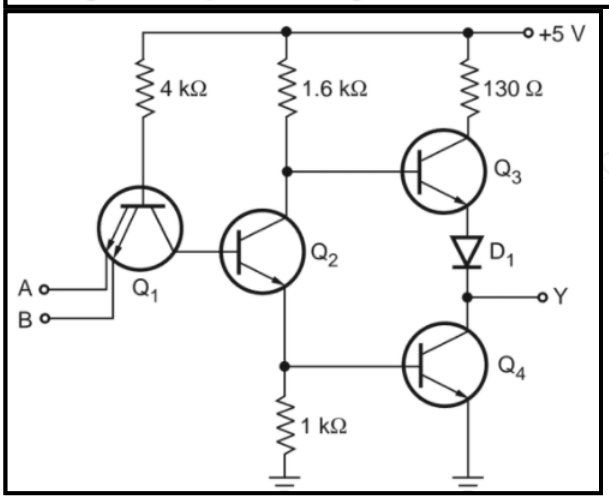


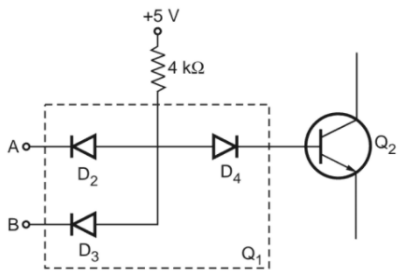


A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

CASE 2

- When A and B both are HIGH, the emitter diode of Q_1 are reversed biased making them off. This causes the collector diode D_4 to go into forward conduction. This forces Q_2 base to go HIGH. In turn, Q_4 goes into saturation, producing a low output.



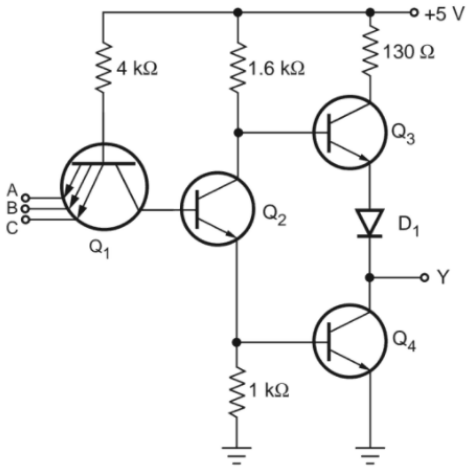


A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

3 INPUT TTL NAND GATE (Totem Pole)

TOTEM POLE TTL NAND GATE (THREE INPUTS)

- Figure shows the circuit diagram of three input NAND Gate
- It is same as that of two input TTL NAND gate except that Q1 transistor has three emitters instead of two

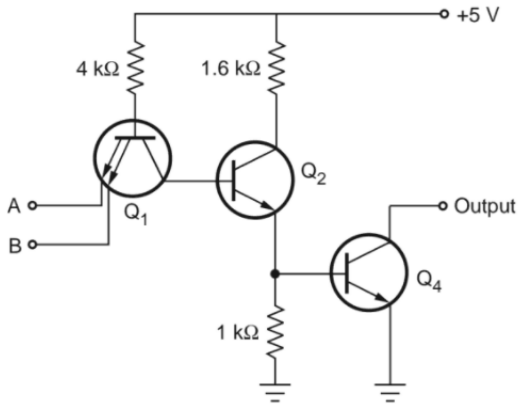


A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

2 INPUT TTL NAND GATE (Open Collector)

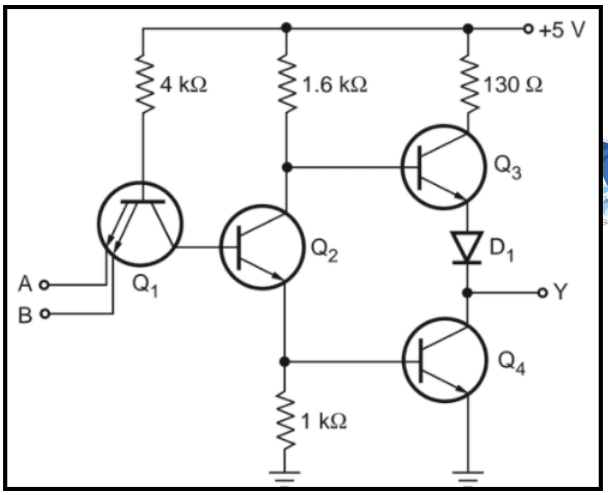
OPEN COLLECTOR TTL NAND GATE (TWO INPUTS)

- Some TTL Devices Provide another type of Output called **Open Collector Output**
- The Output of two different gates with open collector output can be tied together
- Figure shows two input NAND Gate with an open collector output eliminates the pull up transistor Q3 , D1 and R4
- The Output is taken from open collector terminal of Q4

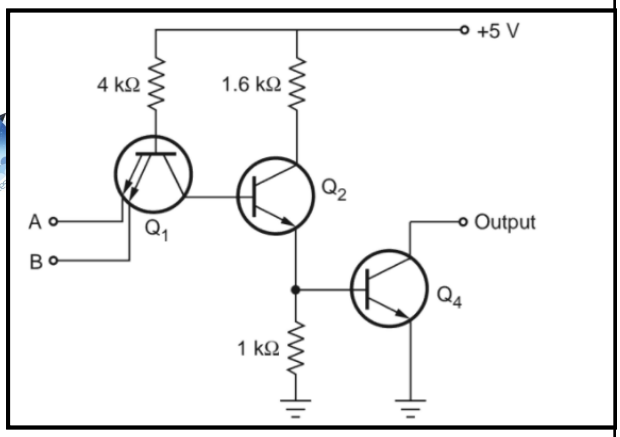


OPEN COLLECTOR TTL NAND GATE (TWO INPUTS)

TOTEM POLE NAND GATE TTL

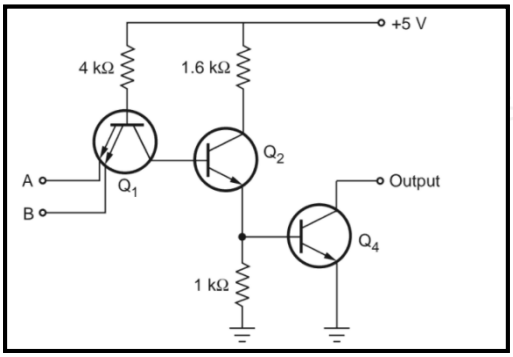


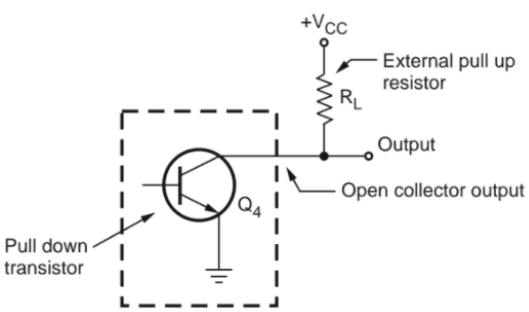
OPEN COLLECTOR NAND GATE TTL



OPEN COLLECTOR TTL NAND GATE (TWO INPUTS)

- Because of collector of Q4 is open , a gate like this will not work properly until you connect an external pull up resistor
- When Q4 is ON, Output is LOW and When Q4 is OFF, Output is tied to VCC through an external pull up resistor





STANDARD TTL CHARACTERISTICS

Characteristics	Values
Supply voltage	For 74 series - (4.75 to 5.25) units For 54 series - (4.5 to 5.5) units
Temperature range	For 74 series - (0 °C to 70 °C) For 54 series - (– 55 °C to 125 °C)
Voltage levels	$V_{OL(max)}$ = 0.4 V $V_{OH(min)}$ = 2.4 V $V_{IL(max)}$ = 0.8 V $V_{IH(min)}$ = 2.0 V
Current levels	$I_{OH(max)}$ = – 400 μA $I_{IH(max)}$ = 40 μA $I_{OL(max)}$ = 16 mA $I_{IL(max)}$ = – 1.6 mA

STANDARD TTL CHARACTERISTICS

Characteristics	Values
Noise margin	0.4 V $V_{NH} = V_{OH(min)} - V_{IH(min)} = 2.4 - 2 = 0.4$ V $V_{NL} = V_{IL(max)} - V_{OL(max)} = 0.8 - 0.4 = 0.4$ V
Power dissipation	10 mW per gate
Propagation delay	Typically 10 ns
Fan-out	High State Fan-out = $\frac{\lvert I_{OH(max)} \rvert}{I_{IH(max)}} = \frac{\lvert -400\ \mu A \rvert}{40\ \mu A} = 10$ Low State Fan-out = $\frac{I_{OL(max)}}{\lvert I_{IL(max)} \rvert} = \frac{16\ mA}{\lvert -1.6\ mA \rvert} = 10$

ADVANTAGES AND DISADVANTAGES OF TTL

Advantages of TTL

1. High speed operation. Fastest among the saturated logic families. The propagation delay time is about 10 ns.
2. Moderate power dissipation.
3. Available in commercial and military versions.
4. Available for wide range of functions.
5. Low cost.
6. Moderate packaging density.

Disadvantages of TTL

1. Higher power dissipation than CMOS.
2. Lower noise immunity than CMOS.
3. Less fan-out than CMOS.

CURRENT AND VOLTAGE PARAMETERS

$V_{IH\ (min)}$ - High-Level Input Voltage : It is the minimum voltage level required for a logical 1 at an input. Any voltage below this level will not be accepted as a HIGH by the logic circuit.

$V_{IL\ (max)}$ - Low-Level Input Voltage : It is the maximum voltage level required for a logic 0 at an input. Any voltage above this level will not be accepted as a LOW by the logic circuit.

$V_{OH\ (min)}$ - High-Level Output Voltage : It is the minimum voltage level at a logic circuit output in the logical 1 state under defined load conditions.

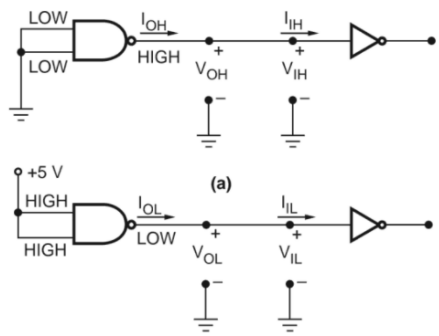
$V_{OL\ (max)}$ - Low-Level Output Voltage : It is the maximum voltage level at a logic circuit output in the logical 0 state under defined load conditions.

I_{IH} - High-Level Input Current : It is the current that flows into an input when a specified high-level voltage is applied to that input.

I_{IL} - Low-Level Input Current : It is the current that flows into an input when a specified low-level voltage is applied to that input.

I_{OH} - High-Level Output Current : It is the current that flows from an output in the logical 1 state under specified load conditions.

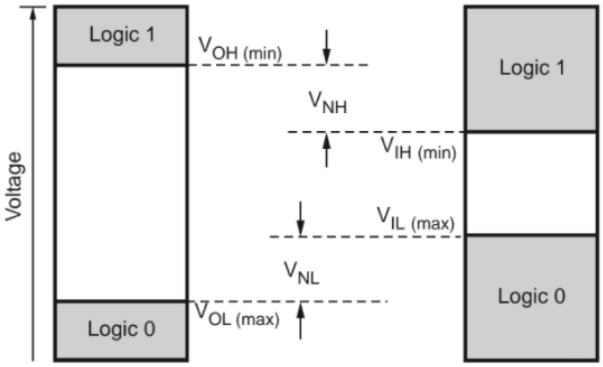
I_{OL} - Low-Level Output Current : It is the current that flows from an output in the logical 0 state under specified load conditions.



NOISE MARGIN

$$V_{NH} = V_{OH(MIN)} - V_{IH(MIN)}$$

$$V_{NL} = V_{IL(MAX)} - V_{OL\,(MAX)}$$



COMPARISON OF TTL AND CMOS

Sr. No.	Parameter	CMOS	TTL
1.	Device used	n-channel and p-channel MOSFET	Bipolar junction transistor
2.	$V_{IH(min)}$	3.5 V	2 V
3.	$V_{IL(max)}$	1.5 V	0.8 V
4.	$V_{OH(min)}$	4.95 V	2.7 V
5.	$V_{OL(max)}$	0.005 V	0.4 V
6.	High level noise margin	V_{NH} = 1.45 V	0.4 V
7.	Low level noise margin	V_{NL} = 1.45 V	0.4 V
8.	Noise immunity	Better than TTL	Less than CMOS

COMPARISON OF TTL AND CMOS

Sr. No.	Parameter	CMOS	TTL
9.	Propagation delay	70 ns	10 ns
10.	Switching speed	Less than TTL	Faster than CMOS
11.	Power dissipation per gate	0.1 mW	10 mW
12.	Speed power product	0.7 pJ	100 pJ
13.	Fan-out	50	10
14.	Power supply voltage	3 - 15 V	Fixed 5 V
15.	Power dissipation	Increase with frequency	Increase with frequency
16.	Application	Portable instrument where battery supply is used.	Laboratory instruments.

MODULE 5
(TOPIC-4)

ECL
EMITTER COUPLED LOGIC

JIBIN EP

INDEX

https://youtu.be/RSgjzUWJ2PE YouTube

EMITTER COUPLED LOGIC

- Emitter-coupled logic is the fastest of all digital logic families. It is also called as current mode logic.
- The design of ECL circuit consists of transistors and resistors.
- Emitter-coupled logic family offers an *incredible propagation delay of 1ns*. The delay is more reduced in the latest ECL families.
-

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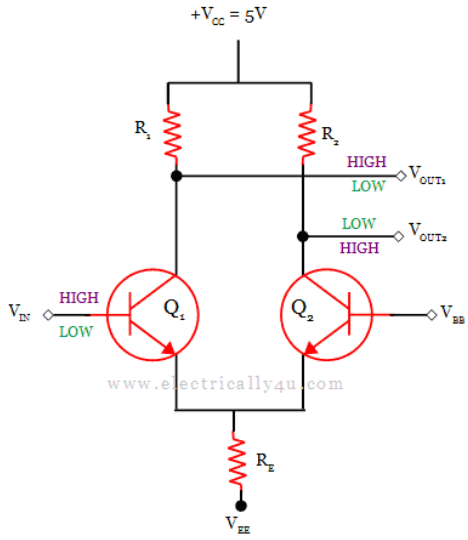
ECL INVERTER

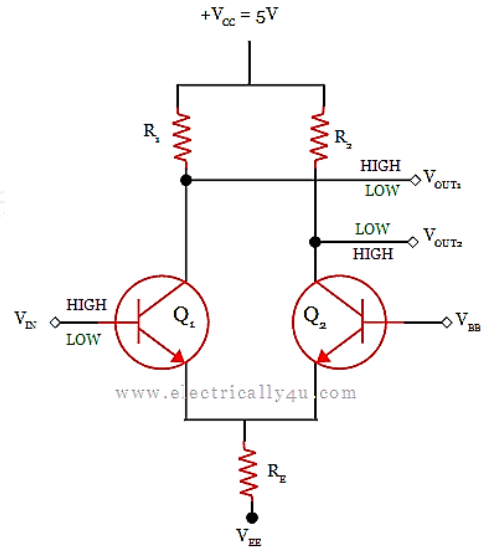
INVERTER CIRCUIT OF EMITTER COUPLED LOGIC

- The circuit shown below represents the emitter-coupled logic circuit of an inverter. It has two NPN transistors connected in differential single-ended input mode.
- Both the emitters are connected together with common resistance RE. It is a current limiting resistance, used to prevent the transistor from entering into saturation.
- It has two outputs: inverting output(VOUT1) and non-inverting output(VOUT 2). VIN is the input terminal, where LOW or HIGH input is given.



INVERTER CIRCUIT OF EMITTER COUPLED LOGIC

- When the input is HIGH, it will turn ON the transistor Q_1 but not saturated and the transistor Q_2 is turned OFF. This will pull the output V_{OUT2} to HIGH but due to the drop in resistant R_1, the output at terminal V_{OUT1} will be at LOW value.
- On the other side, when the input V_{IN} is given LOW value, it will turn OFF the transistor Q_1 and the transistor is turned ON. The transistor Q_2 will not enter into saturation.
- It will make the output at terminal V_{OUT1} to be pulled HIGH value. Due to the drop in resistance R_2, the output at terminal V_{OUT2} will have LOW value.



ADVANTAGES AND DISADVANTAGES OF ECL

Advantages

- Fastest Logic Family

- **Disadvantages**
- High cost
- Low noise margin
- High Power Dissipation
- Problem of Cooling

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CHARACTERISTICS OF ECL

1. Transistors never saturate. So, speed is high with t_{pd} = 1 ns.
2. Logic levels are negative, – 0.9 V for a logic 1 and – 1.7 V for a logic 0.
3. Noise margin is less, about 250 mV. This makes ECL unreliable for use in heavy industrial environment.
4. ECL circuits produce the output and its complement, and therefore, eliminate the need for inverters.
5. Fan-out is large because the output impedance is low. It is about 25.
6. Power dissipation per gate is large, P_D = 40 mW.
7. The total current flow in ECL is more or less constant. So, no noise spikes will be internally generated.

KTU MODEL QUESTION PAPER QUESTIOS

9	Define fan-in and fan-out of logic circuits.	(3)	K_2
10	Define noise margin and how can you calculate it?	(3)	K_2

Module V

19(A)	Explain in detail about TTL with open collector output configuration.	(8)	K_2
19(B)	Draw an ECL basic gate and explain.	(6)	K_2

OR

20(A)	Demonstrate the CMOS logic circuit configuration and characteristics in detail.	(8)	K_2
20(B)	Compare the characteristics features of TTL and ECL digital logic families	(6)	K_2