COMPUTER ORGANIZATION
AFYG 16-BIT
PROCESSOR DESIGN

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Instructions:

R-type:	I-type	J-type
Add -> 0000-000	Addi -> 0010	J -> 1100
Sub -> 0000-001	Andi -> 0011	Jal -> 1101
And -> 0000-010	Ori -> 0100	
Or -> 0000-011	Beq -> 0101	
Xor -> 0000-100	Bne -> 0110	
Sll -> 0000-101	Lb -> 0111	
Srl -> 0000-110	Lw -> 1000	
Slt -> 0000-111	Sb -> 1001	
Jr -> 0001-000	Sw -> 1010	
Mult -> 0001-001	Slti -> 1011	
Mfhi -> 0001-010		
Mflo -> 0001-011		

Registers:

Name	Number	Use case	Preserved
$zero	000	constant0	N.A.
$t0	001	temporary	No
$t1	010	temporary	No
$t2	011	temporary	No
$t3	100	temporary	No
$s0	101	saved temporary	Yes
$s1	110	saved temporary	Yes
$ra	111	return address	No
$pc	X	programming counter	X
$hi	X	high	X
$lo	X	low	X

Instruction Formats:

R-Type				
OP Code 4-bit 15 - 12	Reg S. 3-bit 11 - 9	Reg T. 3-bit 8 - 6	Reg D. 3-bit 5 - 3	Func. 3-bit 2 - 0
I-Type				
OP Code 4-bit 15 - 12	Reg S. 3-bit 11 - 9	Reg T. 3-bit 8 - 6	Immediate 6-bit 5 - 0	
J-Type				
OP Code 4-bit 15 - 12	Address 12-bit 11 - 0			

Alu Control Lines:

Mnemonic	Frmt	RegDst	AluSrc	MemToReg	RegWrt	MemRd	MemWrt	Branch	Jmp	JReg	JLink	ALUOP2	ALUOP1	ALUOP0
Add	R	1	0	0	1	0	0	0	0	0	0	0	1	0
Sub	R	1	0	0	1	0	0	0	0	0	0	0	1	0
And	R	1	0	0	1	0	0	0	0	0	0	0	1	0
Or	R	1	0	0	1	0	0	0	0	0	0	0	1	0
Xor	R	1	0	0	1	0	0	0	0	0	0	0	1	0
Sll	R	1	0	0	1	0	0	0	0	0	0	0	1	0
Srl	R	1	0	0	1	0	0	0	0	0	0	0	1	0
Slt	R	1	0	0	1	0	0	0	0	0	0	0	1	0
Jr	R	1	0	0	0	0	0	0	0	1	1	X	X	X
Addi	I	0	1	0	1	0	0	0	0	0	0	0	0	0
Andi	I	0	1	0	1	0	0	0	0	0	0	0	1	1
Ori	I	0	1	0	1	0	0	0	0	0	0	1	0	1
Beq	I	0	1	0	0	0	0	1	0	0	0	0	0	1
Bne	I	0	1	0	0	0	0	1	0	0	0	0	0	1
Lb	I	0	1	1	1	1	0	0	0	0	0	0	0	0
Lw	I	0	1	1	1	1	0	0	0	0	0	0	0	0
Sb	I	0	1	0	0	0	1	0	0	0	0	0	0	0
Sw	I	0	1	0	0	0	1	0	0	0	0	0	0	0
Slti	I	0	1	0	1	0	0	0	0	0	0	1	1	1
J	J	0	0	0	0	0	0	0	1	0	0	X	X	X
Jal	J	0	0	0	1	0	0	0	1	0	1	X	X	X

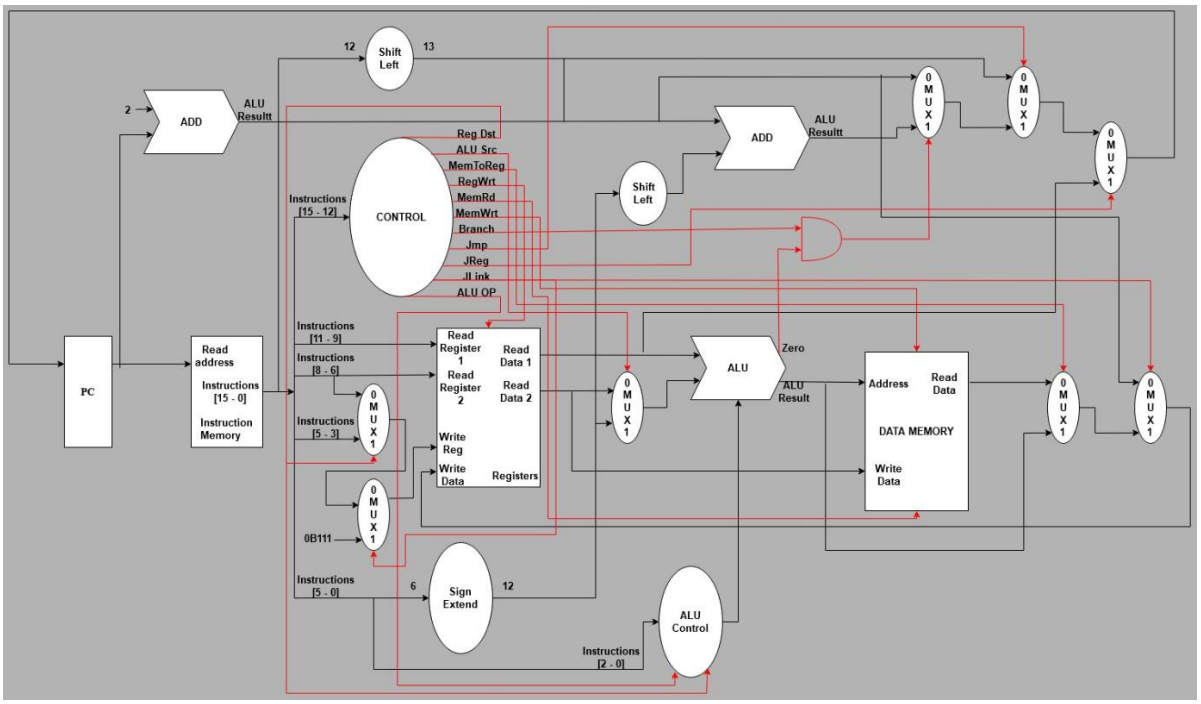
Alu Control Inputs:

MNEMONIC	ALU OP.	FUNC	ALU CONTROL INPUT
Add	010	000	010000
Sub	010	001	010001
And	010	010	010010
Or	010	011	010011
Xor	010	101	010101
Sll	110	000	110000
Srl	110	001	110001
Slt	110	011	110011
Addi	110	---	010000
Andi	011	---	010010
Ori	101	---	010011
Beq	001	---	110000
Bne	001	---	111000
Lb	000	---	011000
Lw	000	---	010000
Sb	000	---	011000
Sw	000	---	010000
Slti	111	---	110011

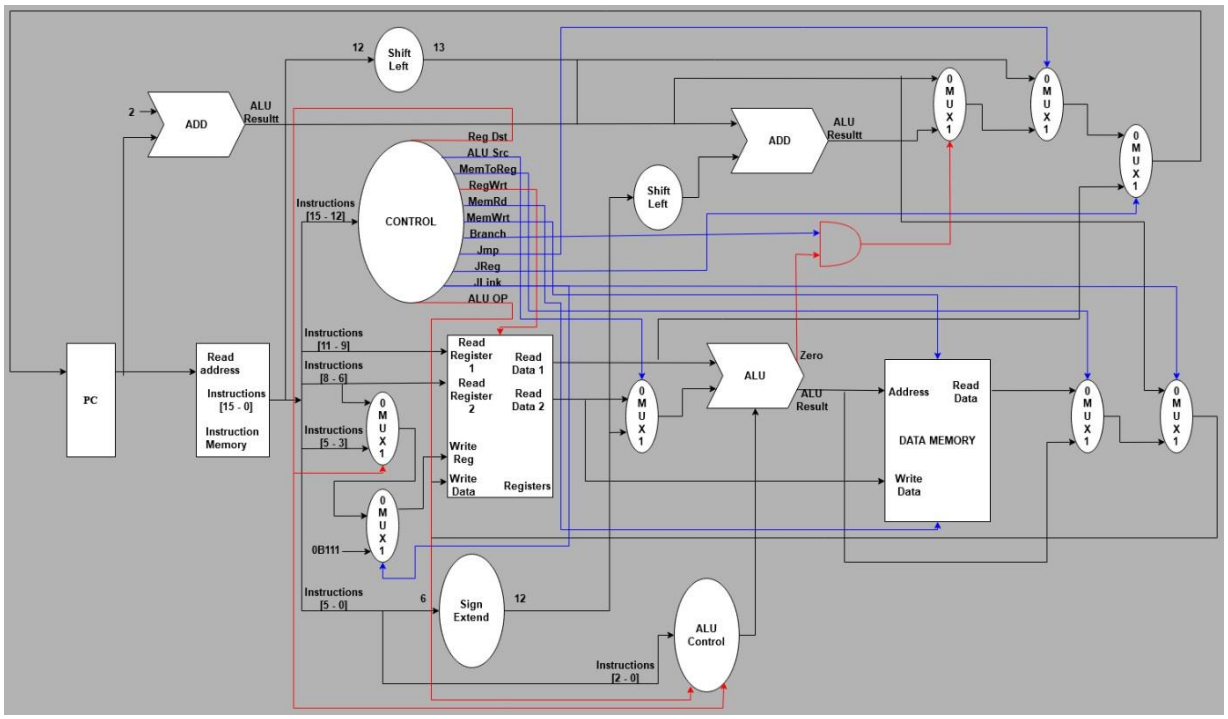
Alu Control Lines:

Control Input	ALU Function
010000	Add
010001	Sub
010010	And
010011	Or
010101	Xor
110000	Shift left
110001	Shift right
110011	Set on less than
110000	Branch on equal
111000	Branch on not equal
011000	Forward low byte
010000	Forward two bytes

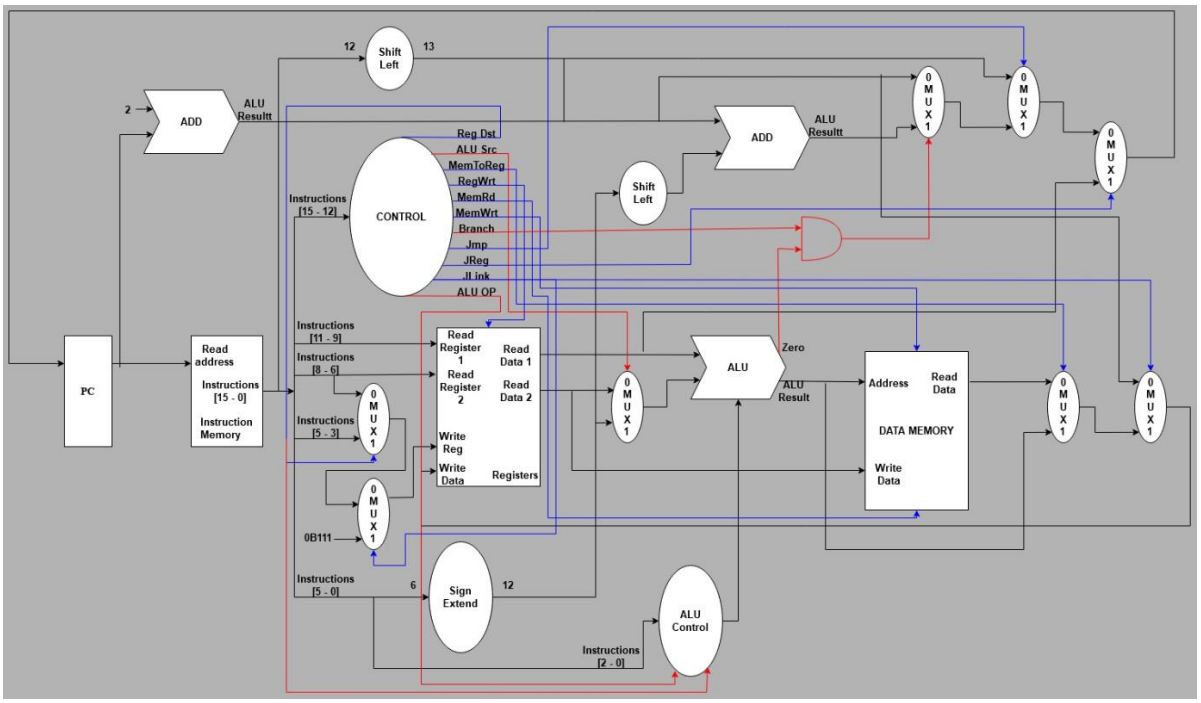
Datapath:



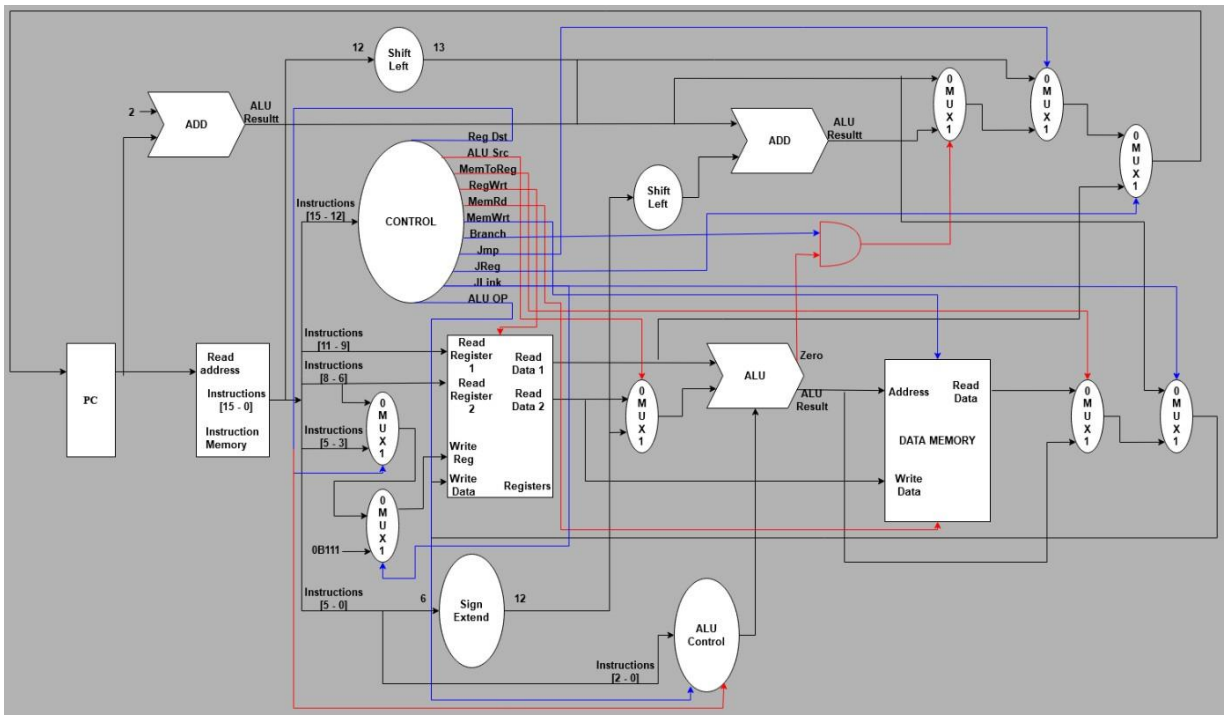
Add:


12
Shift Left
13
2
ADD
ALU Resultt
ADD
ALU Resultt
0 M U X 1
Reg Dst
ALU Src
MemToReg
RegWrt
MemRd
MemWrt
Branch
Jmp
JReg
Jl ink
ALU OP
Instructions [15 - 12]
CONTROL
Shift Left
Instructions [11 - 9]
Instructions [8 - 6]
Instructions [5 - 3]
Read Register 1
Read Register 2
Write Reg
Write Data
Read Data 1
Read Data 2
Registers
PC
Read address
Instructions [15 - 0]
Instruction Memory
0B111
Instructions [5 - 0]
6
Sign Extend
12
ALU
Zero
ALU Result
ALU Control
Instructions [2 - 0]
Address
Read Data
DATA MEMORY
Write Data

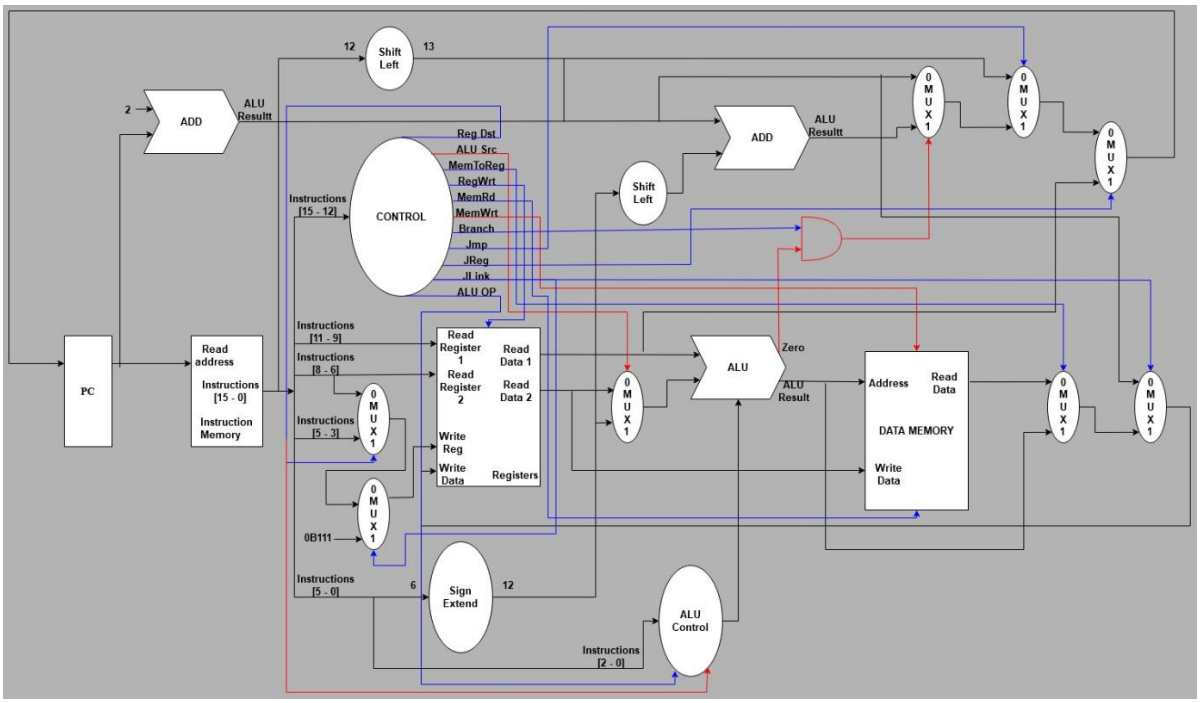
Beq:


12
Shift Left
13
2
ADD
ALU Resultt
ADD
ALU Resultt
0 M U X 1
Reg Dst
ALU Src
MemToReg
RegWrt
MemRd
MemWrt
Branch
Jmp
JReg
Jl ink
ALU OP
Instructions [15 - 12]
CONTROL
Shift Left
Instructions [11 - 9]
Instructions [8 - 6]
Instructions [5 - 3]
Read Register 1
Read Register 2
Write Reg
Write Data
Read Data 1
Read Data 2
Registers
PC
Read address
Instructions [15 - 0]
Instruction Memory
0B111
Instructions [5 - 0]
6
Sign Extend
12
ALU
Zero
ALU Result
ALU Control
Instructions [2 - 0]
Address
Read Data
DATA MEMORY
Write Data

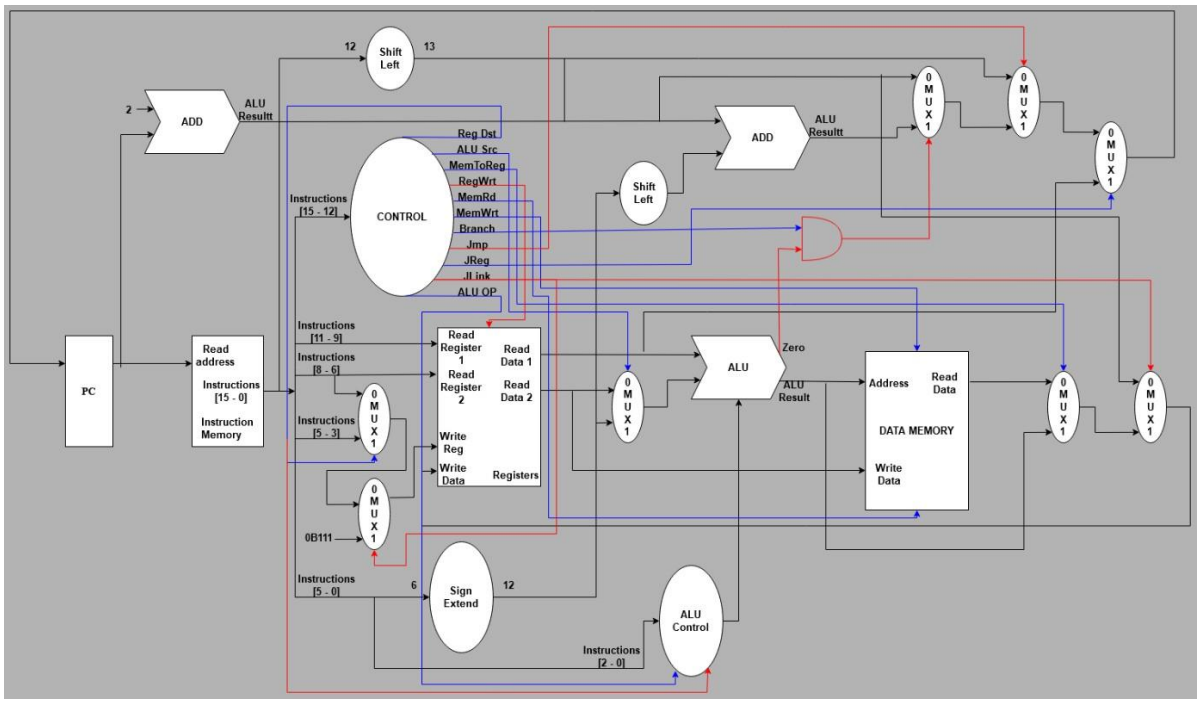
Lw:


12
Shift Left
13
2
ADD
ALU Resultt
Reg Dst
ALU Src
MemToReg
RegWrt
MemRd
MemWrt
Branch
Jmp
JReg
Jl ink
ALU OP
Instructions [15 - 12]
CONTROL
Shift Left
ADD
ALU Resultt
0 M U X 1
PC
Read address
Instructions [15 - 0]
Instruction Memory
Instructions [11 - 9]
Instructions [8 - 6]
Instructions [5 - 3]
Read Register 1
Read Register 2
Write Reg
Write Data
Read Data 1
Read Data 2
Registers
0B111
Instructions [5 - 0]
6
Sign Extend
12
ALU
Zero
ALU Result
ALU Control
Instructions [2 - 0]
Address
Read Data
DATA MEMORY
Write Data

Sw:


12
Shift Left
13
2
ADD
ALU Resultt
Reg Dst
ALU Src
MemToReg
RegWrt
MemRd
MemWrt
Branch
Jmp
JReg
Jl ink
ALU OP
Instructions [15 - 12]
CONTROL
Shift Left
ADD
ALU Resultt
0 M U X 1
PC
Read address
Instructions [15 - 0]
Instruction Memory
Instructions [11 - 9]
Instructions [8 - 6]
Instructions [5 - 3]
Read Register 1
Read Register 2
Write Reg
Write Data
Read Data 1
Read Data 2
Registers
0B111
Instructions [5 - 0]
6
Sign Extend
12
ALU
Zero
ALU Result
ALU Control
Instructions [2 - 0]
Address
Read Data
DATA MEMORY
Write Data

Jal:


12
Shift Left
13
2
ADD
ALU Resultt
ADD
ALU Resultt
0 M U X 1
Reg Dst
ALU Src
MemToReg
RegWrt
MemRd
MemWrt
Branch
Jmp
JReg
Jl ink
ALU OP
Instructions [15 - 12]
CONTROL
Shift Left
Instructions [11 - 9]
Instructions [8 - 6]
Instructions [5 - 3]
Read Register 1
Read Register 2
Write Reg
Write Data
Read Data 1
Read Data 2
Registers
ALU
Zero
ALU Result
Address
Read Data
DATA MEMORY
Write Data
PC
Read address
Instructions [15 - 0]
Instruction Memory
0B111
Instructions [5 - 0]
6
Sign Extend
12
ALU Control
Instructions [2 - 0]