## ISLAMIC UNIVERSITY OF TECHNOLOGY (IUT) ORGANISATION OF ISLAMIC COOPERATION (OIC)

## Department of Computer Science and Engineering (CSE)

## MID SEMESTER EXAMINATION

SUMMER SEMESTER, 2017-2018

**DURATION: 1 Hour 30 Minutes** 

**FULL MARKS: 75** 

## CSE 6269: Embedded Systems Design

Programmable calculators are not allowed. Do not write anything on the question paper. There are <u>4 (four)</u> questions. Answer any <u>3 (three)</u> of them including Question 1 (mandatory). Figures in the right margin indicate marks.

1.	a) b)	[Mandatory] Briefly describe the architecture of Arduino board. In IUT, a smart classroom has been designed that operates with a controlling smart card. With the touch of the controlling card, the computer, air conditioners, attendance system, smart boards are enabled. Briefly describe the architecture, sensor and actuator deployment for the smart class.	10 15
2.	a)	ADC being cheaper than dealing with analog signal, many cases sensor values are <i>oversampled</i> . But the oversampling has an impact on the actuator responding to the sensor. A bang-bang controller needs to smooth the response of the actuator. In a lift, there is a sensor attached to its door that should respond to any movement. However, the response of the door should be carefully designed. Comment of the design considerations of the door of a lift.	7
	b)	Briefly describe the design principle of an accelerator and a gyroscope including their	10
	c)	MEMS implementation.  Describe the relations of modeling, design and analysis of embedded system development.	8
3.	a) b) c)	Describe the six degree of freedom of any locomotive.  Explain the role of Newton's second law to derive the velocity and position from acceleration of the six degree of freedom.  How does model-order reduction help simplifying the modeling?	7 10 8
4.	a) b) c)	Describe the edit-test-debug cycle of developing embedded applications.  What is cross-compilation?  Write a short note on (any three):  i. Micro controller  ii. DSP processor  iii. FIR Filter  iv. RISC vs. CISC processor  v. Processor Pipeline  vi. ISA vs. Embedded Processor	5 5 3×5