B.Sc. Engg. / HD CSE 3rd Semester (65) 23 May 2016

ISLAMIC UNIVERSITY OF TECHNOLOGY (IUT)
ORGANISATION OF ISLAMIC COOPERATION (OIC)
Department of Computer Science and Engineering (CSE)

SEMESTER FINAL EXAMINATION **WINTER SEMESTER, 2015-2016**

DURATION: 3 Hours **FULL MARKS: 150**

CSE 4305: Computer Organization and Architecture

Programmable calculators are not allowed. Do not write anything on the question paper.

There are **8 (eight)** questions. Answer any **6 (six)** of them.

Figures in the right margin indicate marks.

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1. a) Name the five classic components of a computer. What is the difference between "Computer Organization" and "Computer Architecture"? Explain. 5+5

   b) A program runs in 10 seconds on computer X, which has a 2 GHz clock. You are trying to build a computer Y, which will run the program in 6 seconds. You have determined that an increase in the clock rate is possible, but then computer Y will require 1.8 times as many clock cycles as computer X for the program. What should be the clock rate of computer Y to achieve this? 8

   c) Describe the power wall and discuss the implications. How are computer designers coping up with the power wall? 4+3

2. a) What is pipelining? How can you calculate the pipeline speedup in ideal conditions? 4+3

   b) The latencies of the individual stages of a datapath are given in Table 1. 8

Table 1: Datapath component latency

IF	ID	EX	MEM	WB
300ps	400ps	350ps	500ps	100ps

Answer the following questions:

i. What is the clock cycle time in a pipelined and nonpipelined processor?

ii. What is the total latency of a '"lw" instruction in a pipeline and nonpipelined processor?

   c) Consider the MIPS instruction `lw $1, 40($6)`. As this instruction executes, describe the data that are kept in each of the pipeline registers (IF/ID, ID/EX, EX/MEM, MEM/WB). 10

3. a) What is dynamic branch prediction? Draw the finite-state machine for a 2-bit prediction scheme. 10

   b) Figure 1 shows a simplified view of the ALU and pipeline registers without any forwarding. Redraw the diagram with the necessary multiplexers, the forwarding unit, and the data and control lines to implement forwarding. 8

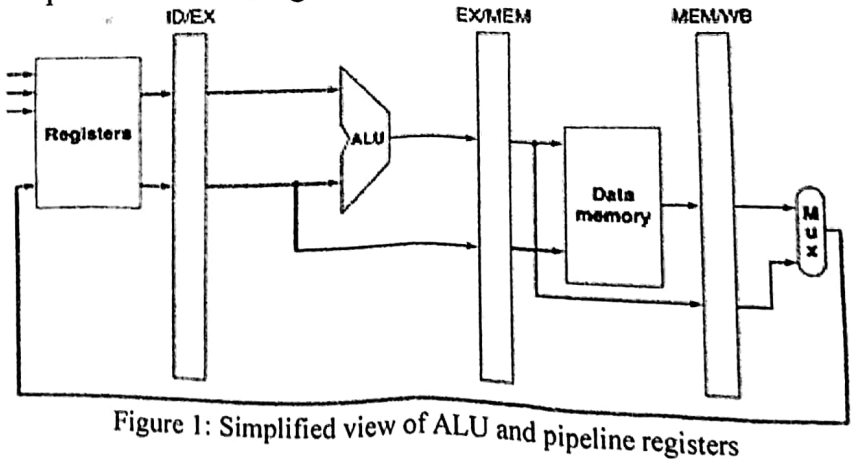

Figure 1: Simplified view of ALU and pipeline registers

c) Describe a situation when a data hazard is not solvable even with forwarding. What can you do to solve this? 3+4

4. a) Given below is a list of 32-bit memory address references, given as word addresses. For each of these references, identify the binary address, the tag, and the index given a direct-mapped cache with 16 one-word blocks. Moreover, list if each reference is a hit or miss, assuming the cache is initially empty. 15

1, 134, 212, 1, 135, 213, 162, 161, 2, 44, 41, 221

b) Answer the following questions with respect to Translation Lookaside Buffer (TLB): 10

i. What kind of memory mapping do you use in TLB? Why?
ii. How do you handle TLB misses?

5. a) Describe the schemes "write-through" and "write-back". 8
b) What is the effect of increasing memory width on memory bandwidth? 5
c) Assuming a cache of 4K blocks, a 4-word block size, and a 32-bit address, find the total number of sets and total number of tag bits for the following cache setups: 4×3

i. Direct mapped
ii. Two-way set associative
iii. Four-way set associative
iv. Fully associative

6. a) Describe two major advantages of virtual memory. 7
b) Given the following virtual memory parameters, calculate the total size of the page table for each case. 8

i. 32 bits virtual address, 4 KB page size, 4 bytes per page table entry
ii. 64 bits virtual address, 16 KB page size, 8 bytes per page table entry

c) Assume that main memory access take 70 ns and that memory access are 36% of all instructions. The following table shows data for L1 caches attached to each of two processors, P1 and P2.

Table 2: L1 cache characteristics

	L1 miss rate	L1 hit time
P1	3.4%	1.08 ns
P2	2.9%	2.02 ns

Answer the following questions:

i. Assuming that the L1 hit time determines the cycle times for P1 and P2, what are their respective clock rates? 2
ii. What is the AMAT for each of P1 and P2? 4
iii. Assuming a base CPI (i.e., without stalls) of 1.0, what is the total CPI (i.e., considering the memory stalls) for each of P1 and P2? Which processor is faster? 4

7. a) Compare between implementing parallel processing in hardware and software. 7
b) Suppose you want to perform two sums: one is a sum of 20 scalar variables, and one is a matrix sum of a pair of two-dimensional arrays, with dimensions 20 by 20. 6+6

i. What speed-up do you get with 10 versus 100 processors?
ii. What speed-up do you get with 10 versus 100 processors given the matrices grow to be 1000 by 1000.

c) Compare and contrast between Shared Memory Multiprocessors (SMP) and Clusters with respect to the following criteria: 6

i. Cost
ii. Expandability

8. a) Why is it important to improve the speed of I/O? Name five of the most popular I/O standards. 4+5

b) Suppose you are given a Disk drive with a MTTF of 3 years and MTTR of 1 day. Answer the following questions: 4×2

i. Calculate the MTBF of the device.
ii. Calculate the Availability of the device.
iii. What happens to availability if the MTTR approaches to 0? Is this a realistic situation?
iv. What happens to availability if the MTTR gets very high, i.e., a device is difficult to repair? Does this imply the device has low availability?

c) Consider two I/O devices- a video game controller and computer monitor. Answer the following questions: 2×4

i. What is polling? Would each of the mentioned devices be appropriate for polling? Explain.
ii. What is interrupt-driven communication? Would each of the mentioned devices be appropriate for interrupt-driven I/O? Explain.