ISLAMIC UNIVERSITY OF TECHNOLOGY (IUT) ORGANISATION OF ISLAMIC COOPERATION (OIC)

Department of Computer Science and Engineering (CSE)

SEMESTER FINAL EXAMINATION

WINTER SEMESTER, 2016-2017

DURATION: 3 Hours

FULL MARKS: 150

CSE 4503: Microprocessors and Assembly Language

Programmable calculators are not allowed. Do not write anything on the question paper.

There are 8 (eight) questions. Answer any 6 (six) of them.

Figures in the right margin indicate marks.

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1	. a)	i. What is PLT and GOT?	6
		ii. What's the motivation for using PLT stub as function trampoline?	v
	b)	iii. Why NOT call the shared library functions directly? Explain how PLT and GOT is used to resolve the base address for any function from any	
	U)	shared libraries which is compiled with Position Independent Code parameter. (3 states)	6
	c)	What is meant by the term Buffer Overflow? How has this problem been resolved in the	5
		existing Linux library?	
	. d)	Code to call a function with 3 parameters from "_start" stub in intel x86 architecture. Demonstrate the same code in x86_64 architecture.	8
		and summer the same source in x00_04 architecture.	
2.	a)	The and the second of the seco	4
	b)	term 'Global' and 'Offset' in it? Show the byte representation of the following commands-	
	0)	i. MOV AX, [6072H]	6
	-)	ii. MOV CX, DX	
	· c)	Write two assembly programs, Program-I will take input and display the inputs (see test case) and store it in the stack.	15
		Consider the content of the stack won't change.	
		Now, Program-II will take the values from stack and display the outputs as shown below.	
		Program-II Program-II	
		Enter Dividend: 10 Quotient: 3	
		Enter Divisor: 3 Remainder: 1	·M
		Note: Dividend will be maximum of 2 digits and divisor of at maximum 1 digit.	
3.	a)		6
	b)	Explain steps of how interrupt is processed in 8086 microprocessors? How does 8086 get	6
	c)	the address of any particular Interrupt Service Routine? How is the 'Interrupt Vector Table' and 'Interrupt Service Routine' related? Specify, what	
		they note and why.	6
	d)	Explain Call and return mechanism for a near procedure and show how the IP and Stack	7
		are affected by procedure calls.	
•	a)	Analyze the given code:	4
		section .data	7.
		1. name db "/bin/sh"	
		section .text	
	2	global _start	
	4	start:	
		push 0	

push name 3. mov rax,59 4. mov rdi,rsp 5. 6. mov rsi,0 7. mov rdx,0 Write comments for instructions 1 to 8. Mention for what purpose the instructions have 6 Write down the significance of Accumulator register before and after function calls by 15 conventional programming. Remove the NULL bytes from the given stub to generate a new code in 32bit assembly which can be used as a shellcode to exploit buffer. [You can work with decimal of the respective hex values, i.e. 10d= 0xA1 file format elf32-i386 shell: Disassembly of section .text: 08048060 < start>: eax,0x66 mov b8 66 00 00 00 8048060: mov ebx,0x1bb 01 00 00 00 8048065: push 0x0 804806a: 6a 00 push 0x1 6a 01 804806c: push 0x2 6a 02 804806e: mov ecx,esp 89 e1 8048070: int 0x80 8048072: cd 80. edx,eax 89 c2 mov 8048074: eax,0x66 ь8 66 00 00 00 mov 8048076: ebx,0xe bb 0e 00 00 00 nıov 804807b: push 0x4 6a 04 8048080: 54 push esp 8048082: push 0x2 6a 02 8048083: push 0x1 6a 01 8048085: push edx 52 8048087: ecx,esp 8048088: 89 e1 mov 0x80cd 80 int 804808a: eax,0x66b8 66 00 00 00 804808c: mov ebx,0x2 8048091: bb 02 00 00 00 mov push 0x0 8048096: 6a 00 pushw 0x672b 66 68 2b 67 8048098: 804809c: 66 6a 02 pushw 0x2 804809f: 89 e1 mov ecx,esp 80480a1: 6a 10 push 0x10 80480a3: 51 push ecx 80480a4: 52 push edx 80480a5: 89 e1 mov ecx,esp 80480a7: cd 80 int 0x80Draw and add a brief explanation of the flag register in 80286. What are the new flags 6+4 introduced in 80386 and 80486? b) Draw the flow diagrams for the three I/O data transfer techniques and label the states. 15 State the differences of Memory mapped I/O and Isolated I/O with figures. a) 4 "Software interrupts are prioritized more than the hardware interrupts when they occur at b) the same time" - justify the statement. Suppose, a multicore processor was carrying out multiple instructions which is obvious. 9

5.

6.

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Also, each of the core was responsible for parallel execution of multiple instructions. How
        Contrast the ideas of Pipelining and Superscalar property in microprocessors.
        Briefly mention and explain the pipelining stages of Floating Point Unit.
                                                                                                      8
        What is an addressing mode? What are different addressing modes? Explain Based
7.
                                                                                                      8
        Indexed addressing modes.
       Write some instructions to replace each upper-case letter in the following string by lower
   b)
                                                                                                       7
        case equivalent using Base addressing mode.
                          MSG DB 'LIFE IS GOOD',$
       The algorithm given below multiplies two unsigned numbers A and B. Using the
  c)
                                                                                                       10
       algorithm, write a procedure MULTIPLY to multiply two numbers A and B.
       [Assume, A and B are already stored in AX and BX.]
               Product = 0
               REPEAT
                       IF LSB of B is 1
                       THEN
                       Product = Product + A
                       END IF
                       Shift left A
                       Shift right B
                UNTIL B=0
                                                                                                        7
         Given,
     a)
                                       MOV EAX, 0x2002b2(RIP)
          Accessing the offset from RIP register is possible only in x86_64 architecture, show how
          this is handled in x86 architecture.
          What is the necessity of using stack segment in assembly language programming? With
                                                                                                       6
          suitable examples demonstrate how to perform push and pop operation in stack.
          What's the purpose of stack pointer(SP) and Base Pointer (BP) registers? Show the
                                                                                                    2+10
          changes in the stack as the function foo executes. Show each state of changes till the stack
          becomes empty again. Initial stack state is NULL.
                                                void foo(int a, char b, int c){
                 int main() {
                                                    int k:
                        foo(3,'A',10);
                                                    k=a;
                        return 0;
                                                    if(k>0)
                 }
                                                          foo(k, 'A', 10);
                                                    else return;
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