B.Sc. Engg. / HD CSE 3rd Semester (67)

08 March 2016 (Morning)

ISLAMIC UNIVERSITY OF TECHNOLOGY (IUT)
ORGANISATION OF ISLAMIC COOPERATION (OIC)
Department of Computer Science and Engineering (CSE)

MID SEMESTER EXAMINATION — **WINTER SEMESTER, 2015-2016**

DURATION: 1 Hour 30 Minutes — **FULL MARKS: 75**

CSE 4305: Computer Organization and Architecture

Programmable calculators are not allowed. Do not write anything on the question paper.

There are **4 (four)** questions. Answer any **3 (three)** of them.

Figures in the right margin indicate marks.

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1. a) Define throughput and response time. Why is it difficult to define performance? 4+4

   b) Consider three different processors *P1*, *P2* and *P3* executing the same instruction set with the clock rates and CPIs given in the following table: 8

Table 1

Processor	Clock Rate	CPI
P1	2 GHz	1.5
P2	1.5 GHz	1.0
P3	3 GHz	2.5

Answer the following questions:

i. Which processor has the highest performance?

ii. If each processor execute a program in 10 seconds, find the number of cycles and the number of instructions.

c) Consider the following sequence of MIPS instructions: 4+5

```
add $8, $4, $1
lw $2, 8($5)
sll $2, $2, 4
andi $5, $5, 12
sw $5, 0($6)
```

Answer the following questions:

i. Determine and describe the data hazard(s) in the instruction sequence.

ii. Reorder the instructions into a new schedule so that it will execute without any stalls on a 5-stage pipelined processor with forwarding.

2. a) Briefly describe the five fields of R-type instructions in MIPS. 5

   b) Describe the following with the help of appropriate examples: 10

i. Pseudodirect addressing

ii. Pseudoinstructions

c) Assume that the variables *f*, *g*, *h*, *i*, and *j* are assigned to registers $s0, $s1, $s2, $s3, and $s4, respectively. Assume that the base address of the arrays A and B are in registers $s6 and $s7, respectively. Write the MIPS assembly code for the C statements below: 3+7

i.
```
f = -g+h+B[1]
```

ii.
```
f = A[B[g]+1]
```

3. a) Define combinational element and state element. What is a clocking methodology and why is it important? 4+3

b) Consider the MIPS datapath shown in Figure 1. Suppose the following latencies (time needed to do their work) for the logic blocks are given: 9

Table 2

I-Mem	Add	Mux	ALU	Regs	D-Mem	Sign-extend	Shift-left
400ps	100ps	30ps	120ps	200ps	350ps	20ps	0ps

Answer the following questions:

i. What is the clock cycle time if the only type of instruction you need to support are ALU instructions (`add, and,` etc.)?

ii. What is the clock cycle time if you only had to support `lw` instructions?

iii. What is the clock cycle time if you must support `add, beq, lw,` and `sw` instructions?

c) Consider the MIPS datapath and assume that the breakdown of the executed instructions is given as below: 9

Table 3

add	addi	not	beq	lw	sw
30%	15%	5%	20%	20%	10%

Answer the following questions:

i. What is the percentage of the data memory usage?

ii. What is the purpose of the "sign-extend" circuit? What percentage of the time is this circuit needed?

iii. If you can improve the latency of one of the given datapath components by 10%, which component should it be? Explain. What is the speed-up from this improvement? Refer to Table 2 for the latency values.

4. a) Consider the MIPS datapath with the control unit. Fill up the following table with 1, 0 or X (don't care) so that the control lines are appropriately determined for the respective instruction. 10

Table 4: Control Values

Instruction	*RegDst*	*ALUSrc*	*MemtoReg*	*RegWrite*	*MemRead*	*MemWrite*	*Branch*
R-format							
lw							
sw							
beq							

b) Answer the questions considering the following two instructions. 10

```
lw:  10001100010000110000000000010000
beq: 00010000001000110000000000001100
```

i. What are the outputs of the "sign-extended" unit for each of the instructions?

ii. What is the new PC address after the instruction is executed?

c) What are the five steps of a MIPS instruction execution? 5

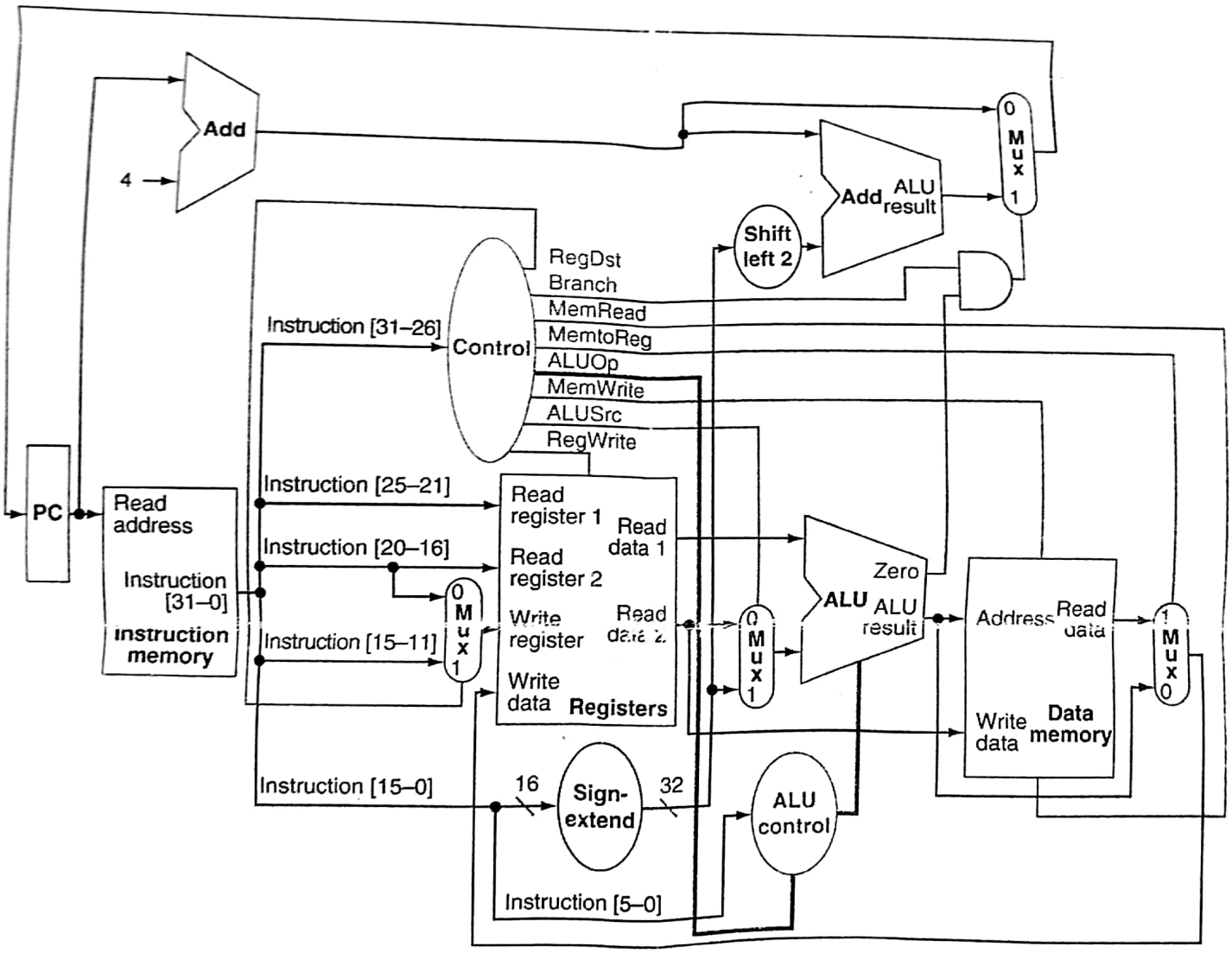

Figure 1: MIPS Datapath along with the Control unit