B.Sc. Engg. (CSE)/ HDCSE, 3rd Sem. Date: 19 March, 2018 (Morning)

# ISLAMIC UNIVERSITY OF TECHNOLOGY (IUT)
# ORGANISATION OF ISLAMIC COOPERATION (OIC)

## DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

Mid-Semester Examination — Winter Semester, A.Y. 2017-2018
Course No.: EEE 4383 — Time: 90 Minutes
Course Title: Electronic Devices and Circuits — Full Marks: 75

There are 4 **(four)** questions. Answer **any 3 (three)** questions. All questions carry equal marks. Marks in the margin indicate full marks. Programmable calculators are not allowed. Do not write on this question paper. Assume suitable value for any missing data.

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1. a) Define intrinsic and extrinsic semiconductors. Draw the detailed transfer characteristics of a pn junction diode composed of Ge, Si and GaAs in the same graph and indicate different regions in the diagram. 07

b) What is transconductance? For a small ac signal as the input, derive the expression for transconductance for a common emitter configuration with circuit diagrams. 06

c) Determine $I$ and $V$ for the circuit in Fig. 1(c) assuming the diodes $D_1$ and $D_2$ are ideal. 06

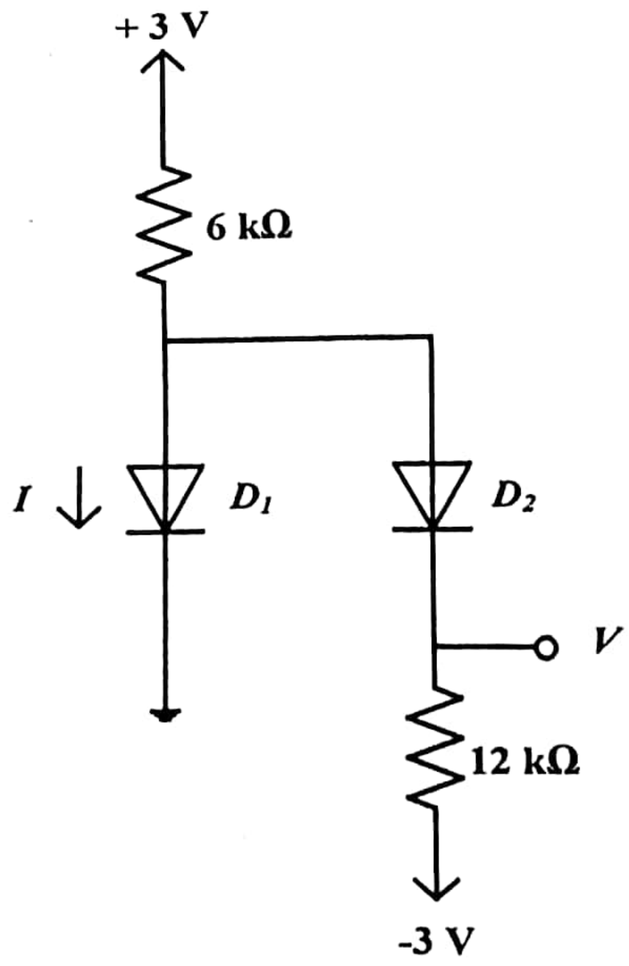


Fig. 1(c)

d) What is the pinch-off voltage for an n-channel JFET? Explain the pinch-off phenomenon with detailed diagram. 06

2. a) Design a full wave rectifier and draw the input and output waveshapes for this circuit. Calculate the Vdc and PIV for this circuit (assume all the diodes are real diodes). 07

b) Draw the majority and minority carrier concentrations profile of an npn transistor in the forward active mode. Explain the different currents generated due to the flow of these carriers and their relations. 06

Explain the avalanche and zener breakdown of a pn junction diode with detailed diagram. What is the difference between them? 06

d) Derive the expressions for the amplifier gain of an npn transistor in active mode for a common emitter configuration. What will be condition for obtaining maximum gain?

3. a) In the circuit of Fig. 3(a), If $\beta = 50$, find $I_E$, $I_B$, $V_E$, $I_C$ and $V_C$. 07

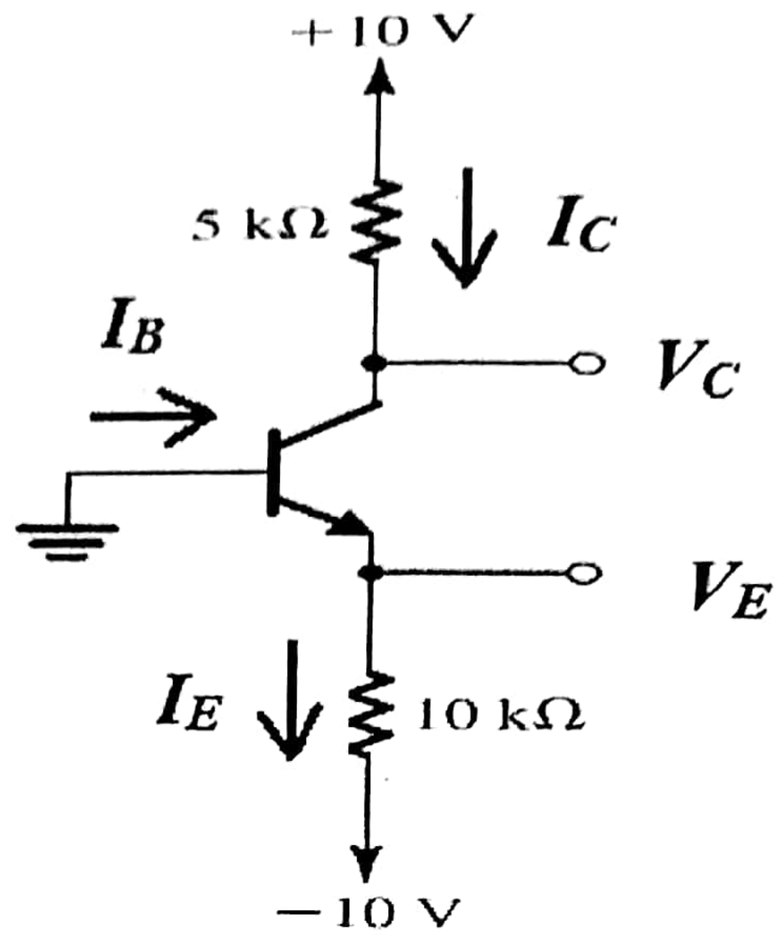


Fig. 3(a)

b) Draw the hybrid pie and T equivalent circuit diagrams for a pnp transistor for a small input signal. 06

c) Define the static and dynamic resistance of a diode. Design a DC battery charger circuit and draw the input and output waveshapes for $V_{dc} = 12$ V and the supply is a 24 V (peak) sinusoid. 06

d) What is a Darlington pair? With detailed diagram, explain the advantages and disadvantages of this arrangement over an npn transistor. 06

4. a) For the circuit in Fig. 4(a), calculate the values of $I_E$, $I_B$, $V_E$, $V_B$, $I_C$ and $V_C$. 07

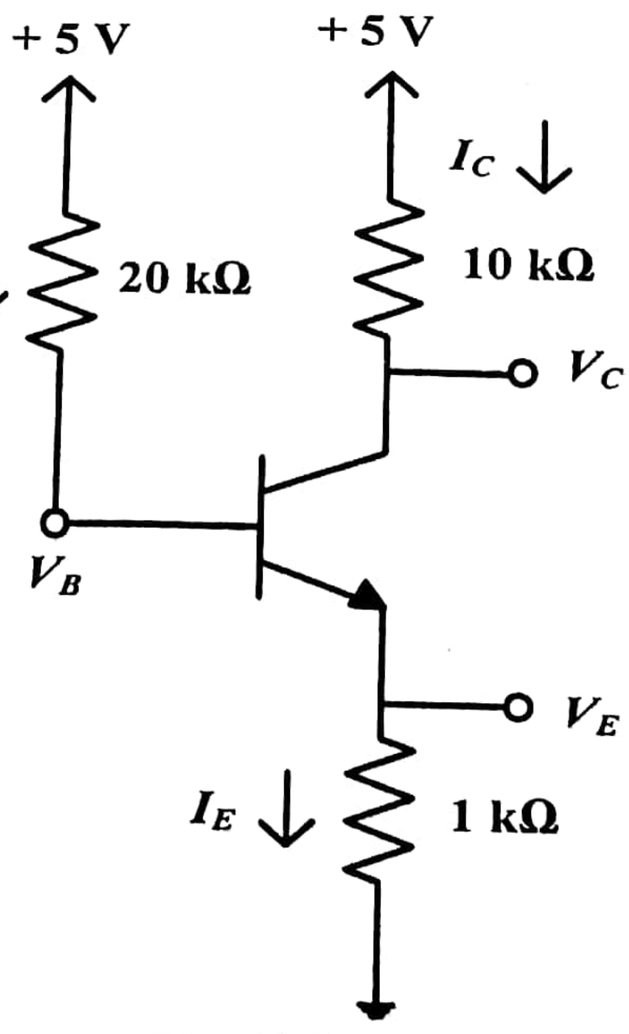


Fig. 4(a)

b) Explain the overdrive factor in the light of the transfer characteristics in Fig. 4(b). Design a simplified equivalent circuit for an npn transistor acting in the saturation mode. 06

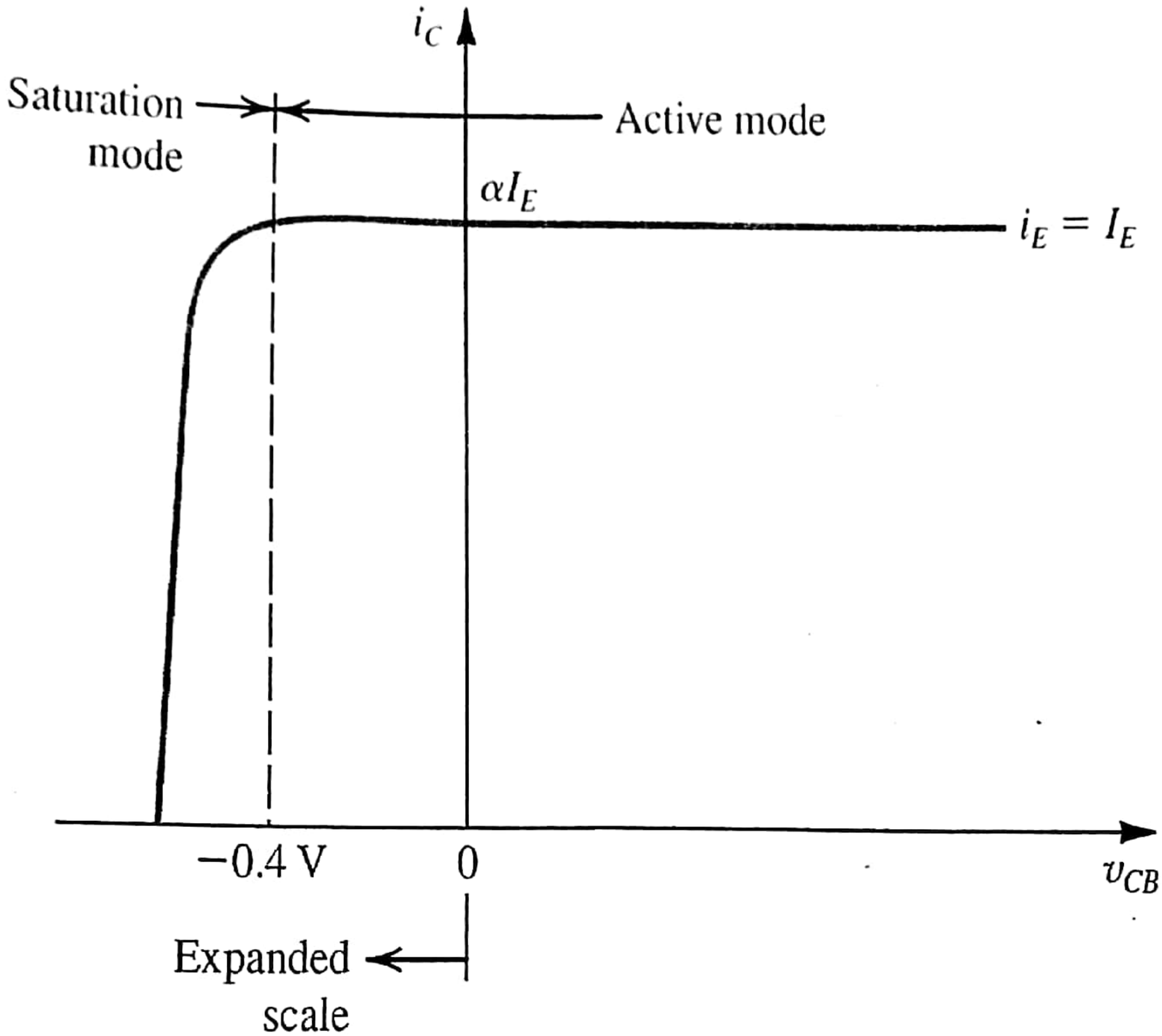


Fig. 4(b)

c) Explain the process of amplification of a small sinusoidal signal for an npn transistor in the active region for a common emitter configuration with appropriate diagrams. 06

d) Using the short hand method, sketch the transfer curve defined by $I_{DSS}$ = 12 mA and $V_P$ = -6 V for a JFET. What type of JFET is this? 06