ISLAMIC UNIVERSITY OF TECHNOLOGY (IUT)
ORGANISATION OF ISLAMIC COOPERATION (OIC)
Department of Computer Science and Engineering (CSE)

MID SEMESTER EXAMINATION **WINTER SEMESTER, 2012-2013**

DURATION: 1 Hour 30 Minutes **FULL MARKS: 75**

CSE 4305: Computer Organization and Architecture

Programmable calculators are not allowed. Do not write anything on the question paper.

There are **4 (four)** questions. Answer any **3 (three)** of them.

Figures in the right margin indicate marks.

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1. a) How is it possible that a processor advertised as having 900-MHz clock rate does not necessarily provide better performance than a processor with 700-MHz clock rate? (Provided that for a source program P1, the compiler generates the same number of actual machine instructions N for both processors). 7

   b) Based on the discussion in Question 1.a), define basic step S and discuss its association with clock cycle. 4

   c) Assume that, the average number of basic steps per instruction is 5 and in an object program P2 there are 100 (N value) machine instructions. If pipelining is used to overlap the execution of instructions, what will be the speed up with respect to a system that does not incorporate pipelining? Provide a pictorial depiction of the pipelining process. 7+4

   d) In a multicomputer system, what is achieved through message passing? 3

2. a) Among the two different approaches to improve the clock rate which one actually reduces the execution time? What is the reason for the other approach not reducing the effective execution time? 2+4

   b) With the help of a diagram that shows the connection between the processor and the memory, describe the steps needed to execute the following instructions: 14

   ADD 20(R0), R1
   MOVE R1, RESULT

   The state of the main memory is provided in the table 1 below. The contents of register R0 and R1 are 560 and 5 respectively. Your discussion should include the state and content of the different processor registers and the main memory at each step of the execution of these instructions.

   Table 1: Main Memory

Label	Address	Content
	0	
	. .	
	500	ADD 20(R0), R1
	504	MOVE R1, RESULT
	. .	
	560	10
	. .	
	580	25
	. .	
RESULT	604	

   c) What is the difference in execution speed between indirect addressing through a register and a memory? 5

3. a) Write a program to evaluate the expression $(A \times B) + (C \times D) + E$ in a stack processor that uses zero-address instructions. Assume that the processor has Load, Store, Multiply and Add instruction. Do not forget to provide the corresponding Register Transfer Notation (RTN) for each instruction in the program. 8

   b) Draw the schematic diagram for the derivation of condition codes and explain how condition codes are affected during program execution. 8+4

   c) What advantage is offered by memory-mapped I/O? Write down the machine instruction sequence to read data from input device. 5

4. a) Suppose a program calls a subroutine which takes four parameters and uses three local variables to perform its task. The subroutine also needs to use registers R0 and R1which were previously used by the calling program. So, they should be saved by the subroutine before using it. Keeping this scenario in mind, discuss how stack pointer and frame pointer can be used for calling the subroutine and returning from the subroutine after execution. 12

   b) With an example explain how branch instruction works using relative addressing mode. 8

   c) What information the assembler needs to have in order to assemble the source program into an object program? How can this information be provided to the assembler? 5