B.Sc. Engg./HD CSE 3rd Semester — 20 March 2018 (Morning)

ISLAMIC UNIVERSITY OF TECHNOLOGY (IUT)
ORGANISATION OF ISLAMIC COOPERATION (OIC)
Department of Computer Science and Engineering (CSE)

MID SEMESTER EXAMINATION — **WINTER SEMESTER, 2017-2018**

DURATION: 1 Hour 30 Minutes — **FULL MARKS: 75**

CSE 4305: Computer Organization and Architecture

Programmable calculators are not allowed. Do not write anything on the question paper.

There are **4 (four)** questions. Answer any **3 (three)** of them.

Figures in the right margin indicate marks.

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1. a) What is interrupt? Explain the difference between computer architecture and computer organization. 1+4

   b) Draw the connection between processor and memory. List the steps needed to execute the machine instruction below in terms of transfer between the components drawn in your figure. 4+6

   ```
   Add     LOCA, R0
   ```

   c) What do you understand by RISC and CISC instruction set? Suppose complete execution of a high level program requires 100 machine language instructions. The average number of basic steps needed per instruction is 13.5. CPU clock cycle time is 5ns. Calculate the execution time of the program. 5+5

2. a) Evaluate the following expression into two address instruction format. 3

   ```
   ((a+b) * (a+c)) /b
   ```

   b) Register R1 and R2 of a computer contain the decimal values 1200 and 4600. What is the effective address of the memory operand in each of the following instructions? 7

   ```
   Move 20(R1), R3
   Load #3000, R3
   Store R3, 30(R1,R2)
   Add -(R2), R3
   Subtract (R1)+, R3
   ```

   c) Convert the expression given at question 2(a) into the format suitable for stack operation and explain the steps involved in executing the expression with diagram. 3+4

   d) Perform the following operation on the given binary string 10001011 by 2 bits. 8
      i. Rotate left with carry
      ii. Rotate right with carry
      iii. Arithmetic right shift
      iv. Logical shift right

3. a) Assume A processor has a direct mapped cache. Data words are 8 bits long (i.e. 1 byte). Data addresses are to the word. A physical address is 20 bits long. The tag is 11 bits. Each block holds 16 bytes of data. How many blocks are in this cache? What is the required size for tag directory? 8

   b) Why static RAM is faster than dynamic RAM? Briefly explain with proper diagram 5

   c) Consider a 16-way set-associative cache. Data words are 64 bits long. Data addresses are to the word. The cache holds 2 Mbytes of data. Each block holds 16 data words. Physical addresses are 64 bits long. 8+4
      i. How many bits of tag, index, and offset are needed to support references to this cache?
      ii. Suppose propagation delay of a comparator is 20k ns where k is the number of comparator. Propagation delay of OR gate is 10ns. Calculate the cache hit latency.

4. a) What do you mean by conflict miss and capacity miss? Explain with example.
   b) Briefly describe the system bus structure with example. 9
   c) Consider a hypothetical 32-bit microprocessor having 32-bit instructions composed of two fields: the first byte contains the opcode and the remainder the immediate operand or an operand address. 6
      i. What is the maximum directly addressable memory capacity
      ii. How many bits are needed for the program counter and the instruction register
   d) What is the condition of overflow in case of two's complement? If a memory system consists of a single external cache with an access time of 20 ns and a hit rate of 0.92, and a main memory with an access time of 60 ns, what is the effective memory access time of this system? 2+3