ISLAMIC UNIVERSITY OF TECHNOLOGY (IUT)
ORGANISATION OF ISLAMIC COOPERATION (OIC)
Department of Computer Science and Engineering (CSE)

SEMESTER FINAL EXAMINATION **WINTER SEMESTER, 2017-2018**

DURATION: 3 Hours **FULL MARKS: 150**

CSE 4305: Computer Organization and Architecture

Programmable calculators are not allowed. Do not write anything on the question paper.

There are 8 (eight) questions. Answer any 6 (six) of them.

Figures in the right margin indicate marks.

1. a) Explain the advantages and disadvantages of using a direct mapped cache instead of an 8-way set associative cache. 5

   b) A computer system uses 16-bit memory addresses. It has a 2K-byte cache organized in a direct-mapped manner with 64 bytes per cache block. Assume that the size of each memory word is 1 byte. 6+4

   i. Calculate the number of bits in each of the tag, index, and offset fields of the memory address.

   ii. Below is a sequence of two binary memory addresses in the order they are used to reference memory. Assume that the cache is initially empty. For each reference, write down the tag and index bits and indicate whether that reference is a hit or a miss

   `0000 0000 1000 0000, 0000 0000 1001 0000`

   c) Repeat question 1(b), if the cache is organized as a 2-way set-associative cache that uses the LRU replacement algorithm. 6+4

2. a) Define Horizontal and vertical organization of micro instruction. Why is the WMFC step needed when reading from or writing to the main memory? 4+4

   b) Suppose a processor is using the single bus structure for internal datapath. Write the sequence of control steps required for each of the following instructions. 4+4

   i. *Add (R3), R1*
   ii. *Add R3, R1*

   c) Briefly describe hardwired control and microprogrammed control with proper diagram. 9

3. a) What do you mean by memory interleaving? How can the memory interleaving increase higher average utilization of memory? 7

   b) What is the advantage of using a write-back cache instead of a write-through cache? You find that it would be very inexpensive to implement small, direct mapped cache of 32K bytes with an access time of 30 ns. However, the hit rate would be only about 50%. If the main memory access time is 60 ns, does it make sense to implement the cache? 5+4

   c) The average memory access time for a microprocessor with 1 level of cache is 2.4 clock cycles 9

   If data is present and valid in the cache, it can be found in 1 clock cycle. If data is not found in the cache, 80 clock cycles are needed to get it from off-chip memory. Designers are trying to improve the average memory access time to obtain a 65% improvement in average memory access time, and are considering adding a 2nd level of cache on-chip. This second level of cache could be accessed in 6 clock cycles. The addition of this cache does not affect the first level cache's access patterns or hit times. Off-chip accesses would still require 80 additional CCs. To obtain the desired speedup, how often must data be found in the 2nd level cache?

4. a) What is virtual memory? Explain the concept of virtual memory address translation scheme with paging using necessary diagrams.
   b) What is TLB? Explain (in 4-5 sentences) why TLB is needed for virtual-to-physical address translation.
   c) Explain TLB hit and TLB miss with proper example and diagram. 10

5. a) Briefly explain the difference between page fault and TLB miss with proper example. 7
   b) What do you mean by RAID? List the characteristics of each RAID level with diagram. 8
   c) Write short note on read and write mechanism of magnetic disk. 7
   d) Consider a machine with 64-bit addresses and an 8KB page size. How many bits are required to represent a page number? 3

6. a) Consider the following sequence of instructions being processed on the pipelined 5-stage RISC processor 6x3

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Load R4, #100(R2)
Add R5, R2, R3
Subtract R6, R4, R5
And R7, R2, R5
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   i. Identify all the data dependencies in the above instruction sequence. For each dependency, indicate the two instructions and the register that causes the dependency.
   ii. Assume that the pipeline does not use operand forwarding. Also assume that the only sources of pipeline stalls are the data hazards. Draw a diagram that represents instruction flow through the pipeline during each clock cycle. How long does it take for the instruction sequence to complete?
   iii. Now, assume that the pipeline uses operand forwarding. There are separate forwarding paths from the outputs of stage-3 and stage-4 to the input of stage-3. Draw a diagram that represents the flow of instructions through the pipeline during each clock cycle. Indicate operand forwarding by arrows.

   b) What is dynamic branch prediction? Draw the finite state machine for a 2-bit prediction scheme. 2+5

7. a) "Pipelining does not result in individual instructions being executed faster; rather, it is the throughput that increases" Explain this with necessary example. 7
   b) Why shouldn't we use a million pipeline stages if an operation can be divided up into a million steps, even if we can keep the pipeline full? 5
   c) Briefly describe the different functional units of basic linear pipeline architecture. 6
   d) Consider the execution of a program of 15000 instructions by a linear pipeline processor with a clock rate of 25MHz. Assume that the instruction pipeline has 5 stages and that one instruction is issued per clock cycle. The penalties due to branch instructions and out-of-sequence executions are ignored 3+4
      i. Calculate the speedup factor as compared with non-pipelined processor
      ii. What are the efficiency and throughput of this pipelined processor

8. a) What do you mean by Direct Memory Access? Briefly explain how DMA controller can transfer a block of data from an external device to the processor? 2+6
   b) Write short notes on the following. 3x3
      i. Cycle Stealing
      ii. Memory-mapped I/O
      iii. Interrupt-service routine
   c) One way of receiving a response from a device is to poll it periodically about whether it has any additional information. What is wrong with this technique? Explain the alternative. 2+6