ISLAMIC UNIVERSITY OF TECHNOLOGY (IUT)
ORGANISATION OF ISLAMIC COOPERATION (OIC)

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

Semester Final Examination Winter Semester, A.Y. 2015-2016
Course No.: EEE 4335 Time: 3 Hours
Course Title: Digital Logic Design Full Marks: 150

There are 8 (eight) questions. Answer any 6 (six) questions. All questions carry equal marks. Marks in the margin indicate full marks. Programmable calculators are not allowed. Do not write on this question paper.

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1. a) Implement the following function with a multiplexer: 10
$F(A, B, C, D) = \sum (0, 1, 3, 4, 8, 9, 12, 13, 15)$

   b) What is a priority encoder? Design a 4-bit priority encoder with Boolean expressions and necessary logic diagrams. 15

2. a) Design a combinational circuit using a ROM which accepts 3-bit binary number as input and shows the square of the input number as output in binary. The size of the ROM used should be of minimum dimension. 15

   b) What are the functions of sequential circuit in digital electronics? 05

   c) Explain the mechanism of a basic RS latch with NAND gates. What is the significance of having set and reset? 05

3. a) Describe the mechanism of edge triggering (both positive and negative) for a D-type flip-flop with appropriate logic diagrams. 15

   b) Draw the timing diagram and logic diagram with truth table for a negative edge triggered JK flip-flop. 10

4. a) From the sequential circuit with D flip-flops in Fig 4(a), solve for the flip-flop outputs A, B and the system output Z, draw the state diagram and state table for all the possible combinations of input X. 15

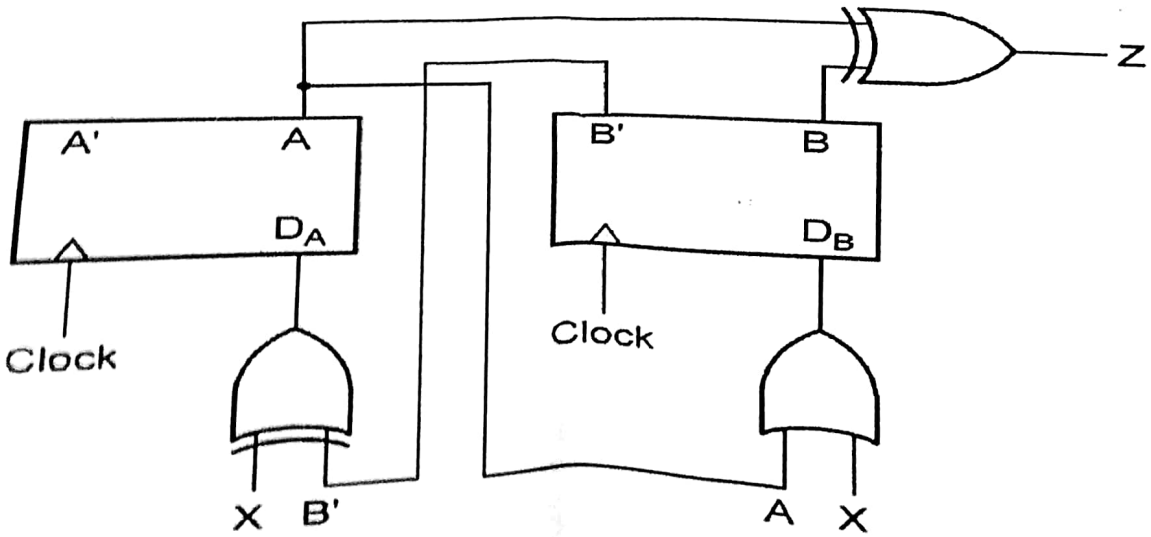

Fig. 4(a)

b) Define registers and counters. 05

c) Design a 4-bit register with parallel load using D flip-flops. 05

5. a) Design a bidirectional shift register with parallel load and clear control having two selection pins S_1 and S_0 which will perform the operations according to the table in Table 5(a). 15

Mode control		Register Operation
S_1	S_0	
0	0	Shift right
0	1	Shift left
1	0	No change
1	1	Parallel load

Table 5(a)

b) Design and explain the mechanism of a 4-bit binary ripple counter. 10

6. a) Construct an 8 × 4 RAM and briefly explain its mode of operations. 20

b) Draw the diagram of a 4-bit binary up-down counter. 05

7. a) Design a 4-bit BCD adder from 4-bit binary adders with truth table and Boolean expression solutions. 10

b) Construct a Full-subtractor circuit with truth table and then re-construct the circuit using only NAND gates. 15

8. a) Solve the following function using the MAP method: 10
$F(w, x, y, z) = \sum (1, 2, 4, 5, 7, 8, 10, 11, 13, 14)$

b) Prove, $x + 1 = x$ using basic postulates of Boolean algebra. 05

c) Given that, $A = 2176_8$ and $B = 2436_8$. Find out A-B using 2's complement. 05

d) Discuss about the application of error detection codes in digital electronics. 05