Presentation Report:

Intel VS AMD

COMP 3318 Operating Systems
North American University
Stafford, Texas 2016
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Differences between 32bit & 64 bit processors
What is a Processor?

https://www.youtube.com/watch?v=-P28LKWTzrI

Processor is the brain computer. It performs much calculation behind the scenes, ultimately allowing you to complete tasks as trivial as composing an e-mail to tasks as intensive as data analysis and modeling.
From a practical standpoint, the true difference at hand is the ability to run a 32-bit operation system (OS) versus a 64-bit OS and their subsequent applications. Technically, 64-bit allows the processor to address larger chunks of data from physical memory (RAM) than their 32- bit counterparts.

AMD vs. INTEL

	AMD FX-8150	Intel i7 2600
Microarchitecture	**Bulldozer**	**Sandy Bridge**
Cores	8 cores 4 modules	4 cores
L1 cache	256 KB(I) 128 KB(D) 64KB per module(I) 16KB per core(D)	4*32 KB(I) 4*32 KB(D) 4-way associative for instructions 8-way associative for data
L2 cache	4*2 MB Each 2MB is shared between 2 cores in one module	4*256 KB Each 256KB is private to each core
L3 cache	8 MB all core shared 64-way associative	8MB all core shared
Replacement scheme	pseudo-LRU	L1 pseudo-LRU L2 pseudo-LRU L4 pseudo-LRU but with an ordered selection algorithm
Latency	4 (L1 cache load)	4 (L1 cache) 11(L2 cache)
Max memory bandwidth	21 GB/s	21 GB/s
Memory channel support	now known	3 memory channels Each channel consists of a separate set of DIMMs
Virtual & physical memory addresses	48-bit virtual and physical addresses	48-bit virtual addresses and 36-bit physical addresses
TLB feature	2 levels TLB	2 levels TLB
How caches are indexed	not known	L1: virtually indexed and physically tagged L2: physically indexed

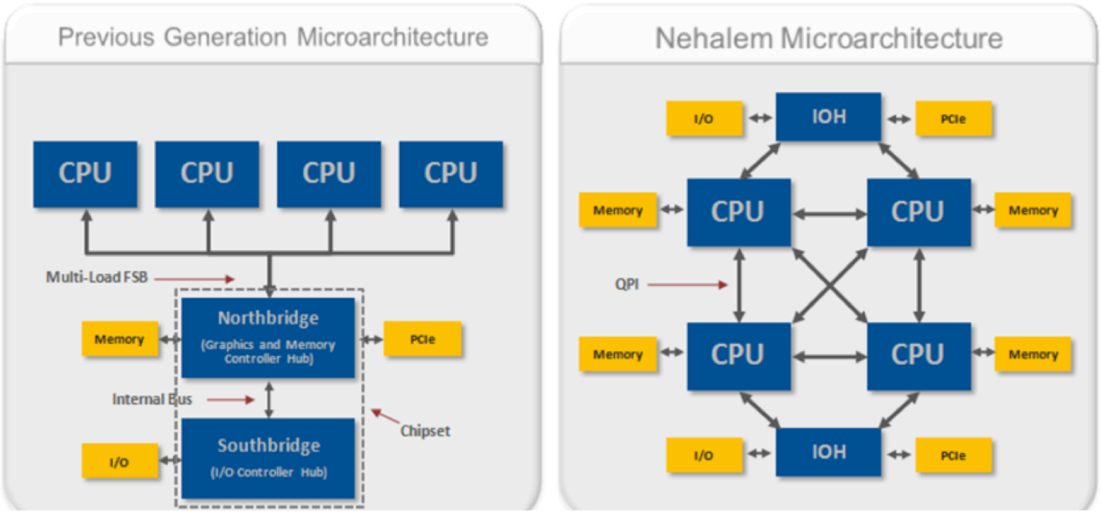
From the table we can conclude that both AMD and Intel have similar memory design. Both of them use LRU policy, which can take advantage of time locality. Both AMD and INTEL have the multiple levels of caches. This design can help the processor to quickly get the data and avoid more cache misses.

Cache memory

Cache memory is also often called CPU memory and it is usually physically located on the CPU.

Not only was the memory controller moved to the CPU for Nehalem processors, Intel also introduced a distributed shared memory architecture using Intel QuickPath Interconnect (QPI). QPI is the new point-to-point interconnect for connecting a CPU to either a chipset or another CPU. It provides up to 25.6 GB/s of total bidirectional data throughput per link.

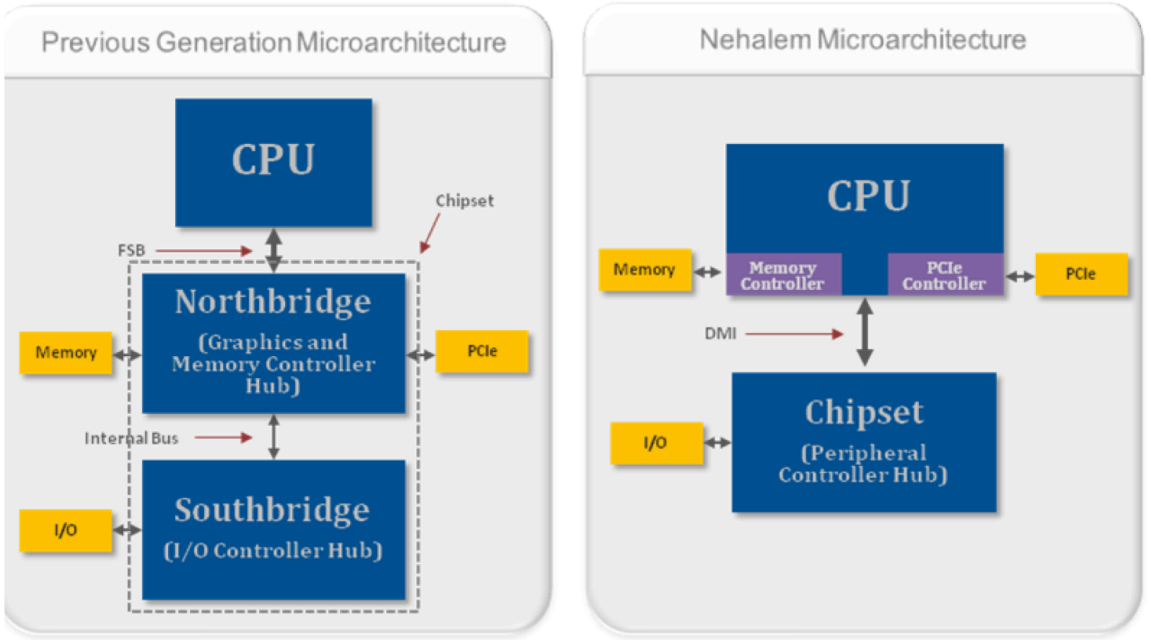
Intel's decision to move the memory controller in the CPU and introduce the new QPI databus has had an impact for single-processor systems. However, this impact is much more significant for multiprocessor systems. Figure 2 illustrates the typical block diagrams of multiprocessor systems based on the previous generation and the Nehalem microarchitecture.



The data that is stored in cache memory in cache is usually the data and commands most often used by CPU. It is very fast way to serve the data to the processor, but the size of the memory cache is limited.
Most modern CPUs have three different types of the cache memory. The first, called L1 cache is the quickest and it is the first place that a CPU will look when it needs data. However, it is also the smallest of the three types of cache memory. The second type of the cache – and the second place that a CPU looks for data –is called L2 cache. It is slightly slower than L1 cache, but it is slightly bigger so it holds more information.
The final type of cache memory is called L3 cache. It is the third place that CPU uses before it goes to the computer's main memory. L3 cache is the biggest cache and, despite being slowest of the three, is till quicker than main memory.

Optimization of Cache Performance

To optimize cache performance , there are 10 common techniques that are applied to cache design. The goal is to reduce hit time , increase cache bandwidth, reduce the miss penalty , reduce miss rate and reduce miss penalty or miss rate through parallelism.



Both use small and simple first-level caches to reduce hit time and power. For i7,L3 is 8MB large and use 16-way associativity while L1 is only 32 KB and 4-way or 8-way associativity.

Pipeline Cache access to increase cache bandwidth

This technique pipeline cache access so that first-level cache hit latency can be

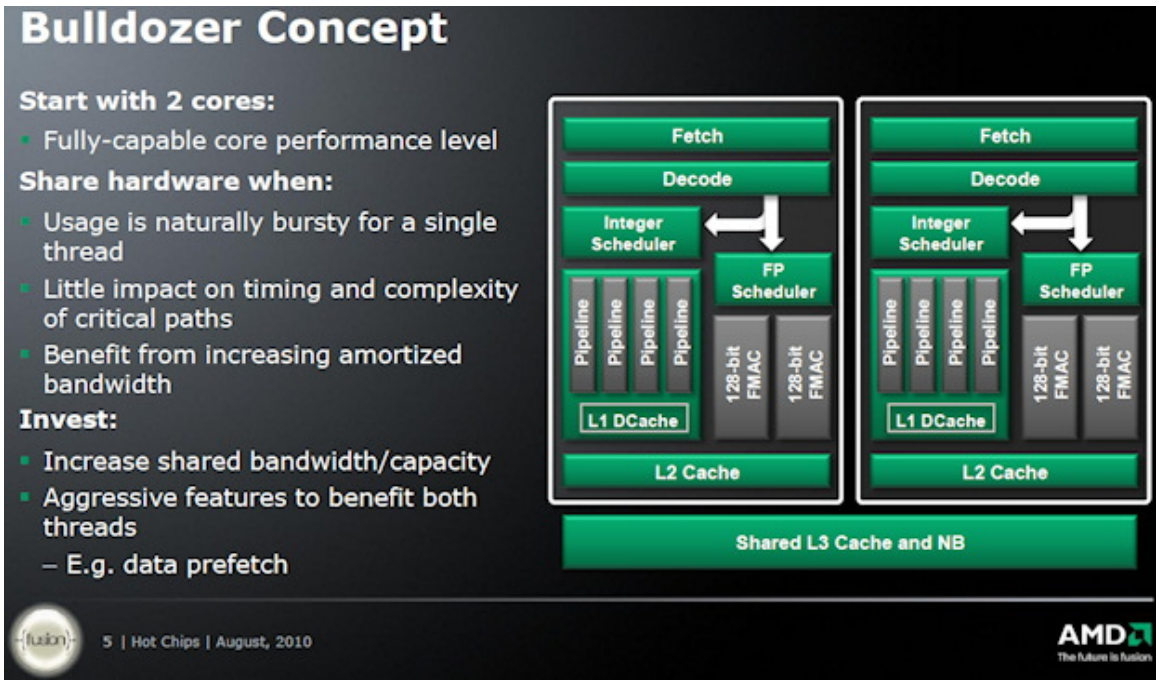
multiple cycles. In this way, clock cycle time is shorter and bandwidth is higher, but hits are slower. In the current Intel Core i7 pipeline takes 4 clocks for cache access. AMD also has the load-store pipeline.

Branch Prediction

Intel Core i7 use two-lower prediction. The first level is small enough to predict a branch every clock cycle, and the second level is larger to serve backup. Each predictor combines:

1) Two-bit predictor
2) Global history predictor
3) A loop exit predictor

The best predictor is selected based on the accuracy of each predictor.
AMD bulldozer has a new branch prediction design.



The scheme is a hybrid method with a local predictor and a global predictor. The branch target buffer (BTB) has two levels:

1) The level -1 is organized as a set-associative cache with 128 4-way sets
2) The level-2 has 1024 5-way sets

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