

I2C Encoder V2

HW v2.0

Revision History

Revision	Date	Author(s)	Description
1.0	24.06.18	Simone	First draft version

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1. Device Overview

The I2C Encoder V2 is a small board where you can use a classical mechanical encoder, or an illuminated RGB encoder with a I²C bus. The device has also 3 configurable GPIOs with the same footprint of an RGB LED. It's possible to connect up to 127 boards in cascade and read all of them with the same I²C bus.

The I2C Encoder V2 has a series of 8 bit registers where it is possible to configure the parameters and four 32 bit of registers. These 32 bit registers are very important because they store counter value, value of increment steps, maximum and minimum thresholds. Every time when the encoder is moved at least one step, the counter value is increased of the increment step value or decreased according to the rotation direction. When the counter value is outside of the limit set by the threshold, the counter value can be wrapped or can stuck on the threshold valued reached.

The I2C Encoder V2 also has an open-drain interrupt pin. It is set to logic low every time when the encoder is rotated or pushed. The status register must be read by the master to check what is changed.

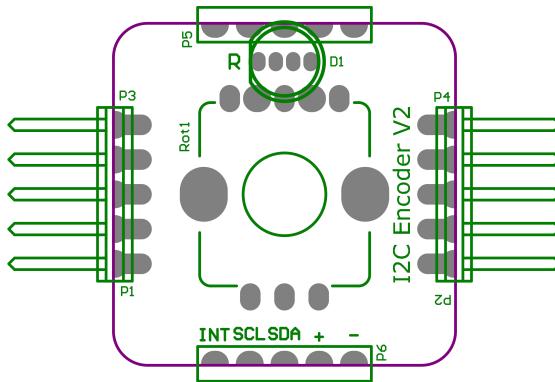


Figure 1.1: Top view of the board

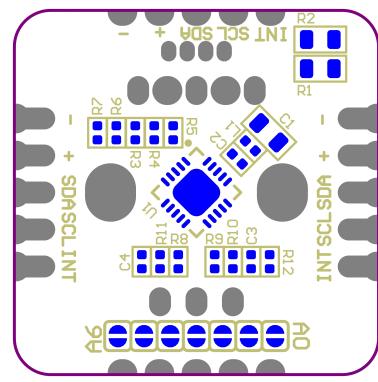


Figure 1.2: Bottom view of the board

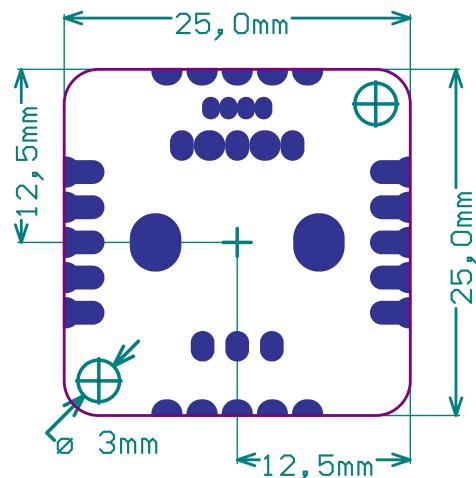


Figure 1.3: Dimensions of the board

1.1 Electrical characteristics

Parameter	Symbol	Min	Max
Supply voltage	V_{DD}	3V	5V
I ² C input-low level	V_{IL}	0	$0.3 * V_{DD}$
I ² C input-high level	V_{IH}	$0.8 * V_{DD}$	V_{DD}
I ² C clock input frequency	f_{SCL}		400kHz
Supply current (LEDs off)	I_{DD}		1.8mA
Interrupt pull-up resistor	R_{INT}	$15k\Omega$	$120k\Omega$

1.2 Connection

Figure 1.4 shows the pin out of the I2C Encoder V2.

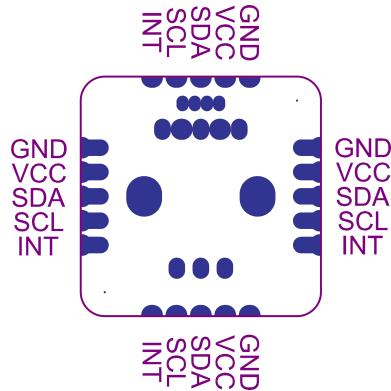


Figure 1.4: Pin-out of the board

Pin	I/O Type	Function
GND	Power	Ground reference for logic
Vcc	Power	Positive supply for logic
SDA	I/O	I ² C data
SCL	I	I ² C clock
INT	OD	Open-drain interrupt output

There are two 5 pin headers one the right and one at the left side of the I2C Encoder V2. And 5 castellated hole on each side. The I2C Encoder V2 can be connected in cascade by soldering the castellated hole as showed in figure 1.5. Since the INT pin is open drain, the signal is propagated along the chain in case of interrupt of one device. In order to avoid I²C address conflict, the address of each device must be different. In the section 1.3, it is described how to set the address.



Figure 1.5: Example of 4 boards connected in cascade

1.3 I²C interface

The I²C Encoder V2 is a I²C slave, it's possible to set 127 different addresses. All of the 7-bit address can be customized by soldering the jumpers A0 - A6 on the bottom of the board. When the jumper is open, it means a logic 0. If a jumper is shorted, it means a logic 1.

I ² C address							
7	6	5	4	3	2	1	0
A6	A5	A4	A3	A2	A1	A0	R/W

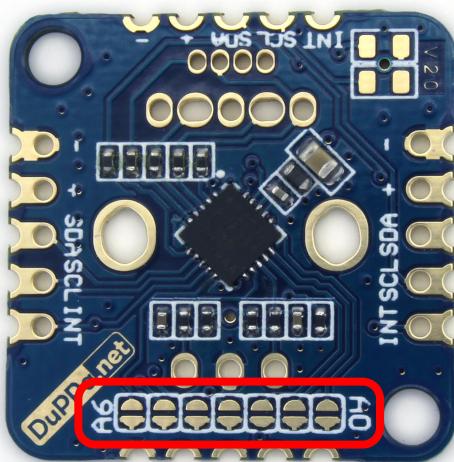


Figure 1.6: Jumpers location

The I²C Encoder V2 has I²C pull-up resistors. They can be enabled by soldering the two resistor **R1** and **R2** like in the figure 1.6. This must be done in case that the master doesn't have these resistors and must be enabled only one I²C Encoder V2 in a chain.

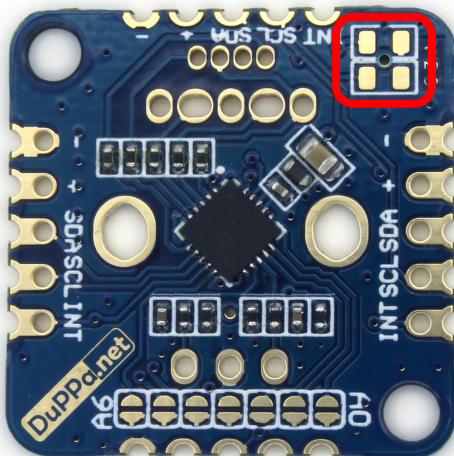


Figure 1.7: Pull-up resistor location

1.4 GP pins

There are 3 configurable GP pins, they are called GP1, GP2 and GP3. They are placed in the same footprint of an 5mm RGB led. In figure 1.8 is showed the position. Each pin can be configured to be:

- **PWM** The pins are configured to be a PWM output, the resolution is 8bit
- **Analog input**: The pins are configured to be an input of the internal ADC, the resolution is 8
- **GPIO output**: The pins are configured to be a digital output.
- **GPIO Input**: The pin is configured to be a digital input. It is possible to set an interrupt at every signal edge

In case of a RGB encoder is mounted, the GP3 will be not available. This is because the GP3 is internally connected to the red color of the RGB led and is automatically configured to be a PWM.

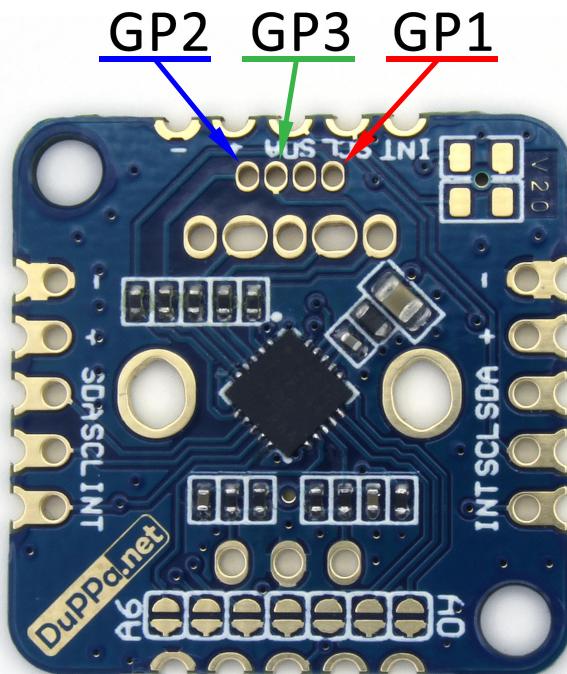


Figure 1.8: GP pins pinout

2. Registers

In this section, the internal registers of I2C Encoder V2 is described.

Address range	Name	Description	Dimension	Default value
0x00	GCONF	General Configuration	1 Byte	0
0x01	GP1CONF	GP 1 Configuration	1 Byte	0
0x02	GP2CONF	GP 2 Configuration	1 Byte	0
0x03	GP3CONF	GP 3 Configuration	1 Byte	0
0x04	INTCONF	INT pin Configuration	1 Byte	0
0x05	ESTATUS	Encoder Status	1 Byte	0
0x06	GPSTATUS	GP Status	1 Byte	0
0x07 - 0x0A	CVAL	Counter Value	4 Byte	0
0x0B - 0x0E	CMAX	Counter Max value	4 Byte	0
0x0F - 0x12	CMIN	Counter Min value	4 Byte	0
0x13 - 0x16	ISTEP	Increment step value	4 Byte	1
0x17	RLED	LED red color intensity	1 Byte	0
0x18	GLED	LED green color intensity	1 Byte	0
0x19	BLED	LED blue color intensity	1 Byte	0
0x1A	GP1REG	I/O GP1 register	1 Byte	0
0x1B	GP2REG	I/O GP2 register	1 Byte	0
0x1C	GP3REG	I/O GP3 register	1 Byte	0
0x80 - 0xFF	EEPROM	EEPROM memory	128 Byte	0

2.1 Configuration

2.1.1 General Configuration

Address: 0x00							
7	6	5	4	3	2	1	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RESET	MBANK	ETYPE	RMOD	IPUD	DIRE	WRAPE	DTYPE

❖ **DTYPE** Data type of the register: Counter Value, Counter Max, Counter Min and Increment step.

- 1: The registers are considered float numbers IEEE 754
- 0: The registers are considered int 32bit

❖ **WRAPE** Enable counter wrap.

- 1: Wrap enable. When the counter value reaches the **CMAX**+1, restart to the **CMIN** and vice versa
- 0: Wrap disable. When the counter value reaches the **CMAX** or **CMIN**, the counter stops to increasing or decreasing

❖ **DIRE** Direction of the encoder when increment.

- 1: Rotate left side to increase the value counter
- 0: Rotate right side to increase the value counter

❖ **IPUD** Interrupt Pull-UP disable.

- 1: Disable
- 0: Enable

❖ **RMOD** Reading Mode.

- 1: X2 mode
- 0: X1 mode

❖ **ETYPE** Set the encoder type

- 1: RGB illuminated encoder
- 0: Standard encoder

❖ **MBANK** Select the EEPROM memory bank. Each bank are 127 byte wide

- 1: Second memory bank
- 0: First memory bank

❖ **RST** Reset of the I2C Encoder V2

- 1: Reset
- 0: No reset

2.1.2 GP1 Configuration

Address: 0x01							
7	6	5	4	3	2	1	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
-	-	-	GP1INT	GP1PUL	GP1MODE		

❖ **GP1MODE** Configuration of the pin GP1

- 00: PWM output
- 01: GPIO output Push-Pull
- 10: Analog input
- 11: GPIO Input

❖ **GP1PUL** Enable or disable the internal pull-up.

- 0: Pull-UP disable
- 1: Pull-UP enabled

❖ **GP1INT** Configuration of the interrupt, available only when the pin is configured as input

- 00: Interrupt disabled
- 01: Interrupt on positive edge
- 10: Interrupt on negative edge
- 11: Interrupt on both edges

2.1.3 GP2 Configuration

Address: 0x02							
7	6	5	4	3	2	1	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
-	-	-	GP2INT	GP2PUL	GP2MODE		

❖ **GP2MODE** Configuration of the pin GP2

- 00: PWM output
- 01: GPIO output Push-Pull
- 10: Analog input
- 11: GPIO Input

❖ **GP2PUL** Enable or disable the internal pull-up.

- 0: Pull-UP disable
- 1: Pull-UP enabled

❖ **GP2INT** Configuration of the interrupt, available only when the pin is configured as input

- 00: Interrupt disabled
- 01: Interrupt on positive edge
- 10: Interrupt on negative edge
- 11: Interrupt on both edges

2.1.4 GP3 Configuration

Address: 0x03							
7	6	5	4	3	2	1	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
-	-	-		GP3INT	GP3PUL	GP3MODE	

Note: When the **ETYPE** bit is set, this pin is in PWM mode automatically and can't be changed.

❖ GP3MODE Configuration of the pin GP3

- 00: PWM output
- 01: GPIO output Push-Pull
- 10: Analog input
- 11: GPIO Input

❖ GP3PUL Enable or disable the internal pull-up.

- 0: Pull-UP disable
- 1: Pull-UP enabled

❖ GP3INT Configuration of the interrupt, available only when the pin is configured as input

- 00: Interrupt disabled
- 01: Interrupt on positive edge
- 10: Interrupt on negative edge
- 11: Interrupt on both edges

2.2 Interrupt output Configuration

This register is used for enable or disable the interrupt source selectively. When an interrupt event occurs, the **INT** pin goes low and the event is stored in the status register.

Address: 0x04							
7	6	5	4	3	2	1	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IGP	-	IRMIN	IRMAX	IRDEC	IRINC	IPUSHP	IPUSHR

❖ **IPUSHR** Push button release bit

- 1: Interrupt enabled when the push button is released.
- 0: Interrupt disabled

❖ **IPUSHP** Push button press bit

- 1: Interrupt enabled when the push button is pressed.
- 0: Interrupt disabled

❖ **IRINC CVAL** increase bit

- 1: Interrupt enabled when the **CVAL** register is increased
- 0: Interrupt disabled

❖ **IRDEC CVAL** decrease bit

- 1: Interrupt enabled when the **CVAL** register is decreased
- 0: Interrupt disabled

❖ **IRMAX CVAL** reaches **CMAX** bit

- 1: Interrupt enabled when **CVAL** reaches **CMAX**
- 0: Interrupt disabled

❖ **IRMIN CVAL** reaches **CMIN** bit

- 1: Interrupt enabled when **CVAL** reaches **CMIN**
- 0: Interrupt disabled

❖ **IGP** GPx pin event bit

- 1: Interrupt enabled when any event occurs on GP1, GP2 or GP3.
- 0: Interrupt disabled

2.3 Status

2.3.1 Encoder Status

Address: 0x05							
7	6	5	4	3	2	1	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
-	-	RMIN	RMAX	RDEC	RINC	PUSHP	PUSHR

PUSHR Status of the push button of the encoder

- 1: Push button is relised
- 0: Push button is not relised

PUSHP Status of the push button of the encoder

- 1: Push button is pressed
- 0: Push button is not pressed

RINC Status of the counter value

- 1: Counter value is increased
- 0: Counter value is not increased

RDEC Status of the counter value

- 1: Counter value is decreased
- 0: Counter value is not decreased

RMAX Status of the counter value

- 1: **CVAL** reaches the **CMAX** value
- 0: **CVAL** is below the **CMAX** value

RMIN Status of the counter value

- 1: **CVAL** reaches the **CMIN** value
- 0: **CVAL** is above the **CMIN** value

2.3.2 GP Status

Address: 0x06							
7	6	5	4	3	2	1	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
-	-	EGP3			EGP2		EGP1

GP1 Configuration of the GP1

- 00: No event occurs
- 01: Positive edge event
- 10: Negative edge event

GP2 Configuration of the GP2.

- 00: No event occurs
- 01: Positive edge event
- 10: Negative edge event

GP3 Configuration of the GP3. Available only with the standard encoder

- 00: No event occurs
- 01: Positive edge event
- 10: Negative edge event

2.4 Encoder registers

2.4.1 Counter Value

Address: 0x07							
31	30	29	28	27	26	25	24
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CVAL BYTE 4 <31 - 24>							
Address: 0x08							
23	22	21	20	19	18	17	16
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CVAL BYTE 3 <23 - 16>							
Address: 0x09							
15	14	13	12	11	10	9	8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CVAL BYTE 2 <15 - 8>							
Address: 0x0A							
7	6	5	4	3	2	1	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CVAL BYTE 1 <7 - 0>							

This is a signed 32 bit register where the counter value is stored. When the encoder is rotated, the value is increased or decreased according to the direction.

2.4.2 Counter Max

Address: 0x0B							
31	30	29	28	27	26	25	24
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CMAX BYTE 4 <31 - 24>							
Address: 0x0C							
23	22	21	20	19	18	17	16
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CMAX BYTE 3 <23 - 16>							
Address: 0x0D							
15	14	13	12	11	10	9	8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CMAX BYTE 2 <15 - 8>							
Address: 0x0E							
7	6	5	4	3	2	1	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CMAX BYTE 1 <7 - 0>							

This is a signed 32 bit register, it is used for storing the maximum threshold of the **CVAL** register. When **CVAL** is greater than **CMAX**, the value of **CVAL** is set according to the flag **WRAPE**.

2.4.3 Counter Min

Address: 0x0F							
31	30	29	28	27	26	25	24
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CMIN BYTE 4 <15 - 8>							
Address: 0x10							
23	22	21	20	19	18	17	16
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CMIN BYTE 3 <7 - 0>							
Address: 0x11							
15	14	13	12	11	10	9	8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CMIN BYTE 2 <15 - 8>							
Address: 0x12							
7	6	5	4	3	2	1	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CMIN BYTE 1 <7 - 0>							

This is a signed 32 bit register, it is used for storing the minimum threshold of the **CVAL** register. When **CVAL** is less than **CMIN**, the value of **CVAL** is set according the the flag **WRAPE**.

2.4.4 Increment step

Address: 0x13							
31	30	29	28	27	26	25	24
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CMIN BYTE 4 <15 - 8>							
Address: 0x14							
23	22	21	20	19	18	17	16
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CMIN BYTE 3 <7 - 0>							
Address: 0x15							
15	14	13	12	11	10	9	8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CMIN BYTE 2 <15 - 8>							
Address: 0x16							
7	6	5	4	3	2	1	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CMIN BYTE 1 <7 - 0>							

This is a 32 bit register, it is used for set the increment step. When the encoder is moved of one step the continents of this register is summed or subtracted to the **CVAL**.

2.5 LEDs registers

2.5.1 LED Red intensity

Address: 0x17							
7	6	5	4	3	2	1	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
LED A PWM Value <7 - 0>							

This register is used for setting the PWM of the **LED R** of the RGB LED. A value of **0x00** means PWM at 0%, LED OFF. A value of **0xFF** means PWM at 100%, LED completly ON.

2.5.2 LED Green intensity

Address: 0x18							
7	6	5	4	3	2	1	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
LED B PWM Value <7 - 0>							

This register is used for setting the PWM of the **LED G** of the RGB LED. A value of **0x00** means PWM at 0%, LED OFF. A value of **0xFF** means PWM at 100%, LED completly ON.

2.5.3 LED Blue intensity

Address: 0x19							
7	6	5	4	3	2	1	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
LED B PWM Value <7 - 0>							

This register is used for setting the PWM of the **LED B** of the RGB LED. A value of **0x00** means PWM at 0%, LED OFF. A value of **0xFF** means PWM at 100%, LED completly ON.

2.6 GPs registers

The usage of these register depends of the configuration of the GP pins:

- **PWM** The register is not used
- **GPIO output:** Is possible to write 1 or 0 for setting the output logic level.
- **Analog input:** Is possible to read the ADC value
- **GPIO Input:** Is possible to read the logic level of the output

2.6.1 GP1 register

Address: 0x1A							
7	6	5	4	3	2	1	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
GP1 Value <7 - 0>							

2.6.2 GP2 register

Address: 0x1B							
7	6	5	4	3	2	1	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
GP2 Value <7 - 0>							

2.6.3 GP3 register

Address: 0x1C							
7	6	5	4	3	2	1	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
GP3 Value <7 - 0>							

3. Schematic

