1.

a)

$$16 * 8/64 = 2$$

So 2 integers can be stored.

b)

A[i][j] repeatedly referenced exhibit temporal locality.

c)

i and j exhibit spatial locality.

2.

a)

References	Binary word Address	Tag	Index	Offset	Hit/Miss
0x03	00000011	0	0	3	Miss
0xB4	10110100	1	6	4	Miss
0x2B	00101011	0	5	3	Miss
0x02	00000010	0	0	2	Hit
0xBF	10111111	1	7	7	Miss
0x58	01011000	0	11	0	Miss
0xBE	10111110	1	7	6	Hit
0x0E	00001110	0	1	6	Miss
0xB5	10110101	1	6	5	Hit
0X2C	00101100	0	5	4	Hit
0xBA	10111010	1	7	2	Hit
0xFD	11111101	1	15	5	Miss

b)

References	Binary word Address	Tag	Index	Offset	Hit/Miss
0x03	00000011	0	0	3	Miss
0xB4	10110100	1	3	4	Miss
0x2B	00101011	0	2	11	Miss
0x02	00000010	0	0	2	Hit
0xBF	10111111	1	3	15	Hit
0x58	01011000	0	5	8	Miss
0xBE	10111110	1	3	14	Hit
0x0E	00001110	0	0	14	Hit
0xB5	10110101	1	3	5	Hit
0X2C	00101100	0	2	12	Hit
0xBA	10111010	1	3	10	Hit
0xFD	11111101	1	7	13	Miss

c)

C-2 Provides the best performance. C-1 have lots of compulsory misses and C-3 have lots of conflict misses.

3.

a)

The storage array's controller organizes its cache into "blocks," which are chunks of memory that can be 4, 8, 16, or 32 KiBs in size. All volumes on the storage system share the same cache space; therefore, the volumes can have only one cache block size.

b)

The cache have 32 blocks.

c)

The ratio between these two are about 8.

d)

Address	Index	Offset	Hit/Miss	Replace	Final Value
0x00	00000	00000	Miss	No	No
0x04	00000	00000	Miss	No	No
0x10	00000	00000	Miss	No	No
0x84	00000	00000	Miss	No	No
0xE8	00100	00101	Hit	Yes	Yes
0xA0	00111	10101	Miss	No	No
0x400	00101	00101	Miss	No	No
0X1E	00100	00101	Miss	No	No
0x8C	00000	10101	Hit	No	No
0xC1C	00000	00000	Hit	Yes	Yes
0xB4	00100	00000	Miss	Yes	Yes
0X884	00101	00000	Miss	Yes	Yes

e)

The hit ratio is 33.33%.

f)

<00100, 0010, mem[2176]>
<00101, 0000, mem[160]>
<00000, 0011, mem[3072]>
<00111, 0000, mem[224]>

4.

a)

P1: 1/0.66ns = 1.515 GHz
P2: 1/0.9ns = 1.111 GHz

b)

AMAT = Hit Rate * Hit time + Miss Rate * Miss Time
P1 = 6.21ns
P2 = 5.06ns

c)

Miss Cycles = IC * Memory Access Freq * Miss Rate * Main Memory Access / L1 Hit Time
Total Cycles = IC + Miss Cycles
CPI = Total Cycles / Instruction Count
For P1, P1 = IC * 2.7 ns
For P2, P2 = IC * 3.2 ns
So P1 is faster.

5.

a)

It has 8 sets, 3 ways, 2 word blocks.

tag width: 58 bits

data fields 64 bits

b)

Address	Binary word Address	Tag	Index	Offset	Hit/Miss
0x03	00000011	0	0	3	Miss
0xB4	10110100	2	6	4	Miss
0x2B	00101011	0	5	3	Miss
0x02	00000010	2	7	6	Miss
0xBE	10111110	1	3	0	Miss
0x58	01011000	2	7	7	Hit
0xBF	10111111	0	1	6	Miss
0x0E	00001110	0	3	7	Miss
0x1F	00011111	2	6	5	Hit
0xB5	10110101	2	7	7	Hit
0xBF	10111111	2	7	2	Hit
0xBA	10111010	0	5	6	Hit
0x2E	00101110	3	5	6	Hit
0xCE	11001110	3	1	6	Miss

c)

Address	Binary word Address	Tag	Index	Offset	Hit/Miss
0x03	00000011	0	0	3	Miss
0xB4	10110100	5	5	0	Miss
0x2B	00101011	1	2	3	Miss
0x02	00000010	5	7	2	Miss
0xBE	10111110	2	6	0	Miss
0x58	01011000	5	7	3	Hit
0xBF	10111111	0	3	2	Miss
0x0E	00001110	0	7	3	Miss
0x1F	00011111	5	5	1	Hit
0xB5	10110101	5	6	3	Hit
0xBF	10111111	5	2	2	Miss
0xBA	10111010	1	3	2	Miss
0x2E	00101110	1	3	2	Miss
0xCE	11001110	6	3	2	Miss

6.

The maximum possible page number is,

$$\frac{2^{36}}{2^{13}} = 2^{23}$$

7.

Address	Result(H/M/PF)
0x123D	M
0x08B3	H
0x365C	H
0x871B	H
0xBEE6	PF
0x3140	H
0xC049	PF

TLB content:

Valid	Tag	Physical Page Number	Time Since Last Access
1	1	13	3
1	7	4	1
1	3	6	2
1	2	14	4

Page Table:

Index	Valid	Physical Page Number
0	1	5
1	1	13
2	1	14
3	1	6
4	1	9
5	1	11
6	0	Disk
7	1	4
8	0	Disk
9	0	Dist
10	1	3
11	1	12