EC605_Lab5

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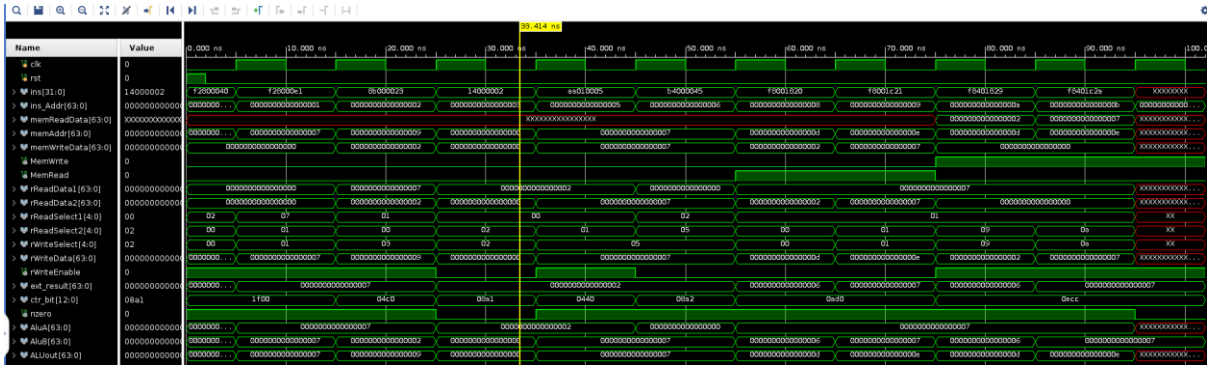
November 2021

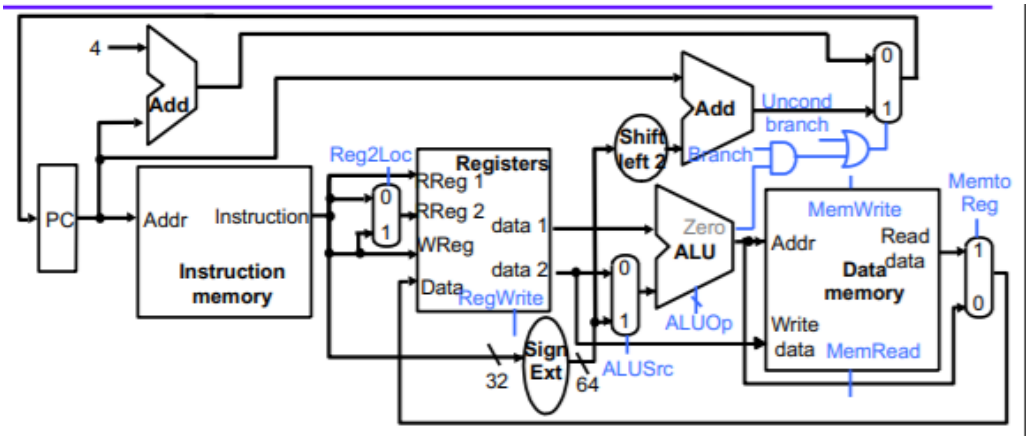
1. Final result



Pic1: final result of datapath

2. introduction

Datapath.v is our integrated document which includes all the components(modules) of our design. We follow the sequence of components in the picture2 which comes from the slide in class. Indeed, we have 11 components in our design from the left to right: PC(branch select), instruction memory, reg2loc, registers, sign extend, alusrc, alumovk, alu, memwrite, memtoreg and an extra control center which is not shown in the picture.



Pic2: main design instruction

A. PC(branch select)

In this module, we use three inputs, branch, unconbranch and nzero_flag to control the output address. The output address determines the instruction memory output---instruction.

B. Instruction memory

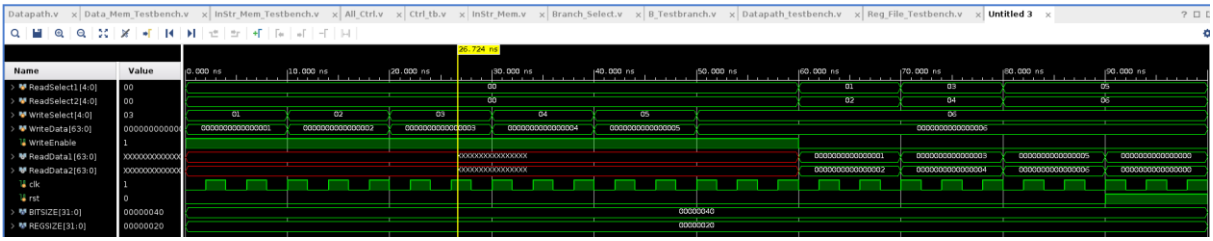
In this part, we input the address and output the instruction each clock cycle bacause for the whole system, the each single cycle running time will no more than one clock cycle.

C. Reg2loc

Choose the input of readselect2 from the ins[20:16] and ins[4:0]

D. Registers

We use it to select the output data from the registers and write specific data into a specific room/address. The input RegWrite decides the write enable.



Pic3: final result of register part

E. Sign extend

Based on the different kinds of instructions input, we can get choose different part of instruction and extend it into 64 bites.

F. Alusrc

We choose the input of ALUb from the data2 and the result of sign extend. Select is 0, out data2. select is 1, out sign extend.

G. Alumovk

We choose the input of ALUb from the data1 and the result of sign extend. Select is 0, out data1. select is 1, out sign extend.

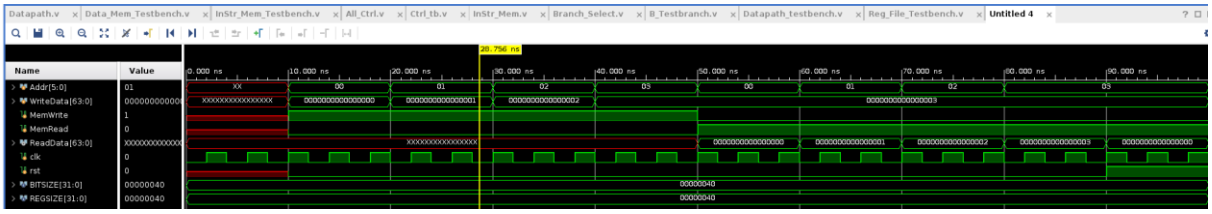
H. Alu

Save all the operation of calculation, here is the running result.

Pic4: final result of ALU

I. Memwrite

The memory is used by stur and ldur.



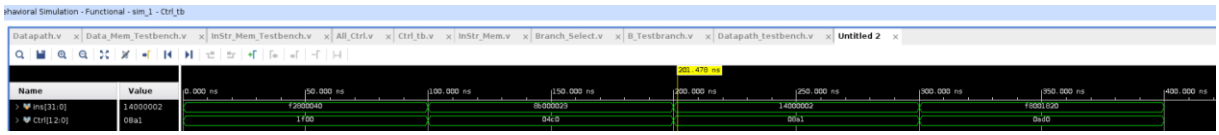
Pic5: final result of memory

J. Memtoreg

Designed for choose the register's writedata from the alu output and memory output. Select is 1 for memory output and 0 for alu output.

K. Control center

This part can output a 13 bits control signal for the whole system. The 13 bits is the sequence of "alu2, reg2loc, regwrite, alusrc, aluop(4bits), memwrite, memread, memtoreg, branch, uncondional branch".

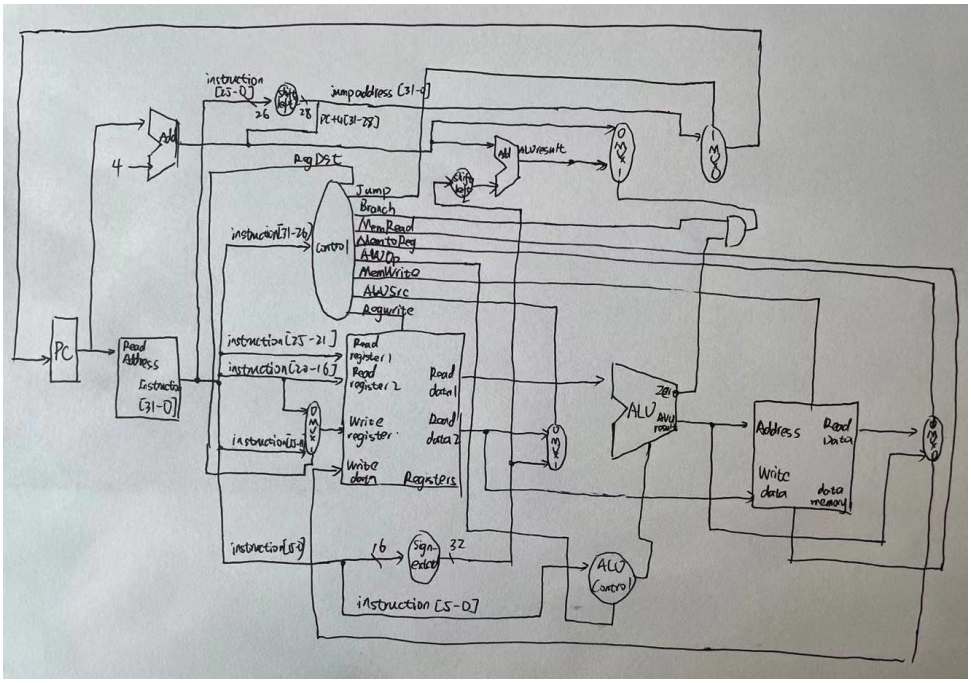


Pic6: final result of control center

3. Design for movk

In our design, comparing with the slide given in class, we add an extra mux module which uses for choosing the input of readdata2 and signed extend. In this way, when the instruction is the movk, the input of alu should be signed extend(aluA) and data2(aluB). In the ALU, we use the code {aluB[63:16], aluA[15:0]} to come out the output. In the part of register, we choose writeselect as the readselect2 which means set the select of reg2loc to 1.

4. Block Diagram of milestone2



Pic7: Diagram of milestone2