Task1: 8 bit Counter

Here is the final result and simulation of our task1. Because the image is really long, so I cut it into several parts.

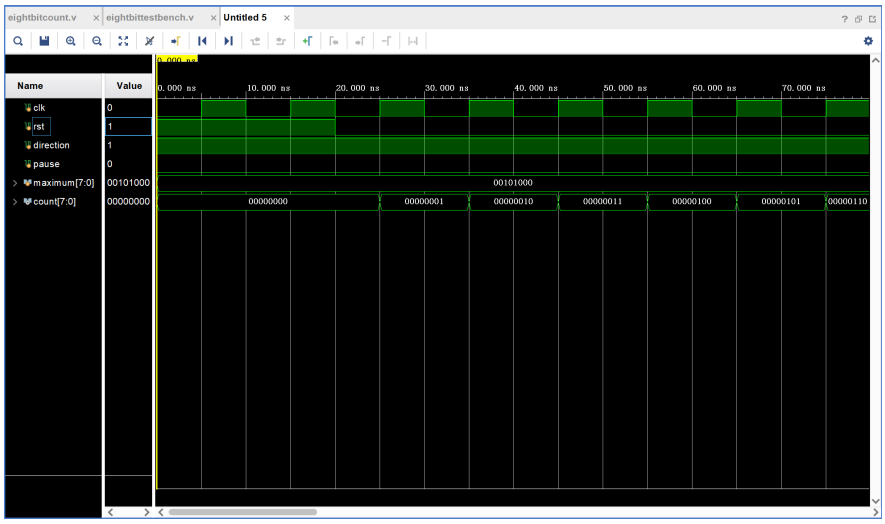

Figure 1: First part of simulation

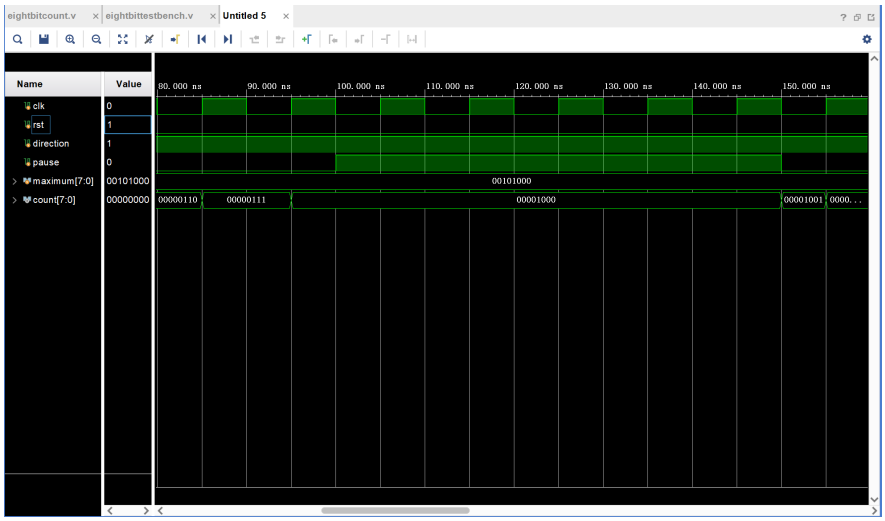

Figure 2: Second part of simulation

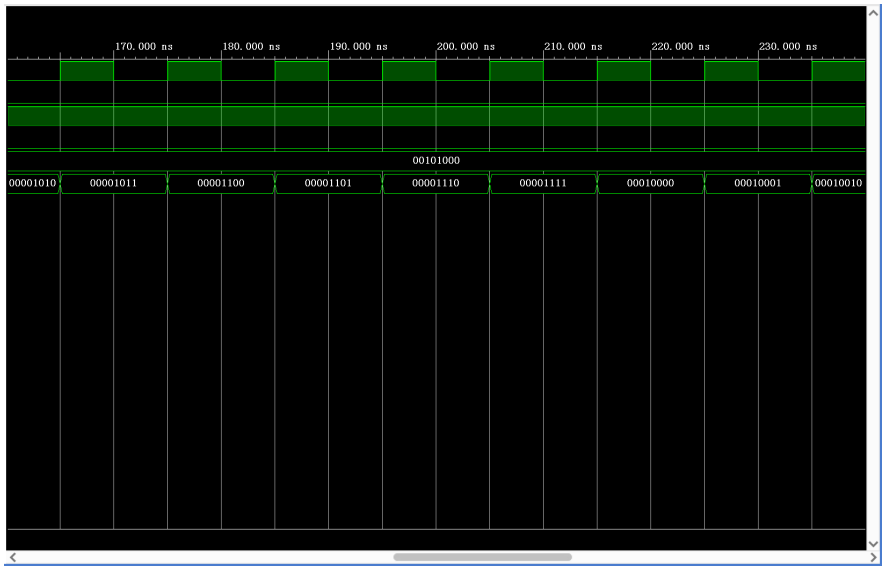

Figure 3: Third part of simulation

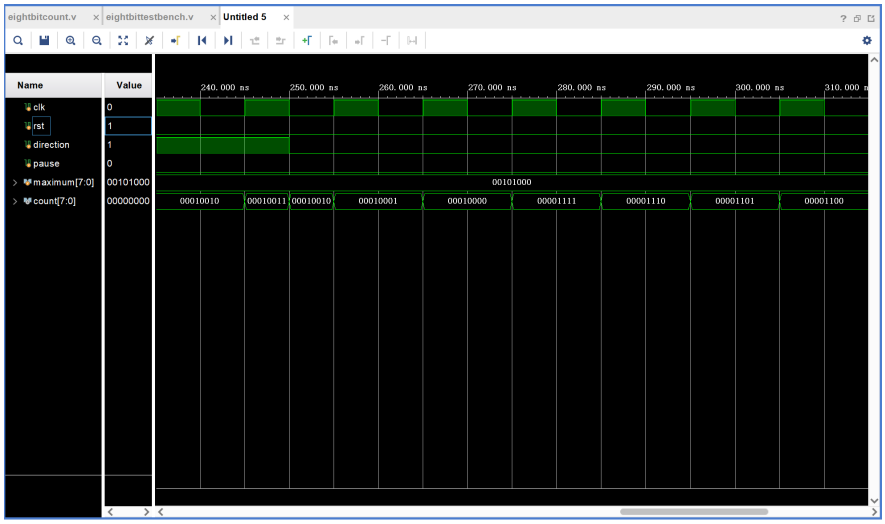

Figure 4: Fourth part of simulation

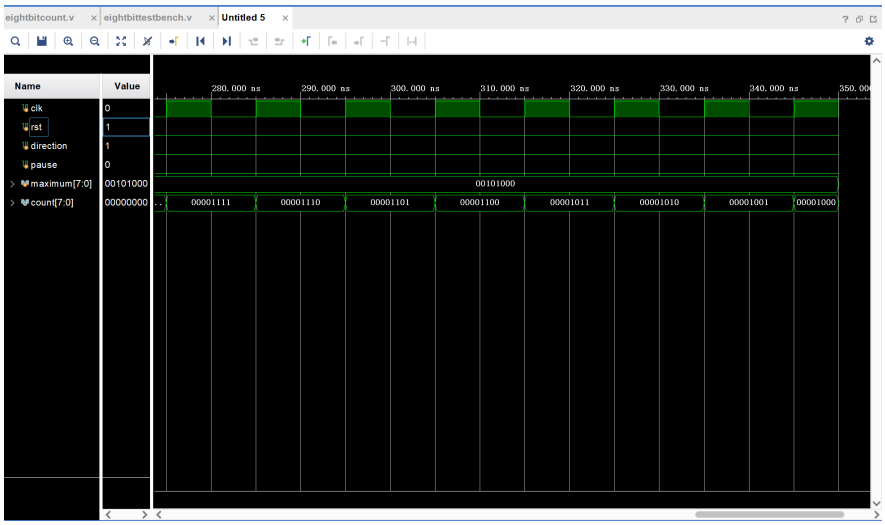

Figure 5: Fifth part of simulation

Task2: Clock Divider

We divide the initial 100 Mega Hz clock into 1 Hz clock. We use a count number to judge whether we need to give a positive edge to the new clock. After count number reaches 100000000, we give the output clock a positive edge. We run the simulation for several seconds and here I choose the first 4 seconds to show.

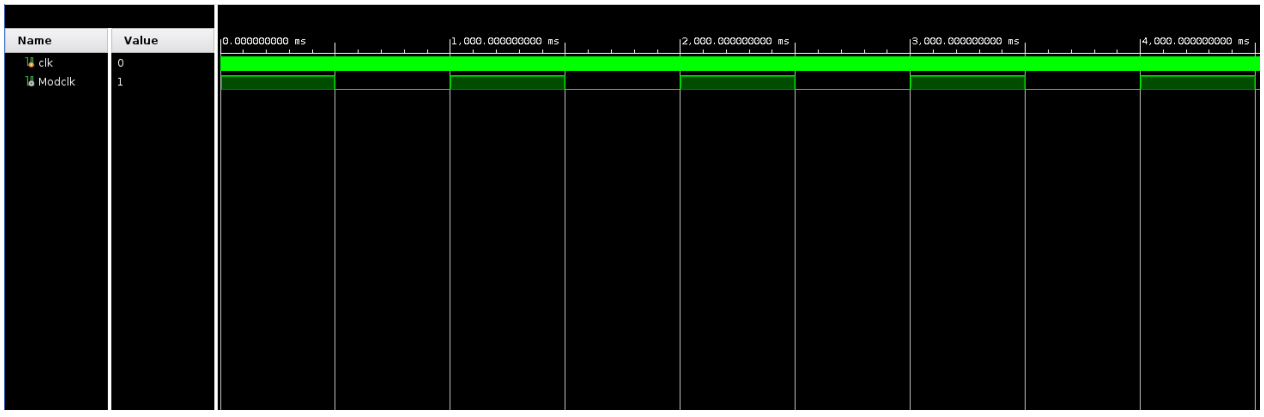

Figure 6: Divider

Task3: Wrap-around LEDs

First we draw the Moore-type FSM and here is the result.

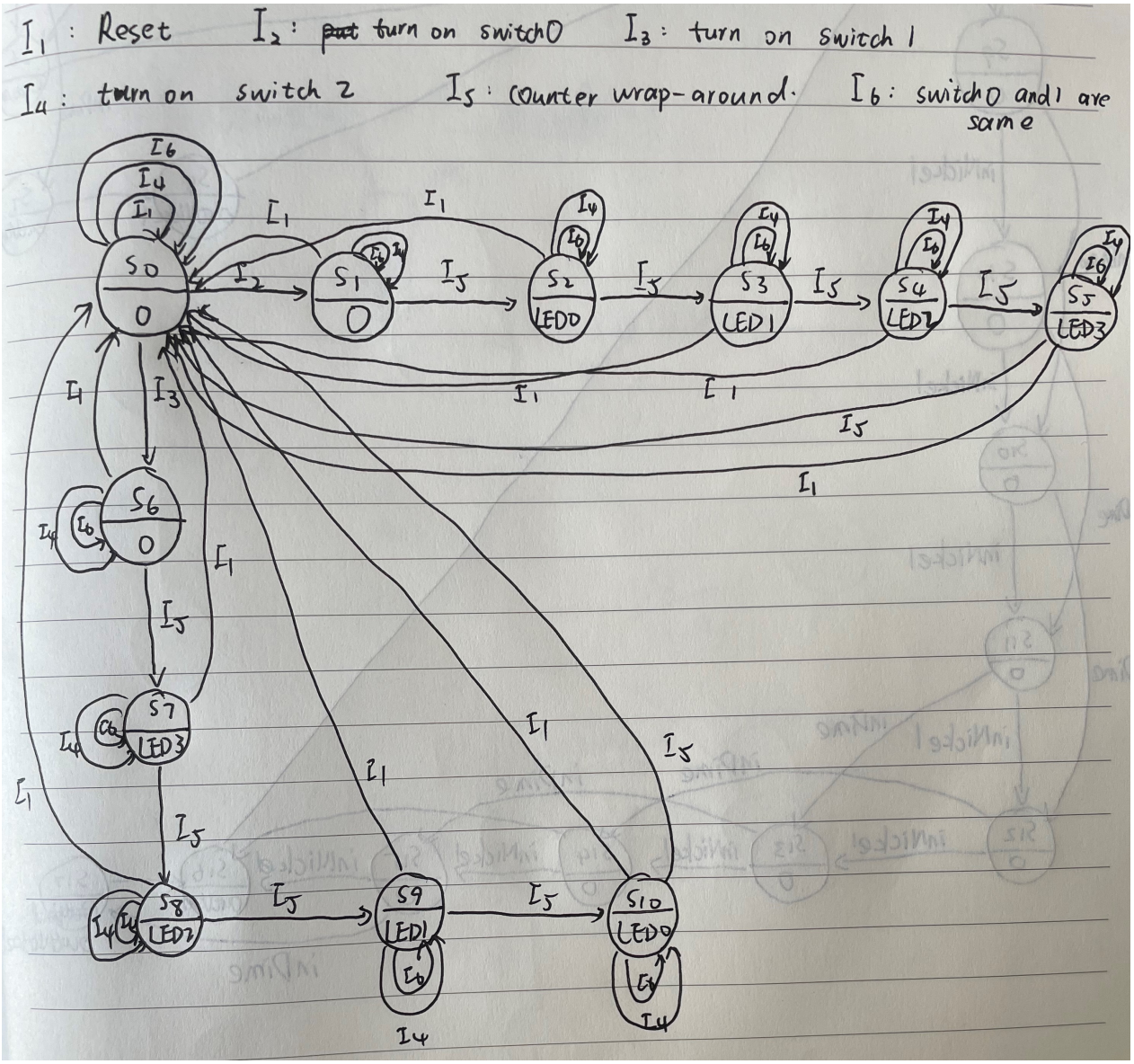

Figure 7: Moore-type FSM

Then we use the module in task1 and task2 and define the states by case function in verilog. In each state, the output will be the LEDs. And here is our simulation result.

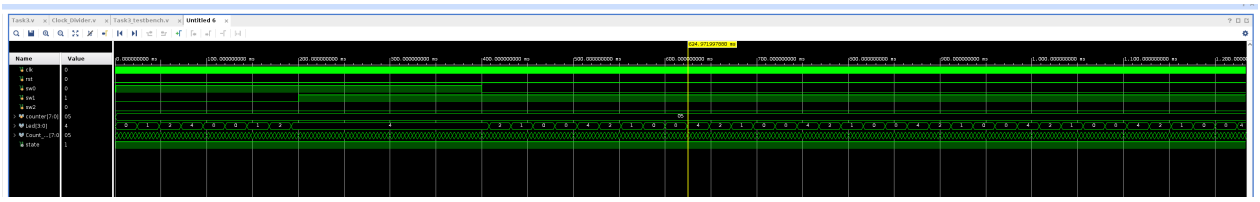

Figure 8: Wrap-around LEDs