Homework 4

Out: 10.20.21
Due: 10.27.21

1. [Single Cycle CPU]
   Consider the following instruction:
   And rd, Rn, Rm // Reg[Rd] = Reg[Rn] AND Reg[Rm]
   a) What are the values of control signals generated by the single-cycle control for this instruction?
   b) Which datapath resources (blocks) perform a useful function for this instruction?
   c) Which datapath resources (blocks) produce no output for this instruction? Which resources produce output that is not used?

2. [Single Cycle CPU]
   Consider the following instruction mix:
   R-type: 24%; I-type: 28%; ldur: 25%; stur: 10%; cbz: 11%; b: 2%
   a) What fraction of all instructions use the data memory?
   b) What fraction of all instructions use the instruction memory?
   c) What fraction of all instructions use the sign extend?
   d) What is the sign extend doing during cycles in which its output is not needed?

3. [Single Cycle CPU]
   When silicon chips are fabricated, defects in materials and manufacturing errors can result in defective circuits. A very common defect is for one signal wire to get "broken" and always register a logical 0. This is called a "stuck-at-0" fault.
   a) Which instructions fail to operate correctly if the *MemToReg* wire is stuck at 0?
   b) Which instructions fail to operate correctly if the *ALUSrc* wire is stuck at 0?
   c) Which instructions fail to operate correctly if the *Reg2Loc* wire is stuck at 0?

4. [Single Cycle CPU]
   Assume that during the current clock cycle the processor fetches the following instruction word: 0xF8014062.
   a) What are the outputs of the sign-extend and the "shift left 2" unit for this instruction word?
   b) What are the values of the ALU control unit's inputs for this instruction?
   c) What is the new PC address after this instruction is executed? List the path through which this value is determined.
   d) For each mux, specify the values of its inputs and outputs. List the values that are register outputs at Reg[Xn].
   e) What are the input values for the ALU and the two add units?
   f) What are the values of all inputs for the register file?

5. [Single Cycle CPU]
   a) What additional logic blocks, if any, are needed to add I-type instructions, such as addi or andi, to the single-cycle CPU? Explain.

b) List the values of the signals generated by the control unit for addi. Explain the reasoning for any "don't care" control signals.

6. [Performance]
   Consider three different processors: P1, P2, and P3, executing the same instruction set. P1 has a 3GHz clock rate and a CPI of 1.5. P2 has a 2.5GHz clock rate and a CPI of 1.0. P3 has a 4.0GHz clock rate and a CPI of 2.2.
   a) Which processor has the highest performance expressed in instructions per second?
   b) If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions.
   ~~c) We are trying to reduce the execution time by 30%, but this leads to an increase of 20% in the CPI, What clock rate should we have to get this time reduction?~~

7. [Performance]
   Consider two different implementations of the same instruction set architecture. The instructions can be divided into four classes according to their CPI (classes A, B, C, and D). P1 with a clock rate of 2.5GHz and CPIs of 1, 2, 3, and 3, and P2 with a clock rate of 3GHz and CPIs of 2, 2, 2, and 2.

   Given a program with a dynamic instruction count of $1.0*10^6$ instructions divided into classes as follows: 10% class A, 20% class B, 50% class C, and 20% class D, which is faster: P1 or P2?
   a) What is the global CPI for each implementation?
   b) Find the number of clock cycles required in both cases.