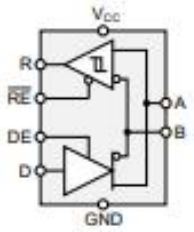
8 Detailed Description

8.1 Overview

The SN65HVD485E device is a half-duplex RS-485 transceiver suitable for data transmission at rates up to 10 Mbps over controlled-impedance transmission media (such as twisted-pair cabling). Up to 64 units of the SN65HVD485E device can share a common RS-485 bus due to the low bus-input currents of the device. The device also features a high degree of ESD protection and low standby current consumption of 1 mA (maximum).

8.2 Functional Block Diagram



8.3 Feature Description

The SN65HVD485E device provides internal biasing of the receiver input thresholds for open-circuit, bus-idle, or short-circuit failsafe conditions. It features a typical hysteresis of 30 mV to improve noise immunity. Internal ESD protection circuits protect the transceiver bus terminals against ±15-kV Human Body Model (HBM) electrostatic discharges.

8.4 Device Functional Modes

When the driver enable pin (DE) is logic high, the differential outputs A and B follow the logic states at data input D. A logic high at D causes A to turn high and B to turn low. In this case, the differential output voltage defined as $V_{OD} = V_A - V_B$ is positive. When D is low, the output states reverse, B turns high, A is low, and V_{OD} is negative.

When DE is low, both outputs turn high impedance. In this condition, the logic state at D is irrelevant. The DE pin has an internal pulldown resistor to ground; thus when left open, the driver is disabled (high impedance) by default. The D pin has an internal pullup resistor to VCC; thus when left open while the driver is enabled, output A turns high and B turns low.

Table 8-1. Driver Function Table

INPUT D	ENABLE DE	OUTPUTS		FUNCTION
		A	B	
H	H	H	L	Actively drive bus High
L	H	L	H	Actively drive bus Low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drive bus high by default

When the receiver enable pin ($\overline{RE}$) is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_A - V_B$ is positive and higher than the positive input threshold (V_{IT+}) the receiver output (R) turns high. When V_{ID} is negative and lower than the negative input threshold (V_{IT-}), the receiver output (R) turns low. If V_{ID} is between V_{IT+} and V_{IT-}, the output is indeterminate.

When $\overline{RE}$ is logic high or left open, the receiver output is high impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted (short-circuit), or the bus is not actively driven (idle bus).

Parameter Measurement Information

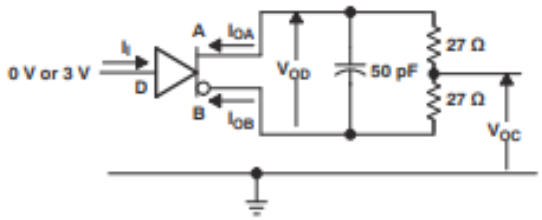


Figure 8-1. Driver Test Circuit, V_{OD} and V_{OC} Without Common-Mode Loading

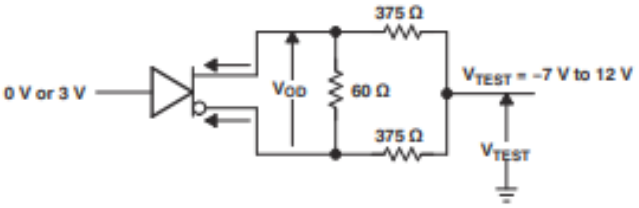


Figure 8-2. Driver Test Circuit, V_{OD} With Common-Mode Loading

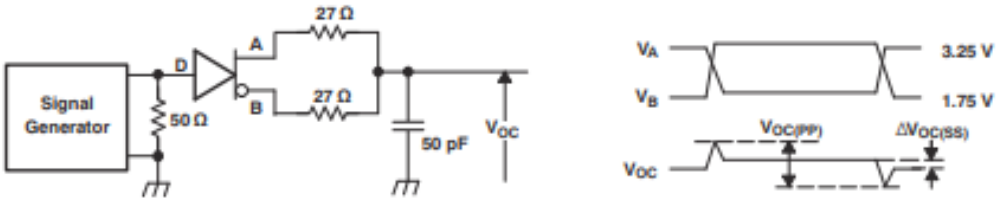


Figure 8-3. Driver V_{OC} Test Circuit and Waveforms

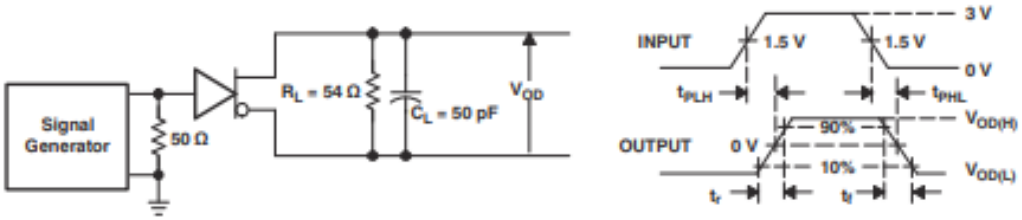


Figure 8-4. Driver Switching Test Circuit and Waveforms

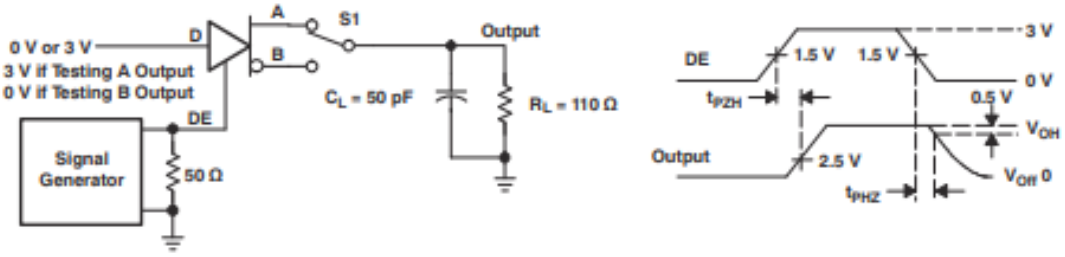
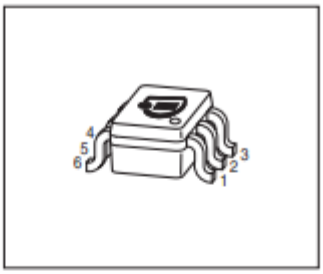
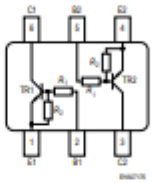


Figure 8-5. Driver Enable/Disable Test Circuit and Waveforms, High Output

NPN/PNP Silicon Digital Transistor Array

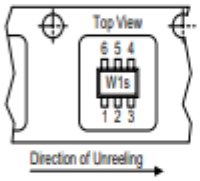




- Switching circuit, inverter, interface circuit, driver circuit
- Two (galvanic) internal isolated NPN/PNP Transistors in one package
- Built in bias resistor NPN and PNP (R_1=22 kΩ, R_2=22 kΩ)
- Pb-free (RoHS compliant) package
- Qualified according AEC Q101

AEC Qualified RoHS

Tape loading orientation



Marking on SOT-363 package (for example W1s) corresponds to pin 1 of device

Position in tape: pin 1 opposite of feed hole side

EH427193

Type	Marking	Pin Configuration						Package
BCR22PN	WPs	1=E1	2=B1	3=C2	4=E2	5=B2	6=C1	SOT363

Maximum Ratings for NPN and PNP Types

Parameter	Symbol	Value	Unit
Collector-emitter voltage	V_{CEO}	50	V
Collector-base voltage	V_{CBO}	50	
Input forward voltage	$V_{i(fwd)}$	60	
Input reverse voltage	$V_{i(rev)}$	10	
DC collector current	I_C	100	mA
Total power dissipation, T_S = 115 °C	P_{tot}	250	mW
Junction temperature	T_j	150	°C
Storage temperature	T_{stg}	-65 ... 150	
Thermal Resistance			
Junction - soldering point[1)]	R_{thJS}	≤ 140	K/W

[1]For calculation of R_{thJA} please refer to Application Note AN077 (Thermal Resistance Calculation)

Electrical Characteristics at T_A=25°C, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
DC Characteristics for NPN and PNP Types					
Collector-emitter breakdown voltage I_C = 100 µA, I_B = 0	$V_{(BR)CEO}$	50	-	-	V
Collector-base breakdown voltage I_C = 10 µA, I_E = 0	$V_{(BR)CBO}$	50	-	-	
Collector cutoff current V_{CB} = 40 V, I_E = 0	I_{CBO}	-	-	100	nA
Emitter cutoff current V_{EB} = 10 V, I_C = 0	I_{EBO}	-	-	350	µA
DC current gain 1) I_C = 5 mA, V_{CE} = 5 V	h_{FE}	50	-	-	-
Collector-emitter saturation voltage1) I_C = 10 mA, I_B = 0.5 mA	V_{CEsat}	-	-	0.3	V
Input off voltage I_C = 100 µA, V_{CE} = 5 V	$V_{i(off)}$	0.8	-	1.5	
Input on Voltage I_C = 2 mA, V_{CE} = 0.3 V	$V_{i(on)}$	1	-	2.5	
Input resistor	R_1	15	22	29	kΩ
Resistor ratio	R_1/R_2	0.9	1	1.1	-
AC Characteristics for NPN and PNP Types					
Transition frequency I_C = 10 mA, V_{CE} = 5 V, f = 100 MHz	f_T	-	130	-	MHz
Collector-base capacitance V_{CB} = 10 V, f = 1 MHz	C_{cb}	-	3	-	pF

1) Pulse test: t < 300µs; D < 2%

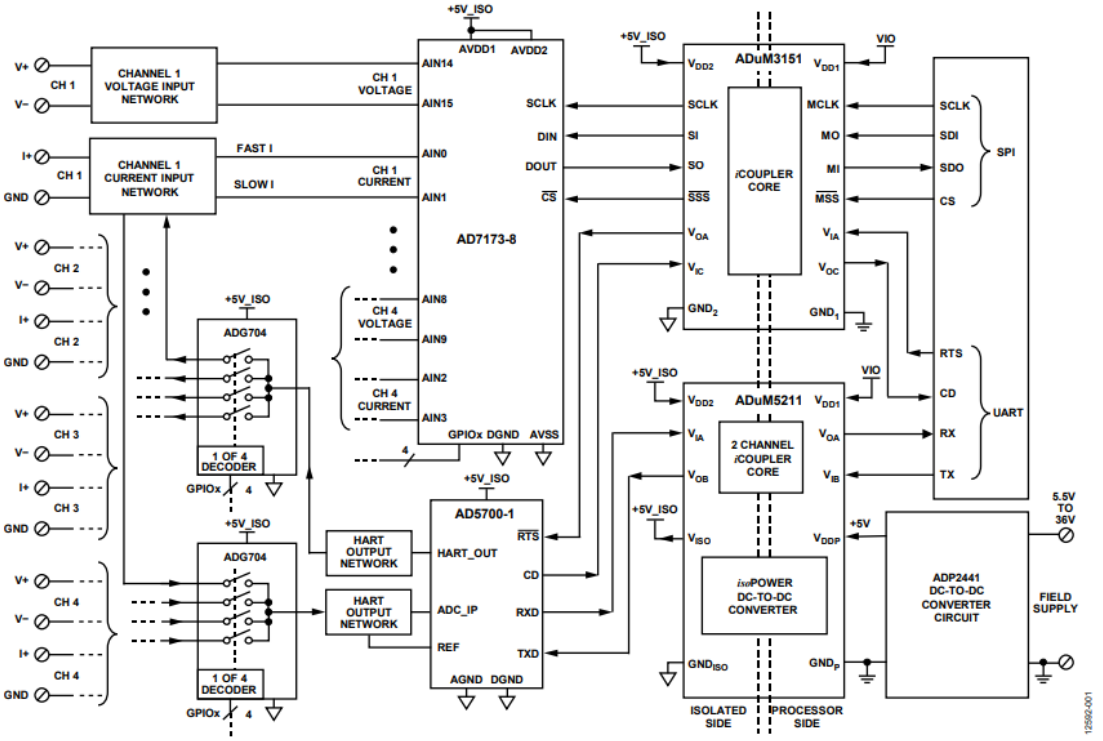


Figure 1. PLC/DCS Quad Channel Voltage and Current Input Front End (Simplified Schematic: All Connections and Decoupling Not Shown)

Table 1. Voltage Input Circuit Parameters (Maximum Values Based on Worst-Case Calculations)

Parameter	Value	Unit	Test Conditions/ Comments
Input Impedance	903	kΩ	
Divider Ratio	0.11		Resistor divider of 402 kΩ and 49.9 kΩ
Initial Error from Resistors	0.18	%FSR max	25°C, uncalibrated; assumed 0.1% resistors
Error from Input Leakage	±0.01	%FSR	±10 V range; AD7173-8, ±2 nA typical leakage
Error from Resistor Drift	18	ppm/°C max	Assumed 10 ppm/°C resistors
	9	ppm/°C max	Assumed 5 ppm/°C resistors
Error from Reference Drift	10	ppm/°C max	Internal reference
Common Mode	±5	V	
Data Rate	31.25	kSPS	1 input enabled (14.7 bit noise-free code resolution for ±10 V)
	1.55	kSPS	4 channels, each fully settled, sinc5+1 filter (14.7 bit noise-free code resolution for ±10 V)
	6.25	SPS	4 channels, each fully settled, 50 HZ/60 Hz reject (18.8 bit noise-free code resolution for ±10 V)
Input Filter	20	kHz	Differential
	200	kHz	Common mode

Current Input Circuit

Figure 3 shows the current input network for Channel 1.

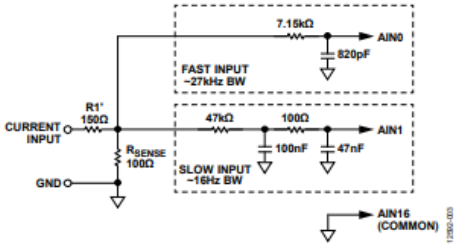


Figure 3. Current Input Equivalent Circuit (Simplified)

The circuit has four current input channels, supporting a maximum input range of 0 mA to 24 mA. The input impedance of the circuit is 250 Ω, and the input is referenced to ground. A precision 100 Ω current sense resistor is used so that a 24 mA input produces 2.4 V, which is within the 2.5 V full-scale range of the AD7173-8 (using the internal 2.5 V voltage reference). The board is populated by default with a 0.1%, 10 ppm/°C R_{SENSE} resistor.

There are two input paths to separate ADC inputs. The fast input path is for channels not using HART, and the slow input path is for channels using HART.

The fast input path allows signals up to the full input bandwidth of the Σ-Δ ADC. It is also possible to use the internal sinc filters to reject the 1.2 kHz and 2.2 kHz HART frequencies. However, using the sinc filters requires running the relevant channel at the 400 SPS data rate (sinc3 filter), which increases the time required to convert all four channels.

The slow input contains a 16 Hz double-pole filter, which filters out the 1.2 kHz and 2.2 kHz HART digital signaling frequencies. Using this input, the Σ-Δ ADC can still run at its fast data rate and also reject the HART digital signaling frequencies. The time required to convert all four channels is not reduced. Operating the ADC at its fast data rate is especially useful if not all channels have HART enabled.

Table 2 summarizes the current input circuit parameters.

Table 2. Current Input Circuit Parameters (Maximum Values Based on Worst-Case Calculations)

Parameter	Value	Unit	Test Conditions/ Comments
Input Impedance	250	Ω	Grounded
Error from Resistor	N/A[1]	%FSR max	Per R_{SENSE} resistor specifications
Error from Resistor Drift	N/A[1]	ppm/°C max	Per R_{SENSE} resistor specifications
Error from Reference Drift	10	ppm/°C max	Internal reference
Data Rate	31.25	kSPS	1 input enabled (14.8 bit noise-free code resolution for 0 mA to 20 mA)
	1.55	kSPS	4 channels, each fully settled, sinc5+1 filter (14.8 bit p-p resolution for 0 mA to 20 mA)
	6.25	SPS	4 channels, each fully settled, 50 Hz/60 Hz reject (18.1 bit p-p resolution for 0 mA to 20 mA)
Input Filter	27	kHz	Fast input
	16	Hz	Slow input providing HART filtering

[1] N/A = not applicable.