Q: Are all of these enough to get full marks in the exam?

A: NO. This is a practice sheet. Meaning, you can practice all you want using the questions from this sheet. However, doing well in exams depends upon your ability to understand a question, formulate an answer, and express it correctly. You see, these are humane skills which cannot be guaranteed by completing a practice sheet only. But yeah, Best of luck anyway.

Chapter 4 (The Processor)

Question - 1:

Draw a diagram of the register file, clearly indicating all input and output pins.
a. Provide a detailed explanation of how the register file performs both read and write operations.
b. **Explain** why the size of the read/write register pin is 5 bits.

Question - 2:

Draw a diagram of the ALU, clearly indicating all input and output pins.
a. **Explain** the significance of the Zero pin in the ALU.
b. **Describe** how the ALU determines which operation to perform on the given inputs.

Question - 3:

Draw a diagram of the ALU Control, clearly indicating all input and output pins.
a. Does the ALU control utilize Instruction bits 30 and 14-12 to generate the output for the LD instruction? Provide a justification for your answer.
b. **Identify** the specific cases in which the ALU control utilizes Instruction bits 30 and 14-12 to generate the output. **Additionally**, explain why only these four bits (Instruction bits 30 and 14-12) are used in such cases.

Question - 4:

Identify the necessary resources or components from the list provided to construct the datapath for each of the following instructions.

PC	Instruction Memory	Data Memory	Register File	ALU	Immediate Generation Unit	Control Unit	ALU Control

i.	ADD X_{21}, X_{22}, X_{23}
ii.	AND X_{21}, X_{22}, X_{23}
iii.	OR X_{21}, X_{22}, X_{23}
iv	ADDi X_{21}, X_{22}, 5
v.	LD X_{21}, 22(X_{21})
vi.	SD X_{21}, 22(X_{21})
vii	BEQ X_{21}, X_{22}, End

Question - 5:

Draw a simplified datapath with control unit that can process ADD X21, X22, X23

Question - 6:

Draw a simplified datapath with control unit that can process ADDI X21, X22, 5

Question - 7:

Draw a simplified datapath with control unit that can process LD X21, 14(X22)

Question - 8:

Draw a simplified datapath with control unit that can process only the following codes:
LD X21, 14(X22)
SD X22, 16(X21)
Mention the control signals also for each instructions.

Question - 9:

Draw a simplified datapath with control unit that can process only the following codes:

ADDI X21, X22, 5
LD X21, 14(X22)
Mention the control signals also for each instructions.

Question - 10:

Draw a simplified datapath with control unit that can process the following codes:
ADDI X21, X22, 5
LD X21, 14(X22)
Mention the control signals also for each instructions.

Question - 11:

Modify the BEQ datapath so that it works for **BNE.**
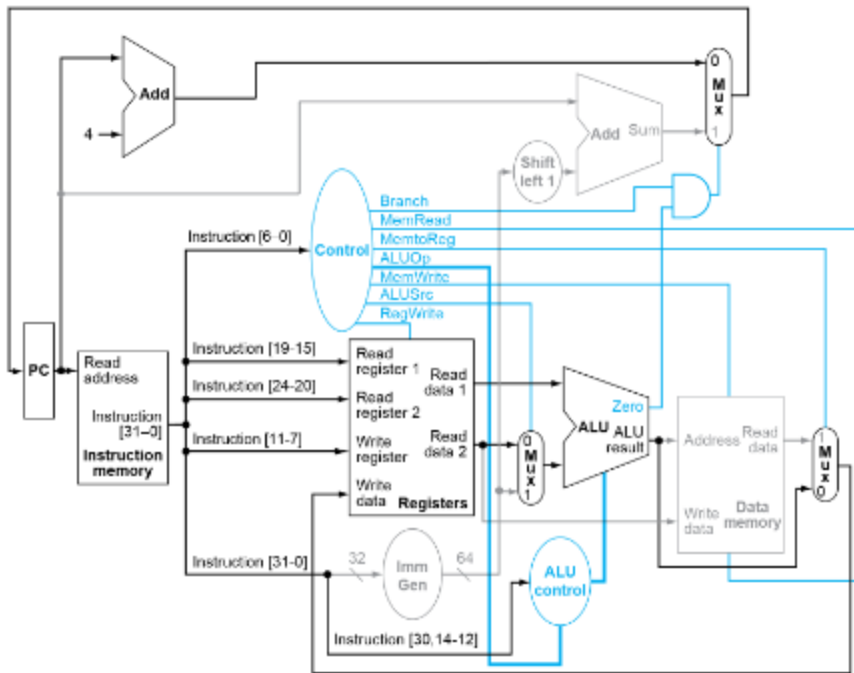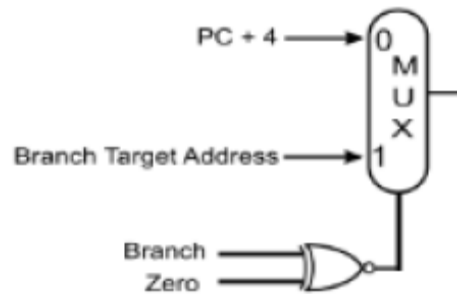
Question - 12:

Construct a single-cycle full-datapath, ensuring that you use only 4:1 multiplexer(s) wherever multiplexer(s) are required.

Question - 13:

Suppose that in a buggy implementation of the RISC V datapath, the AND gate for the branching decision was replaced with an **XNOR** gate. Describe how this error would affect the execution of the following instruction.

i. **SUB** x1, x2, x3 [3 points]
ii. **BEQ** x1, x2, target [3 points]

Question - 14:

Determine the values of the following control bits when executing the instruction "**Add** X21, X22, X23" in the provided single-cycle datapath.

Branch	MemWrite	RegWrite	ALUSrc

Question - 15:

Determine the values of the following control bits when executing the instruction "**Addi** X21, X22, 12" in provided single-cycle datapath for Q-14
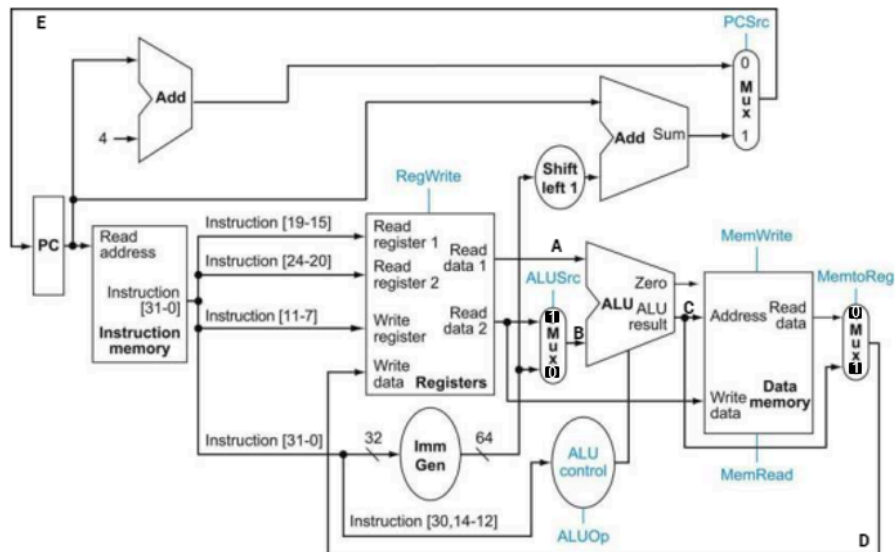
Branch	MemWrite	RegWrite	ALUSrc

Question - 16:

Determine the values of the following control bits when executing the instruction "**Add** X21, X22, X23" in the provided single-cycle datapath.

Branch	ALUSrc	RegWrite	MemToReg

Question - 17:

Study the above RISC-V Datapath thoroughly. Assume that initially $PC=600_h$, $x_1 = 222_h$, $x_2 = 444_h$, $x_3 = 666_h$, $x_4=999_h$.
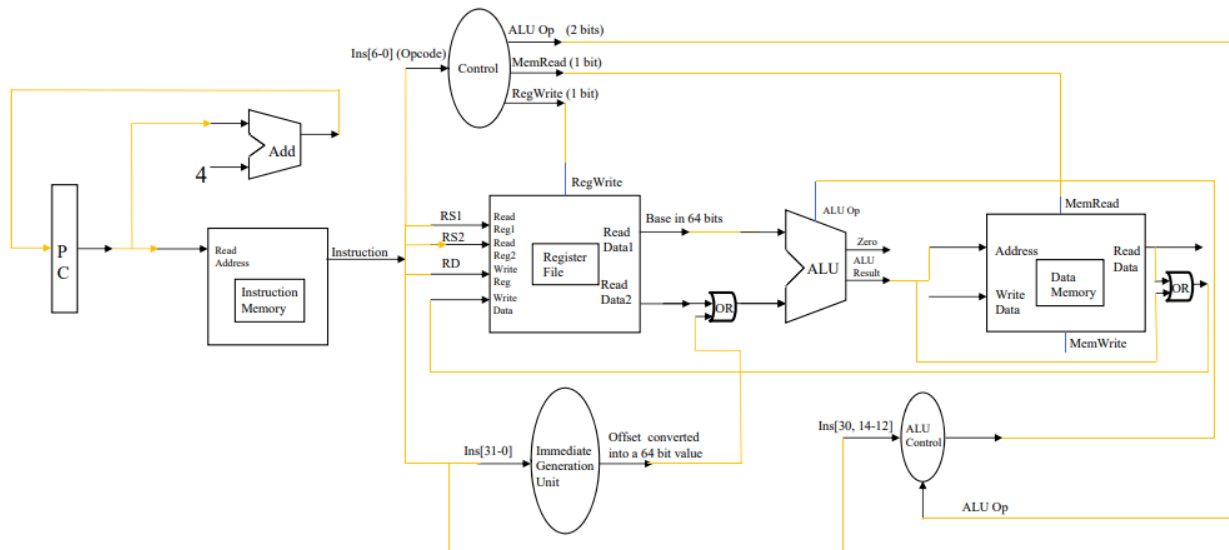
Determine the values of A, B, C, D, E in hex for the instructions executed **sequentially**. If the value does not matter, write it as X (don't care)

		A	B	C	D	E
i.	sub x_1, x_2, x_1					
ii.	sd x_4, $12(x_2)$					

Question - 18:

Carefully examine the RISC-V datapath provided in Q-17. Assume the initial values are: PC = 600h, x1 = 222h, x2 = 444h, x3 = 666h, and x4 = 999h. For the following instructions executed **sequentially**, **determine** the hexadecimal values of A, B, C, D, and E. If the value is irrelevant, indicate it as X (don't care).

i.	sub x_1, x_2, x_1						
ii.	sd x_4, $12(x_2)$						
		PC	A	B	C	D	E
iii.	Addi x_1, x_1, 12						

Question - 19:

Given the following code sequence:

1. ADD X1, X2, X3
2. LD X5, 10(X4)
3. OR X2, X3, X23

Is it possible to execute this code sequence using the provided datapath? If not, correct the datapath.

Question - 20:

Assume the memory is following Big Endian approach.
PC = 0x0040ABCD123045B1

Instruction Memory:

Address	Content
0x40ABCD123045AD	0111 0101
……………………………	1011 1110
……………………………	1001 0001

Data Memory:

Address	Content
0x40ABCD123045AD	0111 0101
……………………………	0111 0100
……………………………	1000 0000

…………………………	1100 0000	…………………………	1000 0001
…………………………	0000 0001	…………………………	0000 0000
…………………………	1001 0101	…………………………	0001 0111
…………………………	0000 0101	…………………………	1000 0101
…………………………	0011 0011	…………………………	1111 0011

Fetch the instruction from memory. **Convert** your answer in Hex.

Question - 21:

The following table shows the different stages involved in executing instructions and the corresponding durations for each stage:

stages	Instruction Fetch	Register Read	ALU Op	Memory Access	Register Write
Duration	50ps	10ps	30ps	20ps	10ps

Given the above durations, determine the total time required to complete each of the following instructions:

	Instructions	Time to complete each instructions
i.	ADD X_{21}, X_{22}, X_{23}	
ii.	AND X_{21}, X_{22}, X_{23}	
iii.	OR X_{21}, X_{22}, X_{23}	
iv	ADDi X_{21}, X_{22}, 18	
v.	LD X_{21}, 22(X_{21})	

	Instructions	Time to complete each instructions
vi.	SD X_{21}, 22(X_{21})	
vii	BEQ X_{21}, X_{22}, End	

Question - 22:

Instruction	Time (PS)
Add X21, X22, X23	10
Sub X21, X23, X24	20
Mul X22, X23, X26	15
LD X22, 0(X21)	25

The above instructions are being run in a **single cycle datapath**.
a. Now determine what is the clock period of this system?
b. What would be the total time to run this instruction sequence?

Question - 23 :

What do you understand by the term "**single-cycle**" in the context of a single-cycle datapath?

Question - 24 :

Stage	IF	ID	EX	MEM	WB
Time (PS)	10	20	20	20	10

The below instructions are being run in a pipelined datapath. Calculate the time required to execute each instruction.

Instruction	Time (PS)
Add X21, X22, X23	
Sub X21, X23, X24	
Mul X22, X23, X26	
LD X22, 0(X21)	

Determine what is the clock period of this system?

Question - 25 :

Write a comparison between the single cycle datapath and a pipelined datapath. Mention why pipelined datapath is implemented in real life.
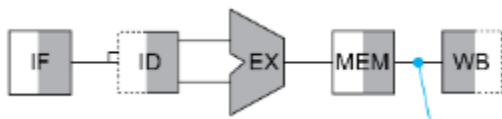
Question - 26 :

In the RISC-V pipelined datapath we have 5 stages. Can we divide these 5 stages into more stages to make the datapath more efficient?

Question - 27 :

Explain Why do data hazards occur in a pipelined Data path?

Question - 28 :

The instructions provided below are executed sequentially within a **pipelined** datapath that is divided into five stages, as depicted in the following diagram. In the diagram, the gray shaded areas represent the periods when tasks are actively being processed in each stage, whereas the unshaded (white) areas indicate inactive portions of each stage.

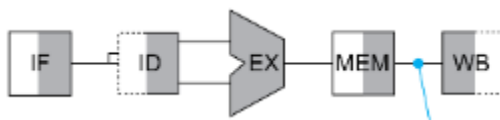| Instruction |
| --- |
| Add X21, X22, X23 |
| Sub X21, X21, X24 |
| Mul X22, X21, X26 |
| LD X22, 0(X21) |

Will any data hazards occur during the execution of this instruction set? If so, identify the number of data hazards and clearly circle them.

Question - 29 :

What do you understand about structural hazards? Explain with an example.

Question - 30 :

The instructions provided below are executed sequentially within a **pipelined** datapath that is divided into five stages, as depicted in the following diagram. In the diagram, the gray shaded areas represent the periods when tasks are actively being processed in each stage, whereas the unshaded (white) areas indicate inactive portions of each stage.

Instruction
Add X21, X22, X23
Sub X21, X20, X24
LD X22, 0(X22)

a. Will any data hazards occur during the execution of this instruction set? If so, identify the number of data hazards and clearly circle them.

b. How many clock cycles are necessary to run this instruction set?

Question - 31 :

The following are the time requirements for various stages of a datapath:

1. Instruction Fetch: 25 ps
2. Instruction Decode: 10 ps
3. Register Read: 15 ps
4. Arithmetic or Logical task execution: 20 ps
5. Data Memory Read: 20 ps
6. Data Memory Write: 20 ps
7. Register Write: 25 ps

You are given the following instruction set, executed sequentially:
1. Add X21, X22, X23
2. Sub X21, X23, X24
3. Mul X22, X22, X26
4. LD X22, 0(X20)

Suppose this instruction set is executed sequentially in a single cycle datapath. Answer the following:

a. **Calculate** the **actual** time required to execute each instruction.

b. **Determine** the clock period of this system.

c. **Calculate** the number of clock cycles needed to execute this instruction set.

d. **Determine** the total time required to execute this instruction set.

Now, assume the instruction set is executed sequentially in an ideal pipelined datapath with 5 stages.

Answer the following:

a. **Calculate** the actual time required to execute each instruction.

b. **Determine** the clock period of this system.

c. **Calculate** the number of clock cycles needed to execute this instruction set.

d. **Determine** the total time required to execute this instruction set.