SCT212-0056/2020 FAVOUR PAUL MUTURI
LAB 4

Problem A: Cache Tag Size and Performance Impact

Given:

- Cache Size = 256 KB = 2^{18} bytes
- Block Size = 64 bytes = 2^{6} bytes
- 4-way Set Associative → Number of sets = $(2^{18} / (4 \times 2^{6})) = 2^{18} / 2^{8} = 2^{10}$ sets
- Address size = 32 bits

(a) Tag size calculation

A memory address is divided into:

- Block offset bits: $\log_2$(Block size) = $\log_2(64)$ = 6 bits
- Index bits: $\log_2$(Number of sets) = $\log_2(1024)$ = 10 bits
- Tag bits: 32 − (6 + 10) = 16 bits

Answer: Tag size = 16 bits

(b) Performance speedup if all memory accesses hit in cache

Let's compute the effective CPI with cache misses:

Assume:

- Base CPI (all hits) = 1.0
- Miss rate = 2% = 0.02
- Miss penalty = 25 cycles

- 50% of instructions are memory accesses (0.5 per instruction)

Then:

- Misses per instruction = 0.5 × 0.02 = 0.01
- Extra CPI due to misses = 0.01 × 25 = 0.25

So:

- Actual CPI = 1.0 (base) + 0.25 (misses) = 1.25

Speedup if all hits:

Speedup=1.251.0=1.25×\text{Speedup} = \frac{1.25}{1.0} = 1.25\times

Answer: The computer would be 1.25 times faster if all memory accesses were hits.

Problem B: Memory Bandwidth Usage

Given:

- 95% hit rate → 5% miss rate
- 1 billion references/sec (1 GHz)
- 25% are writes = $0.25 \times 10^9 = 2.5 \times 10^8$ writes/sec
- 75% are reads = 7.5×10^8 reads/sec
- Block size = 2 words = 2-word transfer on miss
- Bus transfers 1 word at a time
- 30% of blocks in cache are dirty
- Write-allocate on write miss

(a) Write-through cache

- Read miss: brings 2 words = 2 transfers per miss
- Write hit: writes to both cache and memory → 1 memory write per hit
- Write miss: bring 2 words (read) + write 1 word = 3 transfers per miss

Reads:

- Miss rate = 5% of $0.75 \times 10^9 = 3.75 \times 10^7$
- Bandwidth for read misses = $3.75 \times 10^7 \times 2 = 7.5 \times 10^7$ words/sec

Writes:

- Hits = 95% of $0.25 \times 10^9 = 2.375 \times 10^8 \rightarrow 2.375 \times 10^8$ writes/sec to memory
- Misses = 5% of $0.25 \times 10^9 = 1.25 \times 10^7$
- Bandwidth for write misses = $1.25 \times 10^7 \times 3 = 3.75 \times 10^7$ words/sec

Total bandwidth:

7.5×107+2.375×108+3.75×107=3.5×108 words/sec7.5 \times 10^7 + 2.375 \times 10^8 + 3.75 \times 10^7 = 3.5 \times 10^8\ \text{words/sec} Bandwidth usage=3.5×108109=35%\text{Bandwidth usage} = \frac{3.5 \times 10^8}{10^9} = 35\%

Answer (a): 35% memory bandwidth usage (write-through)

(b) Write-back cache

- Only write back dirty blocks on replacement
- Read miss: 2 words = 2 transfers
- Write miss (write-allocate): 2 word read + maybe write back dirty = 2 or 4 words
- Assume 30% blocks dirty → 30% chance to write back 2 extra words

Read misses:
Same as before: $3.75 \times 10^7 \times 2 = 7.5 \times 10^7$

Write misses:
1.25×10^7 misses:

- 70% clean → 1.25e7 × 0.7 × 2 = 1.75e7
- 30% dirty → 1.25e7 × 0.3 × (2 + 2) = 1.5e7

Total write bandwidth = 1.75e7 + 1.5e7 = 3.25e7

Total bandwidth:
7.5e7 + 3.25e7 = 1.075×10^8 words/sec

Bandwidth usage=1.075×108109=10.75%\text{Bandwidth usage} = \frac{1.075 \times 10^8}{10^9} = 10.75\%

Answer (b): 10.75% memory bandwidth usage (write-back)