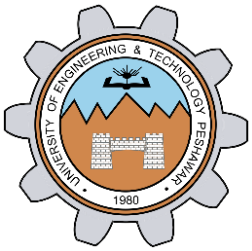
# DLD

# LAB # 09




## Fall 2020

Submitted by: **FAWAD ALI, JAMAL KAHN**

Registration No: **19PWCSE1845, 19PECSR1850**

Semester: **3rd**

Class Section: **C**

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"On my honor, as student of University of Engineering and Technology, I have neither given nor received unauthorized assistance on this academic work."

**Student Signature: _____**

Submitted to:

**Engr. Rehmat Ullah**

DEPARTMENT OF COMPUTER SYSTEMS ENGINEERING

## AIM:

Verification of state tables of R-S and D flip-flops (with PRESET and CLEAR inputs) using NAND gates.

## OBJECTIVES:

After completing this experiment, you will be able to:

We know about the latch and flip flop.

We know about the SR and D flip flop.

We can be create the flip flop using the logic gates.

## EQUIPMENT:

- Dc power supply
- Breadboard

## COMPONENTS:

- IC 7410 quad 3-input NAND gate
- LEDs
- DIP switch
- Wires

## THEORY:

## LATCH:

Latch is an electronic logic circuit with two stable states i.e. it is a bistable multivibrator. Latch has a feedback path to retain the information. Hence a latch can be a memory device. Latch can store one bit of information as long as the device is powered on. When enable is asserted, latch immediately changes the stored information when the input is changed i.e. they are level triggered devices. It continuously samples the inputs when the enable signal is on.
Latch circuits can work in two states depending on the triggering signal being high or low: Active – High or Active – Low.

- In case of Active – High latch circuits, normally both the inputs are low. The circuit is triggered by a momentary high on either of the inputs.
- In case of Active – Low latch circuits, normally both the inputs are high. The circuit is triggered by a momentary low on either of the inputs.

## FLIP-FLOP:

In case of sequential circuits the effect of all previous inputs on the outputs is represented by a state of the circuit. Thus, the output of the circuit at any time depends upon its current state and the input. These also determine the next state of the circuit. The relationship that exists among the inputs, outputs, present and next states can be specified by either the state table or the state diagram. The state table representation of a sequential circuit consists of three sections labelled present state, next state and output. The present state designates the state of flip-flops before the occurrence of a clock pulse. The next state shows the states of flip-flops after the clock pulse, and the output section lists the value of the output variables during the present state.

## Latch vs Flip-Flop:

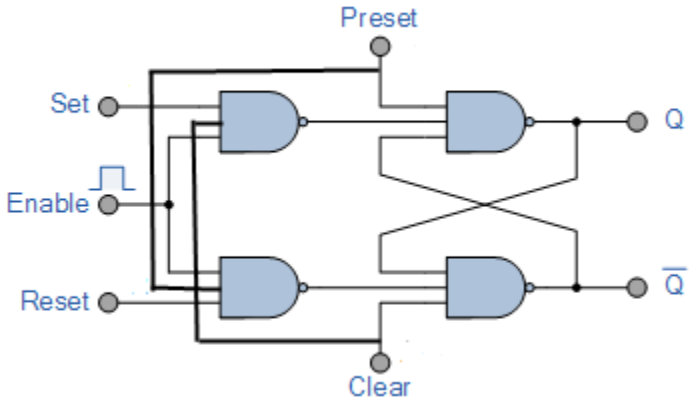
The circuit is similar to latch except enable signal is replaced by clock pulse.

## R-S Latch vs R-S Flip-Flop:

The circuit is similar to R-S latch except enable signal is replaced by clock pulse.

An RS flip flop is similar to RS latches. This type of flip flop has two inputs; SET and RESET, and a CLOCK input. When the clock is triggered, the Q output goes high if the SET input is high. On the other hand, the Q output goes low if the RESET input is high. Remember that SR flip flops have two inputs; the SET and the RESET, and should not be set to high when the clock is triggered. This type of flip flop operates only with positive clock transitions or negative clock transitions.

## LOGIC DIAGRAM:



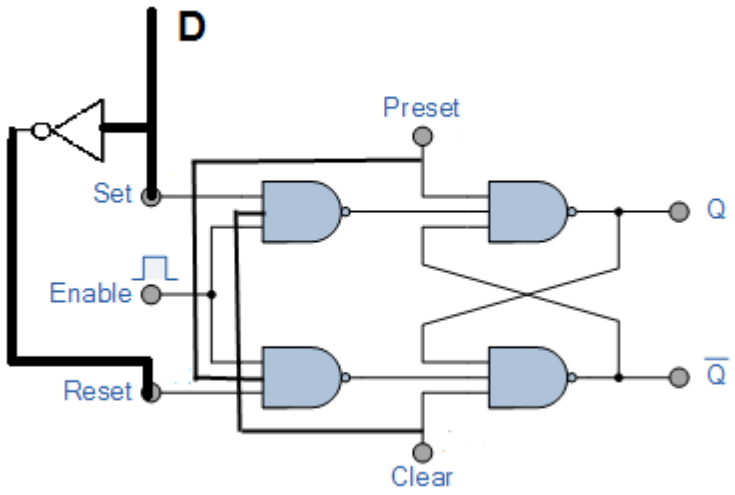

## TRUTH TABLE:

| EN | S | R | PRE | CLR | Q (t+1) |
|---|---|---|---|---|---|
| X | X | X | 0 | 1 | 1 (SET) |
| X | X | X | 1 | 0 | 0 (RESET) |
| 0 | X | X | 1 | 1 | Qt (NC) |
| 1 | 1 | 1 | 1 | 1 | 1 (SET) |
| 1 | 0 | 0 | 1 | 1 | 0 (RESET) |
| 1 | 0 | 1 | 1 | 1 | Qt (NC) |
| 1 | 1 | 0 | 1 | 1 | Indeterminate |

## D FLIP-FLOP:

A D flip-flop has a single data input. This type of flip-flop is obtained from the R-S flip-flop by connecting the R input through an inverter, and the S input is connected directly to data input. The modified clocked R-S flip-flop is known as D flip-flop and is shown below. From the truth table of R-S flip-flop we see that the output of the R-S flip-flop is in unpredictable state when the inputs are high. In many practical applications, these input conditions are not required. These input conditions can be avoided by making them complement of each other.

## LOGIC DIAGRAM:




## TRUTH TABLE:

| EN | D | PRE | CLR | Q (t+1) |
|---|---|---|---|---|
| X | X | 0 | 1 | 1 (SET) |
| X | X | 1 | 0 | 0 (RESET) |
| 0 | X | 1 | 1 | Qt (NC) |
| 1 | 0 | 1 | 1 | 0 (RESET) |
| 1 | 1 | 1 | 1 | 1 (SET) |

## PROCEDURE:

1. Connections are made as per circuit diagram.
2. Verify truth- tables for various combinations of input.

## PRECAUTION:

1. All the ICs should be checked before using the apparatus.
2. All LEDs should be checked.
3. All connections should be tight.
4. Always connect GROUND first and then VCC.
5. The circuit should be off before changing the connections.
6. After completing the experiment switch off the supply to apparatus.

## PRE LAB QUESTIONS:

**1) Differentiate between combinational and sequential circuits.**

**Ans.** A circuit whose output is dependent only on the inputs at that instant is called combinational circuit. And a circuit whose output is dependent on present and past history of the inputs is called sequential circuit.

**2) What is a latch?**

**Ans**. Storage elements that operate with signal levels are referred to as latches.

**3) What is a flip-flop?**

**Ans**. Storage elements controlled by clock transitions are called flip-flops.

## CONCLUSION:

Thus the **S-R and D flip flop and latch** are studied. We have to draw the logic function and logic diagram in verify by experimental to the truth table in the logic gates.