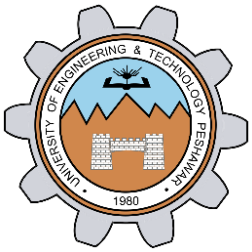
DECODERE AND NCODER

LAB # 06



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"On my honor, as student of University of Engineering and Technology, I have neither given nor received unauthorized assistance on this academic work."

Student Signature: _____

Submitted to:

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DEPARTMENT OF COMPUTER SYSTEMS ENGINEERING

DECODERE AND NCODER

OBJECTIVES:

After completing this experiment, you will be able to:

- Design and construct Decoder and Encoder
- Verify their truth tables using logic gates

EQUIPMENT:

- Dc power supply
- Breadboard

COMPONENTS:

- 7432 quad 2-input OR gate
- 7410 quad 3-input NAND gate
- 7404 hex inverter
- LEDs
- DIP switch
- Two 280 Ω resistors
- Wires

THEORY:

DECODER:

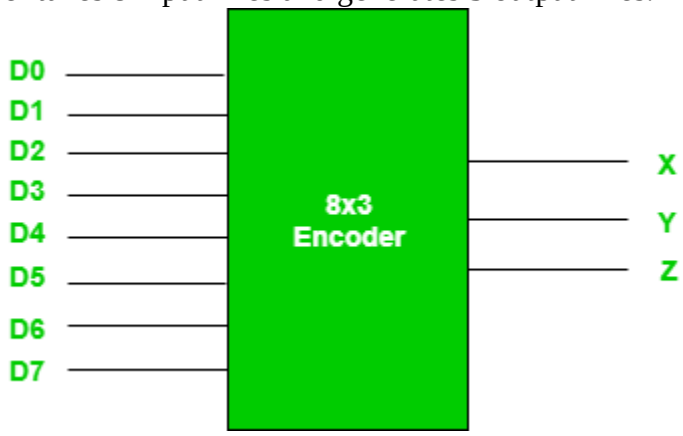
The name "Decoder" means to translate or decode coded information from one format into another, so a binary decoder transforms "n" binary input signals into an equivalent code using 2^n outputs.

Binary Decoders are another type of digital logic device that has inputs of 2-bit, 3-bit or 4-bit codes depending upon the number of data input lines, so a decoder that has a set of two or more bits will be defined as having an *n*-bit code, and therefore it will be possible to represent 2^n possible values. Thus, a decoder generally decodes a binary value into a non-binary one by setting exactly one of its *n* outputs to logic "1".

If a binary decoder receives n inputs (usually grouped as a single Binary or Boolean number) it activates one and only one of its 2^n outputs based on that input with all other outputs deactivated.

ENCODER:

An encoder is a combinational circuit that converts binary information in the form of a 2^N input lines into N output lines, which represent N bit code for the input. For simple encoders, it is assumed that only one input line is active at a time.
As an example, let's consider **Octal to Binary** encoder. As shown in the following figure, an octal-to-binary encoder takes 8 input lines and generates 3 output lines.



TRUTH TABLE :

D7	D6	D5	D4	D3	D2	D1	D0	X	Y	Z
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

As seen from the truth table, the output is 000 when D0 is active; 001 when D1 is active; 010 when D2 is active and so on.

IMPLEMENTATION:

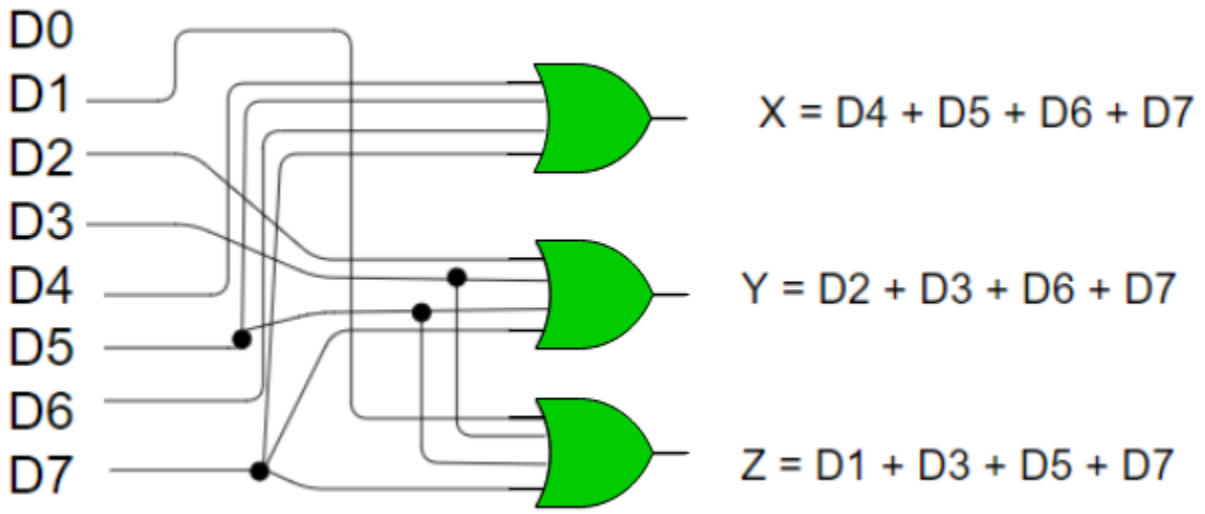
From the truth table, the output line Z is active when the input octal digit is 1, 3, 5 or 7. Similarly, Y is 1 when input octal digit is 2, 3, 6 or 7 and X is 1 for input octal digits 4, 5, 6 or 7. Hence, the Boolean functions would be:

X = D4 + D5 + D6 + D7

Y = D2 +D3 + D6 + D7

Z = D1 + D3 + D5 + D7

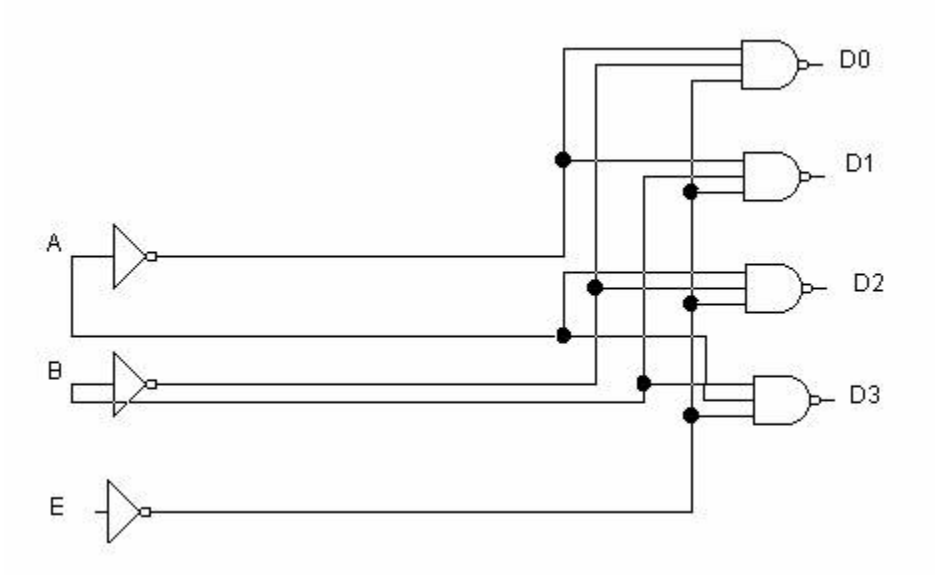
Hence, the encoder can be realised with OR gates as follows:



One limitation of this encoder is that only one input can be active at any given time. If more than one inputs are active, then the output is undefined. For example, if D6 and D3 are both active, then, our output would be 111 which is the output for D7. To overcome this, we use Priority Encoders.

Another ambiguity arises when all inputs are 0. In this case, encoder outputs 000 which actually is the output for D0 active. In order to avoid this, an extra bit can be added to the output, called the valid bit which is 0 when all inputs are 0 and 1 otherwise.

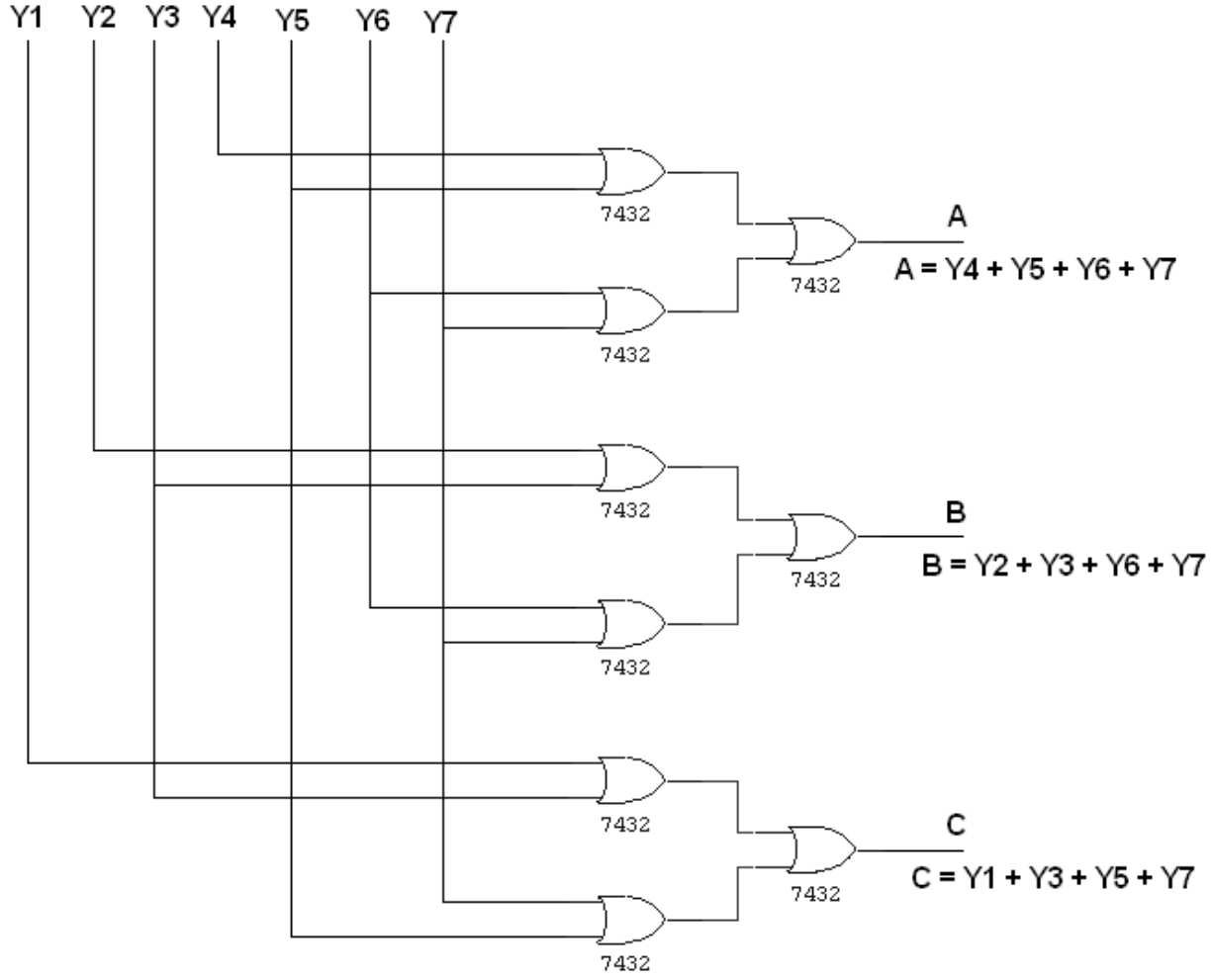
LOGIC DIAGRAM FOR DECODER:



TRUTH TABLE:

INPUT			OUTPUT			
E	**A**	**B**	**D0**	**D1**	**D2**	**D3**
1	**X**	**X**	**1**	**1**	**1**	**1**
0	**0**	**0**	**0**	**1**	**1**	**1**
0	**0**	**1**	**1**	**0**	**1**	**1**
0	**1**	**0**	**1**	**1**	**0**	**1**
0	**1**	**1**	**1**	**1**	**1**	**0**

LOGIC DIAGRAM FOR ENCODER:



TRUTH TABLE:

INPUT							OUTPUT		
Y1	Y2	Y3	Y4	Y5	Y6	Y7	A	B	C
1	0	0	0	0	0	0	0	0	1
0	1	0	0	0	0	0	0	1	0
0	0	1	0	0	0	0	0	1	1
0	0	0	1	0	0	0	1	0	0
0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	1	1	1	1

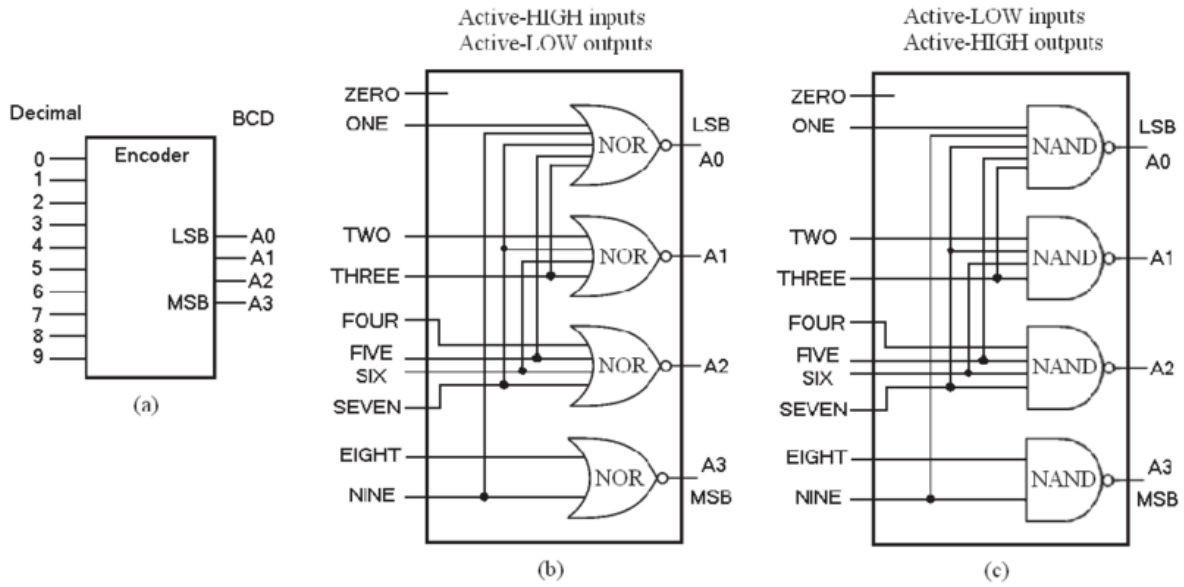
PROCEDURE:

1. Connections are given as per circuit diagram.
2. Logical inputs are given as per circuit diagram.
3. Observe the output and verify the truth table.

REVIEW QUESTIONS:

Q1: Design an Encoder using NOR gates only.

ANS:



Q2: What will be the output of the Decoder circuit if NAND gates are replaced by AND gates?

ANS: The output of the decoder in NAND gates is the low output in thus the NAND Gate replace by the AND gate which the output is high active because the NAND gate is the opposite of the AND gate.

Q3: What is the purpose of enable input in Decoder?

ANS: The enable input in decoder to use which the decoder is active are inactive to use for the decoder is off or on which decoder is work or not this purpose is use.

Q4: Design a 3x8 Decoder using two 2x4 Decoders (74LS139).

ANS:

Lab#2: Design a 3-to-8 decoder using 2-to-4 decoders

A 3-to-8 decoder can be built using two 2-to-4 decoders plus some basic logic gates as shown in the following figure.

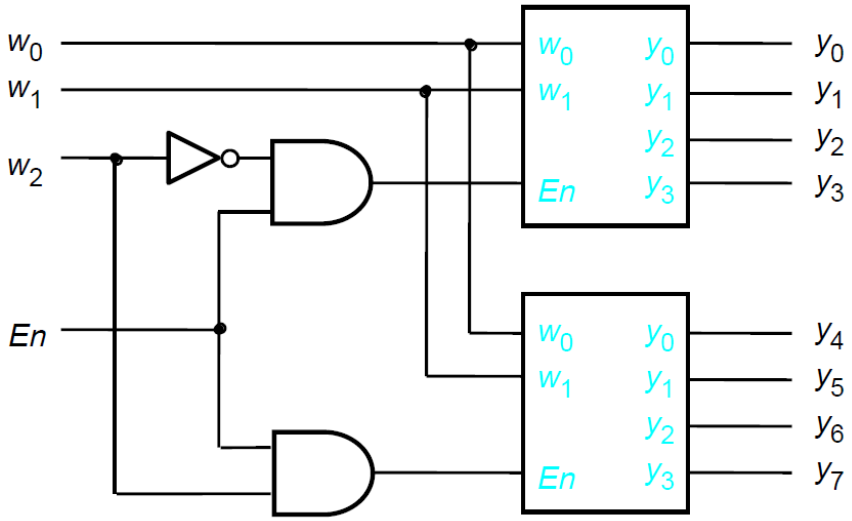


Figure 6.17 of the book -- A 3-to-8 decoder using two 2-to-4 decoders.

CONCLUSION:

Thus DECODERE AND NCODER are studied. They have studied they have to draw the logic function and logic diagram in verify by experimental to the truth table in the logic gates.