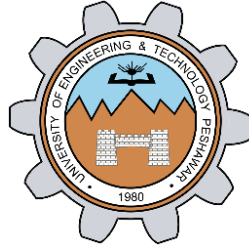


ADDER AND SUBTRACTOR

LAB # 05



Fall 2020

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Class Section: **C**

Date: **24:12:2020**

“On my honor, as student of University of Engineering and Technology, I have neither given nor received unauthorized assistance on this academic work.”

Student Signature: _____

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DEPARTMENT OF COMPUTER SYSTEMS ENGINEERING

ADDER AND SUBTRACTOR

OBJECTIVES:

After completing this experiment, you will be able to:

- Design and construct half adder, full adder, half subtractor and full subtractor circuits
- Verify their truth tables using logic gates.

EQUIPMENT:

- Dc power supply
- Breadboard

COMPONENTS:

- 7432 quad 2-input OR gate
- 7408 quad 2-input AND gate
- 7486 quad 2-input XOR gate
- 7404 hex inverter
- LED
- DIP switch
- Two 280 Ω resistors
- Wires

THEORY:

A digital adder circuit adds binary signals & a subtractor subtracts binary signals. Half Adder/Subtractor is a basic circuit that adds / subtracts 2 bits and generates Sum or Difference along with Carry / Borrow. Unlike Half Adder or Subtractor a Full Adder / Subtractor has the provision to take consideration of previous Carry / Borrow also.

➤ Introduction:

In electronics, an adder or summer is a digital circuit that performs addition of numbers. In many computers and other kinds of processors, adders are used not only in the arithmetic logic unit(s), but also in other parts of the processor, where they are used to calculate addresses, table indices, and similar.

➤ Half Adder:

A **half adder** adds two one-bit binary numbers A and B. It has two outputs, S and C (the value theoretically carried on to the next addition); the final sum is $2C + S$. The simplest half-adder design, pictured on the right, incorporates an XOR gate for S and an AND gate for C. Half adders cannot be used compositely, given their incapacity for a carry-in bit.

➤ Truth Table:

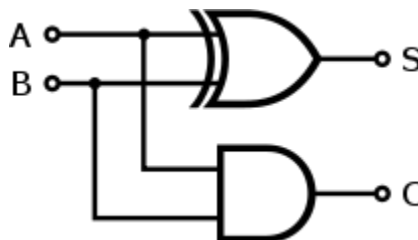
A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

➤ Logic Function:

$$\text{➤ } S = A \text{ xor } B.$$

$$\text{➤ } C = A.B$$

➤ Logic Diagram:



➤ Full Adder:

A **full adder** adds binary numbers and accounts for values carried in as well as out. A one-bit full adder adds three one-bit numbers, often written as A, B, and C_{in} ; A and B are the operands, and C_{in} is a bit carried in (in theory from a past addition). The circuit produces a two-bit output sum typically represented by the signals C_{out} and S, where $sum = 2 \times C_{out} + S$. The one-bit full adder's truth table is:

➤ Truth Table:

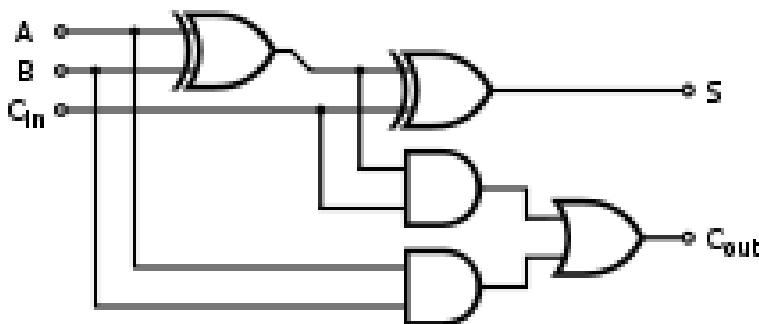
input			output	
A	B	C_{in}	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

➤ Logic Function:

$$S = A \text{ xor } B \text{ xor } C_{in}.$$

$$C_{out} = A.B + A.C_{in} + B.C_{in} = (A \text{ xor } B).C_{in} + A.C_{in}$$

➤ Logic Diagram:



➤ **Half subtractor :**

The **half-subtractor** is a combinational circuit which is used to perform subtraction of two bits. It has two inputs, X (minuend) and Y (subtrahend) and two outputs D (difference) and B (borrow).

➤ **Truth Table:**

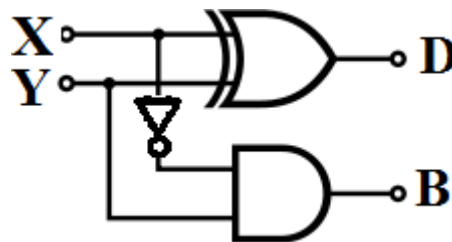
input		Output	
X	Y	D	B
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

➤ **Logic Function:**

➤ $D = X \text{ xor } Y$

➤ $B = X' \cdot Y$

➤ **Logic Diagram:**



➤ **Full subtractor :**

The full-subtractor is a combinational circuit which is used to perform subtraction of three bits. It has three inputs, X (minuend) and Y (subtrahend) and Z (subtrahend) and two outputs D (difference) and B (borrow).

➤ **Truth Table:**

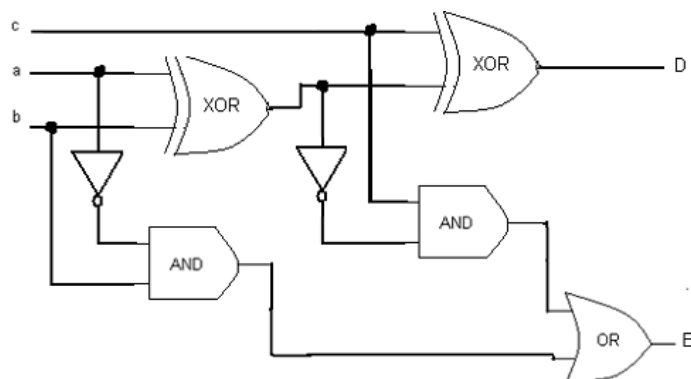
input			output	
X	Y	Z	D	B
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

➤ **Logic Function:**

➤ $D = X \oplus Y \oplus Z$

➤ $B = Z \cdot (X \oplus Y) + X \cdot Y$

➤ **Logic Diagram:**



PROCEDURE:

1. Connections are given as per circuit diagram.
2. Logical inputs are given as per circuit diagram.
3. Observe the output and verify the truth table.

CONCLUSION:

Thus ADDER AND SUBTRACTOR are studied. They have studied the half adder, half subtractor, full adder, full subtractor and they have to draw the logic function and logic diagram in verify by experimental to the truth table in the logic gates.