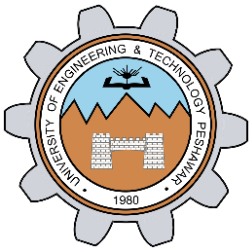
DLD

LAB # 12



Fall 2020

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Class Section: **C**

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"On my honor, as student of University of Engineering and Technology, I have neither given nor received unauthorized assistance on this academic work."

Student Signature: _____

Submitted to:

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DEPARTMENT OF COMPUTER SYSTEMS ENGINEERING

SYNCHRONOUS COUNTERS

OBJECTIVES:

After completing this experiment, you will be able to:

1. Analyze the count sequence of a synchronous counter.
2. To design and implement 3 bit synchronous up/down counter.

EQUIPMENT:

- Dc power supply
- Breadboard

COMPONENTS:

- IC 7486 quad 2-input XOR gate
- IC 7476 JK FLIP FLOP
- LEDs
- Clock
- Wires
- IC 7411 quad 3-input AND gate
- IC 7432 quad 2-input OR gate
- IC 7404 NOT gate

THEORY:

A counter is a register capable of counting number of clock pulse arriving at its clock input. Counter represents the number of clock pulses arrived.
Synchronous counters have all clock lines tied to a common clock, causing all flip-flops to change at the same time. For this reason, the time from the clock pulse until the next count transition is much faster than in a ripple counter. This greater speed reduces the problem of

glitches (short, unwanted signals due to non-synchronous transitions) in the decoded outputs. However, glitches are not always eliminated, because stages with slightly different propagation delays can still have short intermediate states.

An up/down counter is one that is capable of progressing in increasing order or decreasing order through a certain sequence. An up/down counter is also called bidirectional counter. Usually up/down operation of the counter is controlled by up/down signal. When this signal is high counter goes through up sequence and when up/down signal is low counter follows reverse sequence.

What is a Counter?

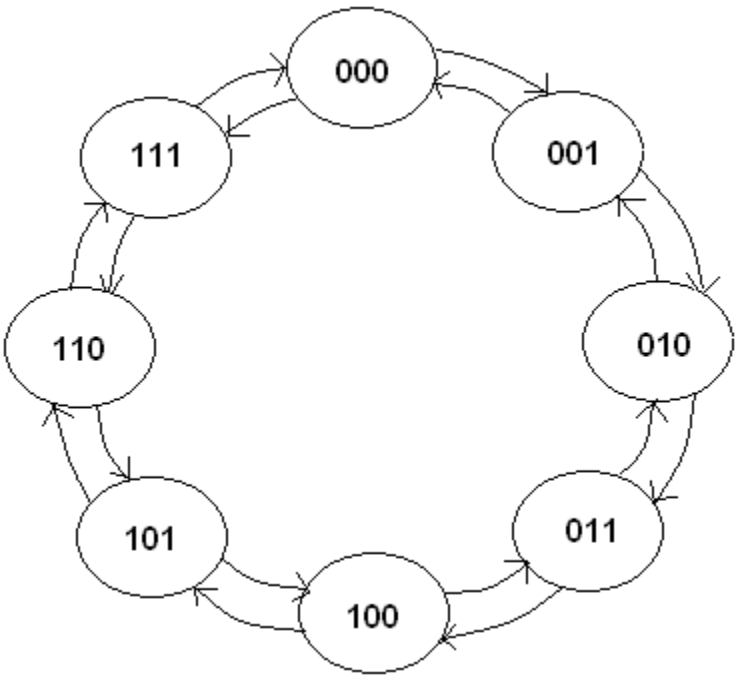
A counter is a device which can count any particular event on the basis of how many times the particular event(s) is occurred. In a digital logic system or computers, this counter can count and store the number of time any particular event or process have occurred, depending on a clock signal. Most common type of counter is sequential digital logic circuit with a single clock input and multiple outputs. The outputs represent binary or binary coded decimal numbers. Each clock pulse either increase the number or decrease the number.

Synchronous Counter:

Synchronous generally refers to something which is cordinated with others based on time. Synchronous signals occur at same clock rate and all the clocks follow the same reference clock.

In previous tutorial of Asynchronous Counter, we have seen that the output of that counter is directly connected to the input of next subsequent counter and making a chain system, and due to this chain system propagation delay appears during counting stage and create counting delays. In synchronous counter, the clock input across all the flip-flops use the same source and create the same clock signal at the same time. So, a counter which is using the same clock signal from the same source at the same time is called Synchronous counter.

STATE DIAGRAM:



CHARACTERISTICS TABLE:

Q	Qt+1	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

K MAP:

UD QA \ QB QC	00	01	11	10
00	1	0	0	0
01	X	X	X	X
11	X	X	X	X
10	0	0	1	0

$JA = \overline{UD}\ \overline{QB}\ \overline{QC} + UD\ QB\ QC$

UD QA \ QB QC	00	01	11	10
00	X	X	X	X
01	1	0	0	0
11	0	0	1	0
10	X	X	X	X

$KA = \overline{UD}\ \overline{QB}\ \overline{QC} + UD\ QB\ QC$

UD QA \ QB QC	00	01	11	10
00	1	X	X	1
01	1	X	X	1
11	1	X	X	1
10	1	X	X	1

$JC = 1$

UD QA \ QB QC	00	01	11	10
00	1	0	X	X
01	1	0	X	X
11	0	1	X	X
10	0	1	X	X

$JB = \overline{UD \oplus QC}$

UD QA \ QB QC	00	01	11	10
00	X	X	0	1
01	X	X	0	1
11	X	X	1	0
10	X	X	1	0

$KB = (UD \oplus QC)$

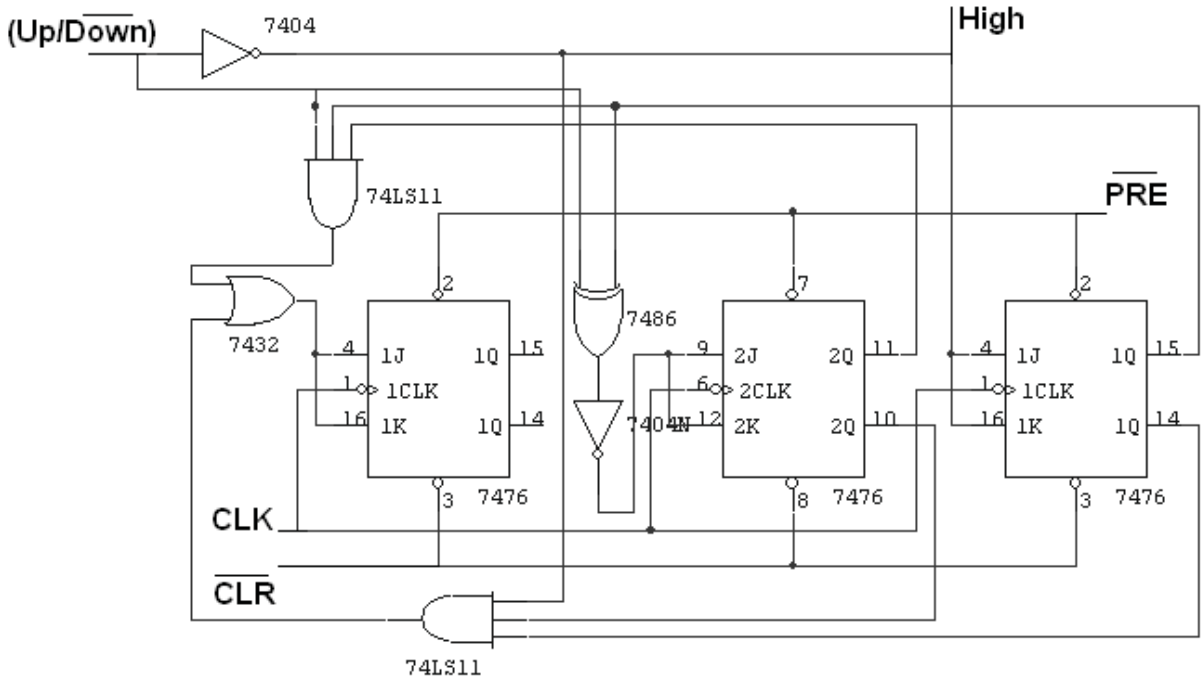
UD QA \ QB QC	00	01	11	10
00	X	1	1	X
01	X	1	1	X
11	X	1	1	X
10	X	1	1	X

$KC = 1$

TRUTH TABLE:

Input Up/Down	Present State Q_A Q_B Q_C			Next State Q_{A+1} Q_{B+1} Q_{C+1}			A J_A	A K_A	B J_B	B K_B	C J_C	C K_C
0	0	0	0	1	1	1	1	X	1	X	1	X
0	1	1	1	1	1	0	X	0	X	0	X	1
0	1	1	0	1	0	1	X	0	X	1	1	X
0	1	0	1	1	0	0	X	0	0	X	X	1
0	1	0	0	0	1	1	X	1	1	X	1	X
0	0	1	1	0	1	0	0	X	X	0	X	1
0	0	1	0	0	0	1	0	X	X	1	1	X
0	0	0	1	0	0	0	0	X	0	X	X	1
1	0	0	0	0	0	1	0	X	0	X	1	X
1	0	0	1	0	1	0	0	X	1	X	X	1
1	0	1	0	0	1	1	0	X	X	0	1	X
1	0	1	1	1	0	0	1	X	X	1	X	1
1	1	0	0	1	0	1	X	0	0	X	1	X
1	1	0	1	1	1	0	X	0	1	X	X	1
1	1	1	0	1	1	1	X	0	X	0	1	X
1	1	1	1	0	0	0	X	1	X	1	X	1

LOGIC DIAGRAM:



PROCEDURE:

1. Connections are given as per circuit diagram.
2. Logical inputs are given as per circuit diagram.
3. Observe the output and verify the truth table.

Advantages and Disadvantage of Synchronous Counter:

Now we are familiar with Synchronous counter and what are the difference between the Asynchronous counter and Synchronous counter. Synchronous counter eliminates lots of limitations which arrive in Asynchronous counter.

The advantages of the Synchronous counter is as follows-

1. It's easier to design than the Asynchronous counter.
2. It acts simultaneously.

3. No propagation delay associated with it.
4. Count sequence is controlled using logic gates, error chances are lower.
5. Faster operation than the Asynchronous counter.

Although there are many advantages, one major disadvantage of working with Synchronous counter is that it requires a lot of extra logic to perform.

CONCLUSION:

Thus the Synchronous counters are studied. We can create 3 bit Synchronous counter by using logic gates and flip flop. We also verify the truth table of these counters.

REVIEW QUESTIONS:

1) What is the difference between asynchronous and synchronous counters? Which counter will you prefer to use in your circuits and why? Also specify the main drawbacks of asynchronous counters.

ANS:

Difference between asynchronous and synchronous counters:

	Synchronous Counter	Asynchronous Counter
1.	In synchronous counter, all flip flops are triggered with same clock simultaneously.	In asynchronous counter, different flip flops are triggered with different clock, not simultaneously.
2.	Synchronous Counter is faster than asynchronous counter in operation.	Asynchronous Counter is slower than synchronous counter in operation.
3.	Synchronous Counter does not produce any decoding errors.	Asynchronous Counter produces decoding error.

4.	Synchronous Counter is also called Parallel Counter.	Asynchronous Counter is also called Serial Counter.
5.	Synchronous Counter designing as well implementation are complex due to increasing the number of states.	Asynchronous Counter designing as well as implementation is very easy.
6.	Synchronous Counter will operate in any desired count sequence.	Asynchronous Counter will oper ate only in fixed count sequence (UP/DOWN).

We can prefer to synchronous counter because **Synchronous counters** are easier to design than **asynchronous counters**. are all clocked together at the same time with the same clock signal. Due to this common clock pulse all output states switch or change simultaneously. ... Overall faster operation may be achieved compared to **Asynchronous counters**.

The asynchronous counters are also called **ripple** counters because the new **count ripples** through them. The major **disadvantage of ripple** counters is that because of new **count** "rippling" through the flip flops all the bits of the **count** arrive at different times.