CENTER OF NANOELECTRONICS & DEVICES

# CND 212: Digital Testing and Verification

## Assignment #: 3

## Section #: 16

**Submitted by:**


| Student Name | ID |
|---|---|
| Fayza Ahmed Sayed Ahmed | V23010517 |
| Eslam Hussien Ahmed Solyman | V23010203 |
| Omar Mohamed Sabaan | V23010277 |
| Youssef Ahmed Hassan | V23009895 |


**Submitted to TA: Eng. Rana Badran**

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Q1. Write a SystemVerilog assertion to check if a signal valid is high whenever a signal ready is high.

Answer:

```
property p;
  @(posedge clk) (ready) |-> (valid);
endproperty
assert property (p);
```

Another Answer: **assert property ( @(posedge clk) disable iff (rst_n) $rose(ready) |-> ##1 valid);**

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Q2. Write a SystemVerilog assertion to check if a sequence of events a, b, and c occurs in the given order with a one-cycle gap between each event. Ensure that the sequence does not trigger if the reset signal is active.

Answer: **assert property ( @(posedge clk) disable iff (rst_n) (a |-> ##1 b ##1 c));**

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Q3. Write a SystemVerilog cover directive to measure the coverage of a signal data being greater than zero.

Answer: **cover property (@(posedge clk) data > 0);**

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Q4. Write a SystemVerilog sequence that checks if a signal a is high for at least two clock cycles, followed by a sequence of events b and c, and assert it.

Answer:

```
sequence seq1;
   a ##1 a ##1 b ##1 c;
endsequence
assert property (@(posedge clk) disable iff (rst_n) seq1) else $error("Sequence seq1
violated!");
```

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Q5. Write a SystemVerilog sequence, s1, that checks for the following pattern in a signal sequence:

- The sequence should start with a rising edge of a signal called data_valid.
- The sequence should then wait for a delay of 7 clock cycles.
- After the delay, the signal data_out should be equal to the value stored in data_in before the delay.

Answer:

```
sequence s1;
  @(posedge data_valid) ##7 (data_out == $past(data_in, 7));
endsequence
property p;
  s1;
endproperty
assert property (p);
```

Q6. Consider the following SystemVerilog sequence: **S1 ##2 S2[=1:2] ##1 S3 ##1 S4[->1:3] ##1 S5.** Your task is to analyze the given sequence and identify the conditions that will result in the sequence succeeding or failing. Write a comprehensive explanation that includes:

• The conditions under which the sequence will succeed.

• The conditions that will cause the sequence to fail.

• Provide specific examples for both success and failure cases to demonstrate your understanding

| **Conditions for Sequence Success:** | **Conditions for Sequence Failure:** |
|---|---|
| The sequence will succeed under the following conditions:<br>• S1 occurs, followed by exactly 2 clock cycles, then S2 occurs 1 or 2 times, followed by S3, then S4 occurs 1 to 3 times, and finally S5 occurs. | The sequence will fail under the following conditions: If any of the specified events in the sequence ***does not*** occur in the defined order and timing, the sequence will fail. |
| **Success Case Example:**<br>• S1 occurs at time t1.<br>• After 2 clock cycles, S2 occurs at time t3.<br>• Then, S3 occurs at time t4.<br>• Following that, S4 occurs at time t5, t6, or t7.<br>• Finally, S5 occurs at time t8. | **Failure Case Example:**<br>• S1 occurs at time t1.<br>• After 2 clock cycles, S2 does not occur.<br>• This leads to the failure of the sequence as S2 did not occur within the specified timing after S1. |