2 December 2019 5 ربيع الثاني 1441

وَمَا أُوتِيتُم مِّنَ الْعِلْمِ إِلَّا قَلِيلًا

Ain Shams University – Faculty of Engineering – ECE Dept. – Integrated Circuits Lab.
Dr. Hesham Omran

Digital Design and Computer Architecture (DDCA)
Lab 03
Design of Single-Cycle RISC-V Processor

Objectives

1. Design a single-cycle processor datapath and control logic.
2. Acquire a deep understanding of the operation of a single-cycle processor.
3. Design and verify a complex digital system using HDL.
4. Run and debug logic simulations.

Submission and Peer-Grading Instructions

1. **DO NOT WRITE YOUR NAME ON YOUR SUBMITTED WORK. YOUR SUBMISSION WILL BE GRADED ANONYMOUSLY.**
2. Submit your solution on Canvas as a single zip file that contains all the deliverables.
3. You may discuss the questions together, but you are NOT allowed to share the answers.
4. If you cheat, attempt to cheat, or help someone else to cheat you will get ZERO marks.
5. Remember: قال رسول الله صلى الله عليه وسلم: من غش فليس منا
6. You will be invited to review three anonymous submissions after the due date.
7. You must complete the reviews within one week of the deadline. You must be fair and justify the grade you give in detail. Give the grade (for every deliverable) and justify it as a comment on Canvas. Do NOT attach extra files for your grading.
8. **If you do not complete the grading (with clear justifications) within one week of the deadline, 20% of the full mark will be deducted from your mark.**
9. **10% of the full mark will be deducted for every late day after the deadline (in addition to losing the peer-review marks).**
10. دعواتي لك بالتوفيق

Lab Instructions

1. Use VHDL or Verilog to write your code.
2. Your processor should implement the following subset of RV32I instruction set:
   a. R-Type: add, sub, and, or
   b. I-Type: addi, andi, ori, lw, jalr
   c. B-Type: beq, bne
   d. J-Type: jal
   e. S-Type: sw
3. Assume instruction/data memory access has 100 ps delay. Assume any other major stage in the datapath has 50 ps delay. Assume 10 ps delay for simple logic stages.
4. Use 1 ns clock period in your testbench.
5. Note that reading register-file/memory data is combinational, but writing is clocked.
6. The top module should be divided into two main modules: datapath and control logic. The instruction and data memories should be connected to the top module in the testbench.
7. For simplicity, assume that the instruction memory is a 1kB word-addressable ROM and the data memory is a 1kB word-addressable RAM, i.e., you will only connect bits 9 to 2 in the address bus.

Note that practically the instruction and data memories are not implemented using RTL code. What you build here is a behavioral model that is merely used for verification.

Deliverables

Index	Deliverable	Points
1.	Report all your HDL modules. **Hint: Read Section 7.6 in the textbook (DDCA 2nd edition by Harris and Harris) as it will be a good starting point.**	4
2.	Use Venus to generate the machine code for a Fibonacci sequence program. Load the machine code in your instruction memory. Simulate the processor to calculate the 6th Fibonacci number (= 8). Report your assembly code. Report your testbench. Report your simulation results clearly. **Hint: Read Section 7.6.3 in the textbook (DDCA 2nd edition by Harris and Harris).**	3
3.	Use Venus to generate the machine code for an arbitrary sample program. The program should exercise all the instructions you implemented (you may extend the Fibonacci sequence program). Report your assembly code. Report your testbench. Report your simulation results clearly.	3

Reference

Harris D and Harris S, Digital design and computer architecture, Morgan Kaufmann, 2nd ed., 2012.

Thanks to all who contributed to these labs. If you find any errors or have suggestions concerning these labs, please contact Hesham.omran@eng.asu.edu.eg.