

Wynn Kaza

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Education

University of Michigan, Ann Arbor, MI

Fall 2024 - Winter 2025

Major: Masters of Engineering in Computer Science and Engineering

University of Michigan, Ann Arbor, MI

Graduation May 2024

Major: Bachelors of Engineering in Computer Engineering

GPA: 3.965 (Undergraduate)

Classes: Parallel Computing, Parallel Computing Architecture, Operating System, Computer Networks, Advanced Compilers, Computer Architecture, Data Structures & Algorithms,, Computer Organization, Digitally Integrated Circuits

Relevant Experiences

IBM

Rochester, MN

Hardware Engineering Intern: Z&Cognitive Systems

May 2023 - Aug 2023

- Revamped backend database infrastructure by transitioning from sqlite3 to MariaDB using C++, improving data security and the department's ability to handle increased test data volume and multiple users.
- Designed Arduino Nano 33 BLE PCB shield and wrote API C++/Python library to interface between tester and computer
- Refactored C++ code for vpd tools, increasing speed for future development and simplifying cross-platform compilation

Whisker

Rochester Hills, MI

Electrical Engineering Intern

May 2022 - Aug 2022

- Developed a solution for Company's Main Board Test Fixture, resolving an critical issue with the ESP-Programmer burning out when programming the main board
- Constructed multiple R&D based PCBs in Altium for different parts of the design process, encapsulating breakout boards for ESP-Programmers, ToF Sensors, Stepper Motor Driver, and more
- Built two test fixtures to test design changes on LR4 Main Board and ToF Board, confirming effect of board changes

Projects / Experiences

Instructional Aid

January 2024 - May 2024

- Instructed ENGR 100-250, An Introduction to Computing Systems with 70+ freshmen
- Taught weekly lab sessions, engaging students in learning Verilog and applying them to develop a single-cycle datapath processor on a FPGA, alongside building device drivers to interact with IO devices in assembly

R10K Inspired Out-of-Order Processor : RISC-V

October 2023 - December 2023

- Design and implemented N-Way Superscalar OoO processor with early branch resolution using SystemVerilog
- Developed Pag branch predictor, non-blocking D-Cache, victim cache, and store queue to improve CPI
- Synthesized design obtained 12.06 ns clock period with a 1.87 CPI average on test bench

Cache Tiling and Tile Size Selection Algorithms

October 2023 - December 2023

- Wrote LLVM pass to replicate cache tiling to reduce number of cache misses in matrix multiplication
- Improved upon original tiling algorithm by reducing instruction overhead (specifically branches)
- Developed two new algorithms to find optimal tiling size within the new restrictions: implemented algorithms obtained 58.56% and 84.37% less cache miss than the original untilted matrix multiplication

Undergraduate Researcher : Systems

Feb 2023 - Current

- Characterized workload, efficiency, and weight distribution of graph mining algorithm running on various thread counts, CPU, and GPU using ScoreP and Vampir (Paper: Everest gpu-accelerated-system-for-mining)

MASA : Avionics Team

Aug 2022 - Current

- Implemented run-length encoding compression algorithm in GO, reducing data sent to the server by 8-13x
- Implemented Json compression algorithm, removing current client to server bottleneck from sending database frames as Json, having an average of 10x encoding speedup, 5x reduced memory, and 3x less heap allocations
- Worked on debugging firmware/hardware issues to fix communication errors with SPI, I2C, and cross-talk

Technical Skills

Hardware Engineering: SystemVerilog, Verilog, C, ARM, Assembly, FPGA, Ubuntu, Altium/Allegro, Virtuoso

Software Engineering: C++, Python, GoLang, Bash, OpenMP, Cuda, LLVM, Javascript, SQL, Version Control (Git/Github)