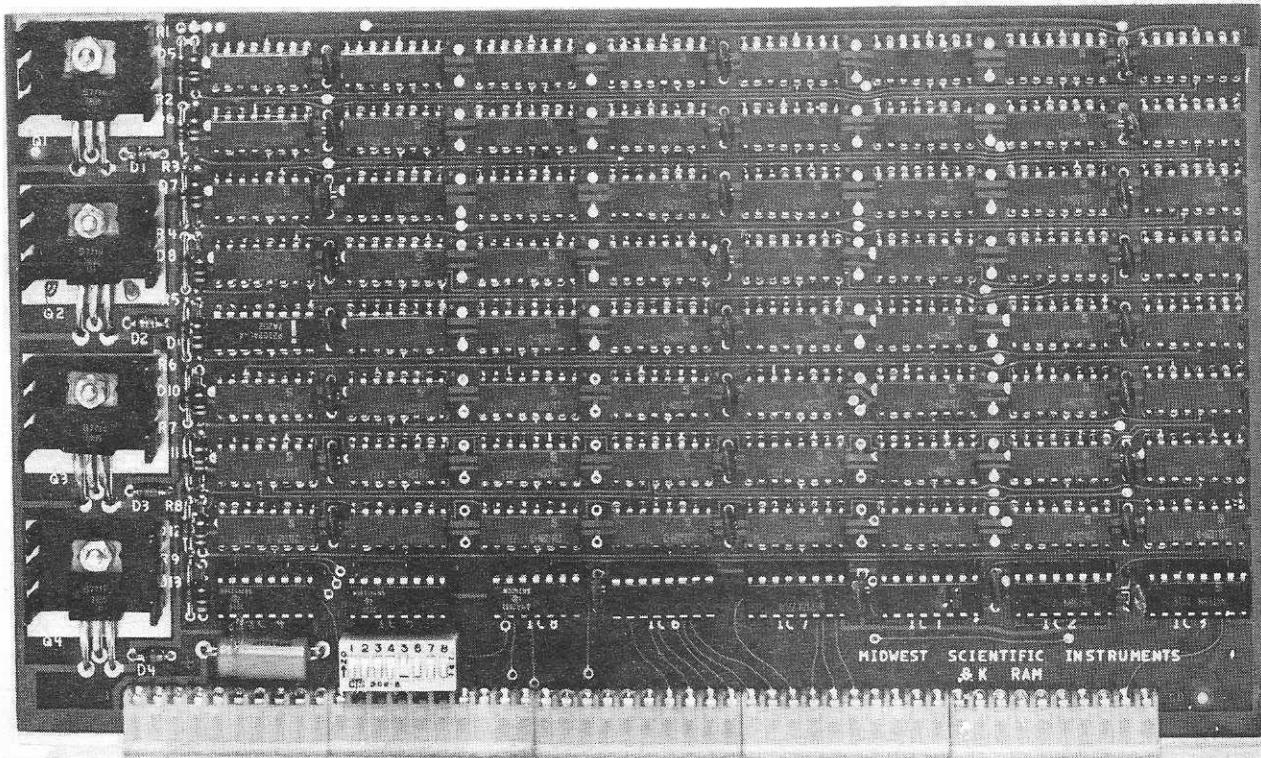


8K RAM BOARD

Model RAM-68



*Midwest Scientific Instruments, Inc.
Olathe, Kansas*

THE MSI 8K RAM BOARD, MODEL RAM-68

GENERAL DESCRIPTION

The MSI Model RAM-68 is an 8K Memory Board which is designed to be compatible with the SS-50 bus architecture employed by the MSI 6800 or SWTP 6800 Computer Systems. The board contains 8,192 eight-bit bytes of fully buffered static memory, having an access time of 450 ns. The base address of the board is switch selectable and can be set to begin at any desired 8K increment of memory from 0 to 64K. A convenient DIP switch assembly on the board has eight toggle switches. Only one of the toggle switches may be in the "ON" position at a given time. The remaining seven must be turned "OFF". The Table below indicates the appropriate switch settings in order to address the desired memory segment.

MEMORY SEGMENT	SWITCH SETTINGS							
	1	2	3	4	5	6	7	8
0000 - 1FFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON
2000 - 3FFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF
4000 - 5FFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF
6000 - 7FFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF
8000 - 9FFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF
A000 - BFFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF
C000 - DFFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF
E000 - FFFF	ON	OFF						

NOTE: Switch must be mounted as shown in Figure 1 below:

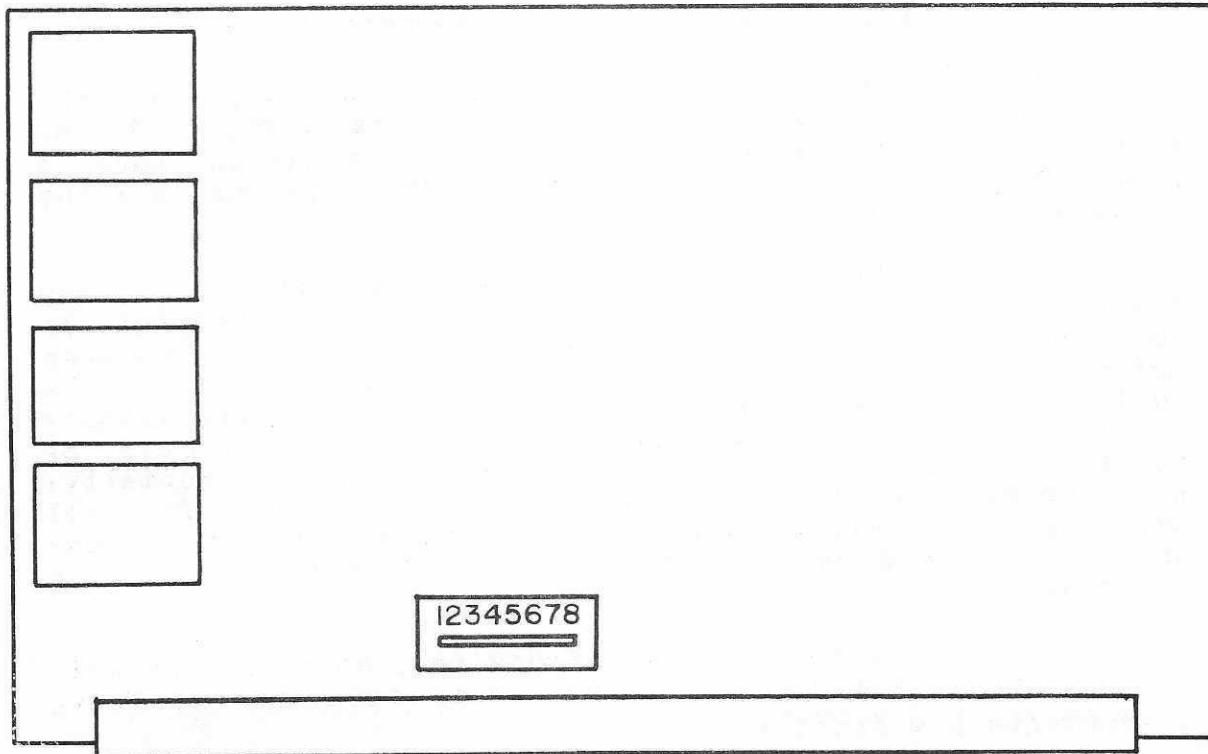


Figure 1

A network of diodes and pull-up resistors is included so that back up Vcc may be supplied from a battery pack, if desired. This network insures that Vcc remains applied to all memory chips and that the chip select lines are also held in a high state so as to prevent loss of memory during a power failure. Refer to the Schematic Diagram and Assembly Drawing for the correct polarity of the battery connections. Four on-board 7805 regulator chips supply Vcc to the board. The bus must carry an unregulated supply of approximately +8V in order to power the board.

THEORY OF OPERATION

Address lines are brought to the RAM chips through buffer packages IC6 and IC7. These are non-inverting buffers (8T97) which remain permanently enabled at all times. The address lines are active high. Decoder package IC5 (74S138) is used to decode the three highest order address bits along with the valid memory address signal (VMA) and Phase 2 clock. The output of this decoder is fed to the DIP switch assembly in order to select the desired memory segment. The output of this decoder is, in turn, used to enable IC4 which decodes the lower order address lines in order to select a 1K memory segment on the board. The chip select outputs from decoder IC4 (74S138) are pulled up through a resistor and diode network to the standby Vcc power supply, if used. This network insures that the chip select lines remain high via the battery power supply during power failure.

P.C. BOARD ASSEMBLY INSTRUCTIONS

Before beginning assembly of the PC board, perform the following steps. Referring to the parts list, and the Assembly Drawing, carefully check the parts kit in order to properly identify each component and make sure that all the necessary parts are included.

Next, carefully examine the P.C. Board itself for any flaws or defects. A magnifying glass is helpful in identifying the presence of any hairline shorts between foils, incomplete etching of the board or breaks in the foil. Such defects are rare but a careful preliminary examination is very worthwhile. Any defects should be corrected before beginning assembly of the board. Normally, we recommend using a 30 watt soldering iron for all assembly. Use only solder having a resin core, never use any type of acid based solders. A 60/40 or 63/37 alloy is recommended.

I.C. sockets may be used if desired, however, use only the highest quality sockets available, such as the Texas Instruments Low Profile.

Note that the unmarked I.C. symbols on the PC Board

are the locations of the 2102 memory chips. Also note that the assembly drawing shows more .01 bypass capacitors than are shown on the PC Board silk screen. The extra capacitors have been included.

The PC board has been silk screened to show the proper placement of all components. Refer also to the Assembly Drawing for correct placement and orientation of all components. Refer also to the RAM-68 Schematic Diagram, Drawing No. 100040, for the wiring configuration.

Data lines are buffered bi-directionally using integrated circuits IC1, IC2, and IC3 (8T98) which are tri-state bus driver packages. Appropriate segments of these packages are enabled depending upon whether a read or write operation is taking place.

The memory chips used in the RAM-68 Board are low-power 2102 static RAMs having an access time of less than 500 ns.

ASSEMBLY PROCEDURE

() Install the four 7805 voltage regulators in positions Q1, Q2, Q3, and Q4. Place a heatsink under each of the regulators. Use 4-40 x 3/8 BHMS, #4 lock washers, and hexnuts which have been provided.

() Install the five 10 pin female Molex connectors on the bottom edge of the PC Board. The body of the connector lies on the component side of the circuit board. The connector should be held firmly in position, with the body of the connector lying flat against the circuit board and pushed tightly against the edge of the circuit board, during soldering. First solder only the end pins of each connector. This procedure will insure correct alignment of the connectors. After soldering the end pins, the remaining pins of each connector may be soldered.

() Insert the small plastic keying pin into the index position of the bottom edge connector. This will prevent the PC Board from being accidentally plugged in backwards or with the pins offset.

() Install resistors R1 thru R9 into their appropriate positions on the PC Board. Solder.

() Install the capacitor C1 in its appropriate position on the circuit board. Be careful to observe the polarity of this electrolytic capacitor during installation to insure that it is oriented correctly.

() Install the 8 position DIP switch on the PC Board. Solder. The switch should be installed in an upright position so that the numbers will correspond with the address selection Table shown above.

() Install diodes D1 thru D13 into their appropriate positions on the PC Board. Be careful to observe the banded end of the diode during installation to insure that each diode is oriented properly. Solder.

() Install IC1 thru IC8 in their proper positions along the bottom of the PC Board. Be careful to orient the ICs correctly with respect to Pin 1. Solder.

() Install the 2102 memory chips in positions IC9 thru IC72. Solder.

() Install capacitors C2 thru C61 in their appropriate positions on the PC Board. These are bypass capacitors, which are located between the +5 Volt bus and ground throughout the PC Board.

() Upon completion of the PC Board assembly, carefully examine the board for the presence of any solder splashes, solder bridges, or shorts between adjacent pads on the board. These must be carefully removed before proceeding with checkout of the board. A magnifying glass greatly aids in the detection of such defects. If available, excess flux may be removed from the board with trichlorethylene. This also makes defects much easier to locate.

MEMORY BOARD CHECKOUT PROCEDURE

() Following careful examination of the PC Board, place the board into the computer system and apply power. The computer system should respond normally with the asterisk (*) prompt character. If the board prevents this response, then remove power from the system and examine the board for the presence of shorts or other defects on the address, data, or other lines which communicate with the computer bus.

() Using a voltmeter, or an oscilloscope if available, determine that the output of each of the 7805 voltage regulators is +5 V.D.C. and is free of any ripple.

() Perform the memory diagnostic program listed below.

MEMORY CHECKOUT PROCEDURES

INTRODUCTION

The execution of the following memory diagnostic program is essential following assembly of any memory board. Don't be misled by the various memory diagnostic programs, which are in circulation for 6800 systems, since most of these programs are very inadequate and fail to reveal memory problems in many cases. The program presented herein is the best that we have seen and will detect almost any memory problem which we have encountered thus far. The code can

be relocated easily and can be used on EPROM which is highly recommended for quick availability. This program is a part of the MSI Extended Monitor EPROM.

To execute the program, place the beginning address of the memory area to be tested in memory locations \$F002-\$F003 (Monitor RAM area). The ending memory location+1 is placed in memory locations \$F004-\$F005. Then execute the program at its beginning address. Be careful not to test the memory area which contains the MEMORY TEST program itself, or it will be wiped out.

If memory location \$F020 contains a \$00, then the program will print a "@" after each 256 passes through memory. If \$F020 is not \$00, then a "+" will be printed following each pass through memory. This is the most desireable for a quick check.

When memory defects are detected, the bad address, expected data, and actual data read back are printed on the terminal.

TYPES OF MEMORY PROBLEMS

If a single bit remains set, or fails to set, within a 1 K segment of memory, then a single defective 2102 memory chip almost certainly is at fault. Refer to the schematics on the RAM-68 memory board in order to locate the bad chip.

If a single bit remains set, or fails to set, throughout all addresses on the memory board, then look for a more general problem with that particular data line or data bus driver package.

If the memory fails in a repetitive pattern through the board then look for a memory addressing problem, such as a shorted address line or a defective address buffer package.

Memory failures, not caused by bad memory chips, usually manifest themselves as one or more bits responding to multiple addresses. Locating such faults is relatively simple if the memory test first detects a failing location.

First zero memory as shown in example 1. Then examine the defective location and verify that the contents are actually zero. Write an \$FF into the defective location(s) then check to see what other locations were simultaneously altered.

Consider the following possibilities:

1. Data going high changes the address by raising an address line high that should have remained low (data line shorted to address line).

2. Two address lines shorted. All bits in the address less than those shorted will have common data. Cause the processor to execute a \$9D instruction and observe the address lines on the 2102 chips to see if they toggle in the correct relationship to each other.

3. Data bits alternately high and low usually indicate that the data line is actually displaying one bit of the address (data line and address line shorted together).

MSI WARRANTY POLICY

MSI warrants all equipment and materials to be free from defective workmanship and material for a period of 90 days beyond the date of purchase from either MSI directly or an authorized MSI dealer. Activation of product warranty must be by the return of the warranty registration card.

During the warranty period, any products purchased as wired and tested units will be repaired or replaced, at MSI's sole option, free of charge, when shipped to MSI prepaid, accompanied by a complete written description of the defect and a return authorization number, as long as the product has not been subjected to electrical or mechanical abuse, in the opinion of MSI. MSI accepts no responsibility for equipment returned freight collect, without a return authorization number, or without a written description of the defect.

During the warranty period, any products purchased in kit form will be repaired or replaced, at MSI's sole option, free of any charge for parts. However, labor charges for the repair will be assessed on a time required basis. MSI reserves the right to reject any product as not repairable if in our opinion it has been subjected to accident, abuse, or improper assembly procedures. Upon completion of repairs, the product will be returned to the customer collect.

MSI 6800 COMPUTER, 8K-RAM BOARD

PARTS LIST

<u>ITEM NO.</u>	<u>QUANTITY</u>	<u>DESCRIPTION</u>	<u>REFERENCE DESIGNATION</u>	<u>MSI PART NO.</u>
1	1	PCB, RAM-68, 8K RAM		967
3	9	RESISTOR, 6.8K, +10%, 1/4W	R1 thru R9	030
5	60	CAP., Disc., .01uf, 25V	C2 thru C60	156
6	C1	CAP., Electro., 25uf, 25V	C1	177
8	13	DIODE, 1N4003	D1 thru D13	102
10	64	IC, 21L02	IC9 thru IC72	414
11	1	IC, 7400	IC8	201
12	2	IC, 74S138	IC4, IC5	339
13	2	IC, 8T97	IC6, IC7	420
14	3	IC, 8T98	IC1, IC2, IC3	419
16	4	IC, 7805, +5V Regulator	Q1 thru Q4	495
18	1	SWITCH, 8-SPST, DIP	SWITCH	844
20	5	CONNECTOR, 10 Pin, F.G.		1043
21	1	KEYING PIN, Molex		1051
23	4	SCREW, 4-40 x 3/8", B.H.M.		716
24	4	NUT, 4-40, Hex		714
25	4	WASHER, #4, I.T.L.		744
26	4	HEATSINK		1822

0030 *
0040 *
0050 * THIS ALGORITHM ORIGINALLY WRITTEN BY CHARLES MC COLLOUGH
0060 * RE-WRITTEN AND EXPANDED BY EDGAR R. ALLEN
0070 * THIS VERSION WRITTEN 1/20/78
0080 *
0090 * MOST MEMORY TESTS EITHER DEAL WITH A SINGLE
0100 * LOCATION ONLY, WHICH WILL NOT FIND BITS RESPONDING TO
0110 * MORE THAN ONE ADDRESS OR THEY FILL MEMORY WITH A BYTE
0120 * THEN CHANGE BITS IN THE TEST LOCATION THEN VERIFY THAT
0130 * NO OTHERS HAVE BEEN ALTERED. THE FIRST IS TOTALLY
0140 * INADEQUATE AND THE SECOND HAS AN EXPONENTIAL INCREASE
0150 * RATE. THIS MEANS THAT TESTING TWICE AS MUCH MEMORY
0160 * TAKES FOUR TIMES AS LONG. WE FEEL THIS IS UNACCEPTABLE
0170 * WITH TODAYS LARGER MEMORY SIZES.
0180 *
0190 * THIS PROGRAM GENERATES A PATTERN DEPENDENT UPON A
0200 * SEED BYTE AND THE PLACEMENT OF THE CURRENT TEST LOC-
0210 * ATION. THEN THE SAME PATTERN IS GENERATED WITHIN
0220 * THE REGISTERS AND COMPARED TO THE DATA IN MEMORY.
0230 * IF THE EXPECTED AND ACTUAL DATA AGREE THEN THE NEXT
0240 * LOCATION IS EXAMINED. OTHERWISE THE FAILING ADDRESS,
0250 * THE FAILING BITS, THE EXPECTED DATA AND THE ACTUAL
0260 * DATA ARE PRINTED. THE EXPECTED AND ACTUAL DATA MAY AGREE,
0270 * THIS PROBABLY MEANS THAT THE MEMORY IS TOO SLOW. THIS
0280 * MAKES THE PRINT OF THE FAILED BITS QUITE HANDY.
0290 *
0300 * THE WAY THE DATA IS GENERATED IS BY EXCLUSEIVE-
0310 * ORING THE LOW AND HIGH BYTES OF THE COUNTER
0320 * WITH THE SEED. THIS COUNTER IS THEN INCREMENTED FOR
0330 * THE NEXT LOCATION. AFTER ALL LOCATIONS HAVE BEEN
0340 * FILLED THEY ARE COMPARED TO THE SAME DATA GENERATED
0350 * IN THE SAME WAY. THE SEED IS THEN INCREMENTED AND
0360 * ANOTHER PASS IS MADE. AFTER ALL COMBINATIONS OF THE
0370 * SEED HAVE BEEN TRIED THE COUNTER IN 'SAVEX' IS
0380 * INCREMENTED AND USED AS THE START OF ANOTHER 259 PASSES
0390 * OR ONE GROUP. THIS REMOVES ONE BYTE FROM THE FRONT OF THE
0400 * SERIES AND ADDS A NEW BYTE TO THE BACK. THIS HAS THE
0410 * EFFECT OF SHIFTING THE PATTERN OVER ONE ADDRESS
0420 * MEANING THE TRANSITIONS FROM ONE STATE TO THE OTHER
0430 * OF EACH BIT ALSO MOVES. THE TEST WILL DETECT ERRORS
0440 * WHEN THE FAILING BITS ATTEMPT TO MAKE A TRANSITION
0450 * BETWEEN THE TWO, OR MORE, ADDRESSES WHICH AFFECT
0460 * EACH OTHER.
0470 *
0480 * THIS PROGRAM USES MSIBUG SCRATCHPAD RAM
0490 * LOCATIONS. THE PROGRAM ITSELF IS FULLY RELOCATABLE.
0500 *
0510 * TO RUN THE MEMORY TEST, PUT THE BEGINNING ADDRESS +1
0520 * TO CHECK IN \$F002 & \$F203 AND THE END ADDRESS +1
0530 * IN \$F004 & \$F005. GO AT +0 INTO THE PROGRAM WHICH IS
0540 * \$2000 IN THIS EXAMPLE. THE GROUP NUMBER IS PRINTED
0550 * AFTER 256 PASSES THROUGH MEMORY. IF \$F020 IS NON-ZERO
0560 * A + IS PRINTED AFTER EACH PASS. WHEN AN ERROR OCCURS,
0570 * THE FAILING ADDRESS, THE FAILING BITS, THE EXPECTED
0580 * DATA AND THE ACTUAL DATA ARE PRINTED. TO START THE
0590 * MEMORY TEST ON A PARTICULAR GROUP, CLEAR THE SEED
0600 * (\$F022), PUT THE DESIRED GROUP NUMBER IN \$F025 & \$F027,
0610 * AND GO AT +9 INTO THE PROGRAM WHICH IN THIS EXAMPLE
0620 * IS \$2009.

READY

RAM-1.8

00610 *
 00620 * MIDWEST SCIENTIFIC INSTRUMENTS
 00630 *
 00640 OPT O
 00650 F002 FIRST EQU \$F002
 00660 F004 LAST EQU \$F004
 00670 F022 SEED EQU \$F022
 00680 F024 COUNT EQU \$F024
 00690 F026 GROUP EQU \$F026
 00700 F028 SAVEX EQU \$F028
 00710 2000 ORG \$2000
 00720 2000 7F F022 TOP CLR SEED
 00730 2003 CE 0000 LDX #0000
 00740 2006 FF F026 STX GROUP
 00750 2009 8D 02 TRICKY BSR START *THIS ALLOWS BRA MORE THAN 12
 00760 200B 20 FC BRA TRICKY *BECAUSE THE ADDRESS IS ON
 00770 200D FE F026 START LDX GROUP *THE STACK
 00780 2010 FF F024 STX COUNT
 00790 2013 FE F002 START2 LDX FIRST *THIS PUTS DATA INTO RAM
 00800 2016 B6 F025 SET LDA A COUNT+1
 00810 2019 B8 F024 EOR A COUNT
 00820 201C B8 F022 EOR A SEED
 00830 201F A7 00 STA A 0,X
 00840 2021 7C F025 INC COUNT+1
 00850 2024 26 03 BNE COMP1
 00860 2026 7C E024 INC COUNT
 00870 2029 08 COMP1 INX
 00880 202A BC F004 CPX LAST *STA A BEFORE CPX MEANS LAST
 00890 202D 26 E7 BNE SET *NOT TESTED
 00900 202F FE F026 LDX GROUP *RE-INITIALIZE COUNT
 00910 2032 FF F024 STX COUNT
 00920 2035 FE F002 CHECK LDX FIRST *POINT TO FIRST LOCATION
 00930 2038 B6 F025 TEST LDA A COUNT+1
 00940 203B B8 F024 EOR A COUNT
 00950 203E B8 F022 EOR A SEED
 00960 2041 16 TAB *SAVE THE EXPECTED DATA
 00970 2042 A8 00 EOR A 0,X
 00980 2044 27 21 BEQ CONTIN *IF THEY ARE THE SAME THEY
 00990 2046 37 PSH B *CANCEL
 01000 2047 36 PSH A
 01010 2048 FF F028 STX SAVEX
 01020 204B CE E17D LDX #\$E17D
 01030 204E BD E07E JSR \$E07E
 01040 2051 CF F028 LDX #SAVEX
 01050 2054 BD E0C8 JSR \$E0C8 *PRINT ADDRESS
 01060 2057 30 TSX *POINT TO FAILED BITS
 01070 2058 BD E0CA JSR \$E0CA *OUTPUT 2HEX AND SPACE
 01080 205B BD E0CA JSR \$E0CA *AND AGAIN
 01090 205E 32 PUL A
 01100 205F 32 PUL A
 01110 2060 FE F028 LDX SAVEX *POINT TO ACTUAL DATA
 01120 2063 BD E0CA JSR \$E0CA
 01130 2066 09 DEX *PREPARE FOR CONTIN
 01140 2067 7C F025 CONTIN INC COUNT+1

01150	206A	26	03	BNE	COMP2	
01160	206C	7C	F024	INC	COUNT	
01170	206F	08		INX		
01180	2070	BC	F004	CPX	LAST	
01190	2073	26	C3	BNE	TEST	*GET NEW DATA
01200	2075	7C	F022	NEXT	INC	SEED
01210	2078	26	0D	BNE	LOOP	*NEW SEED FOR NEXT PASS
01220	207A	FE	F026	LDX	GROUP	
01230	207D	08		INX		*NEXT GROUP
01240	207E	FF	F026	STX	GROUP	
01250	2081	CE	F026	LDX	#GROUP	
01260	2084	7E	E2C8	JMP	\$E0C8	
01270	2087	7D	F022	LOOP	TST	\$F020
01280	208A	26	01	BNE	P1	*PRINT '+'?
01290	208C	39		RTS		*NO
01300	208D	86	2B	P1	LDA A	#\$2B
01310	208F	7E	E1D1	PRINT	JMP	\$E1D1
01320				END		*YES

TOTAL ERRORS 00000

ENTER PASS : 1P,2P,2L,2T

```

00010          NAM    MEMEXS
00020          OPT    0
00030 0100      ORG    $100
00040 E0D0      MON    EQU    $E0D0
00050 F002      MEMSTR EQU    $F002
00060 F004      MEMEND EQU   $F004
00070 *
00080 * EXAMPLE 1 FILLS MEMORY WITH ZEROS
00090 * STARTING AT THE ADDRESS IN MEMSTR
00100 * ($F002 & $F003), UP TO THE ADDRESS
00110 * IN MEMEND ($F004 & $F005).
00120 *
00130 0100 86 00 EXAM1  LDA A #$00
00140 0102 FE F002      LDX    MEMSTR
00150 0105 A7 00      FILL   STA A 0,X
00160 0107 08      INX
00170 0108 BC F004      CPX    MEMEND
00180 010B 26 F8      BNE    FILL
00190 010D 7E E0D0      JMP    MON    GO TO MONITOR
00200 *
00210 * EXAMPLE 2 CHECKS MEMORY FOR ZEROS
00220 * FROM THE ADDRESS IN MEMSTR UP TO THE
00230 * ADDRESS IN MEMEND. WHEN A NON-ZERO
00240 * BYTE IS FOUND, THE SWI INSTRUCTION
00250 * CAUSES THE REGISTERS TO BE PRINTED.
00260 * THE INDEX REGISTER HAS THE ADDRESS
00270 * OF THE NON-ZERO BYTE.
00280 *
00290 0110 FE F002 EXAM2  LDX    MEMSTR
00300 0113 09      DEX
00310 0114 86 00 COMP   LDA A #$00
00320 0116 08      INX
00330 0117 BC F004 NEXT   CPX    MEMEND
00340 011A 26 03      BNE    CONT
00350 011C 7E E0D0      JMP    MON    GO TO MONITOR
00360 011F A1 00 CONT   CMP A 0,X
00370 0121 27 F1      BEQ    COMP
00380 0123 3F      SWI
00390                      END               ERROR - DISPLAY REGISTERS

```

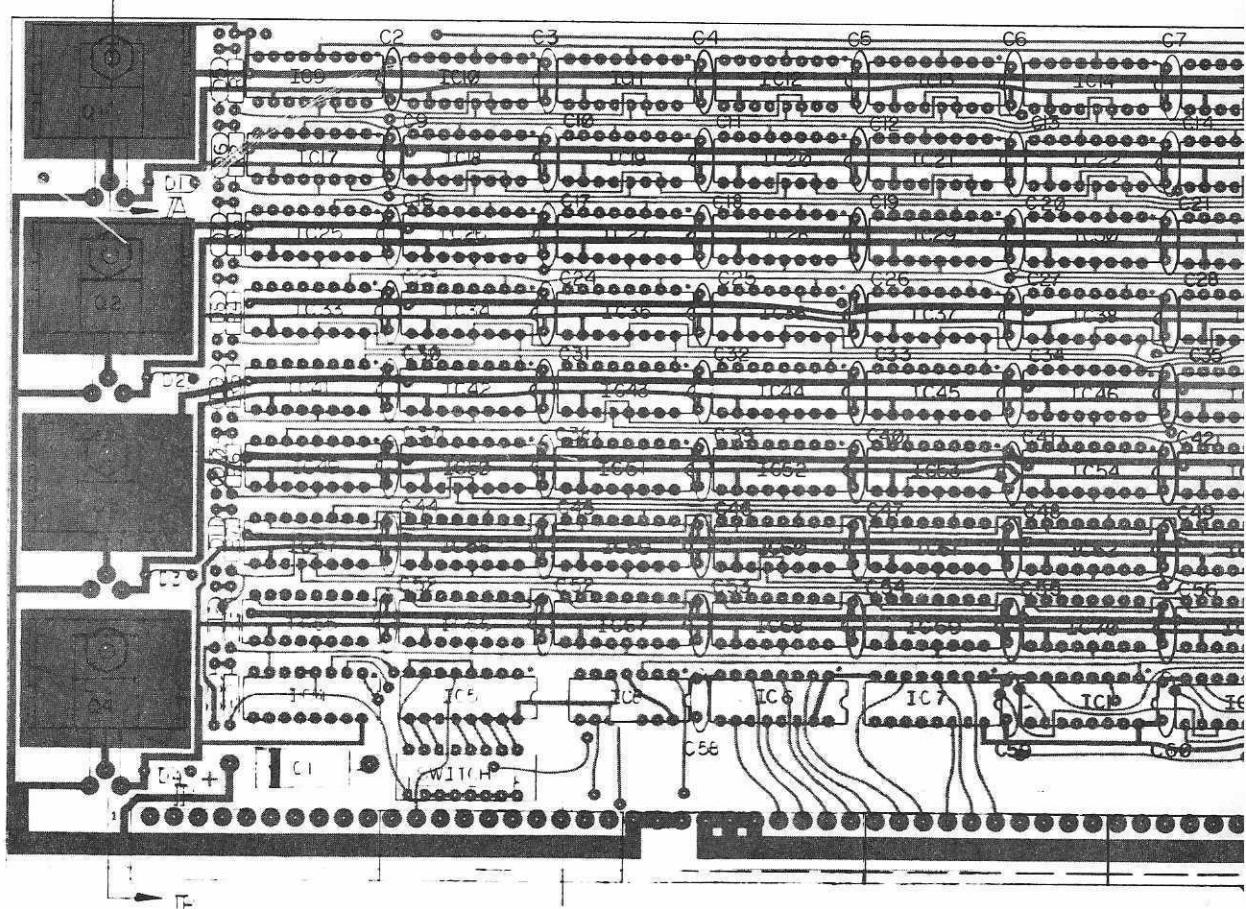
TOTAL ERRORS 00000

ENTER PASS : 1P,2P,2L,2T

8 7 6 5

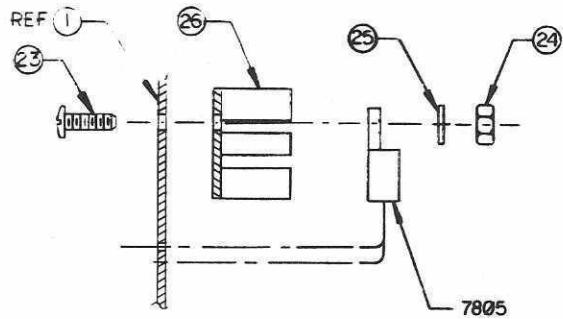
D

A



B

FOR CONN PIN 1E (2) --



A

DETAIL A-A

MOUNTING HARDWARE FOR
VOLTAGE REGULATOR
4 PLACES

② FT98 IS INTERCHANGEABLE WITH 74368 OR 8098.

① FT97 IS INTERCHANGEABLE WITH 74367 OR 8097.

NOTES: UNLESS OTHERWISE SPECIFIED

8

7

6

5

4

3

2

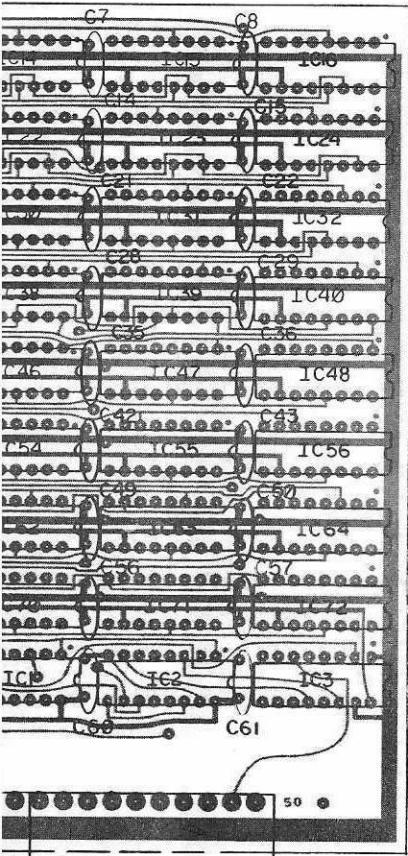
1

D

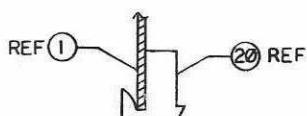
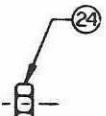
C

B

A



(20) 5 PLACES

VIEW IB-IB

7805

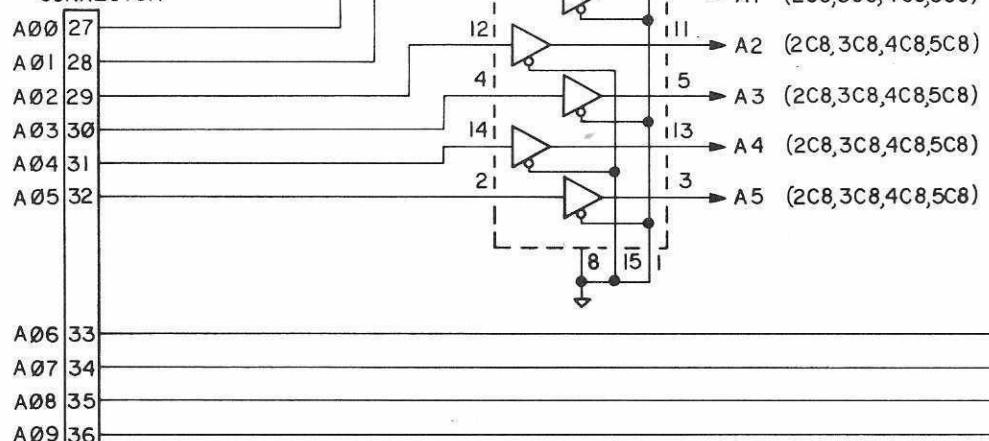
ITEM	QTY	PART NUMBER	DESCRIPTION	REF DES	MSIPN
PARTS LIST					
DRWN K.Ophus	DATE 2-21-76	<i>Midwest Scientific Instruments Olathe, Kansas</i>			
CHK	DATE				
APPR	DATE	TITLE MSI 6800 COMPUTER ASSY, RAM-68, 8K RAM			
MATERIAL					
SIZE	MSI PART NO.	DRWG NO.	REV		
D	REF 967	100044	-		
SCALE	2/1	SHEET	1 OF 1		

8

7

6

5

50 PIN
CONNECTOR

A I0 37

A I1 38

A I2 39

A I3 40

A I4 41

A I5 42

+8VUR { 21 → +8VUR

22 → +8VUR

23 → +8VUR

GND { 24 → GND

25 → GND

26 → GND

R/W 10

Ø2 12

VMA 11

+5V → IC8 (10)

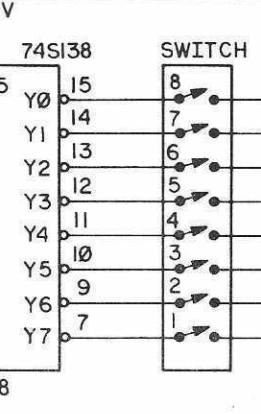
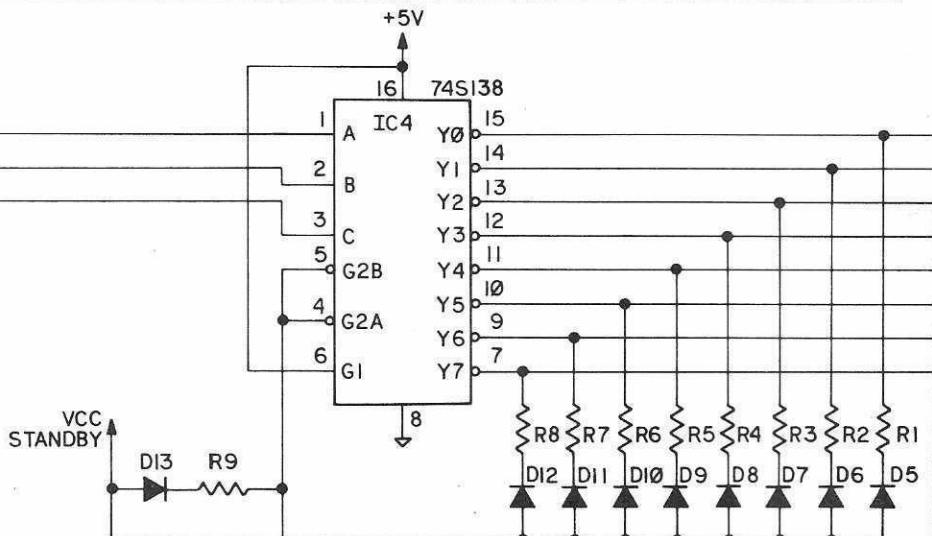
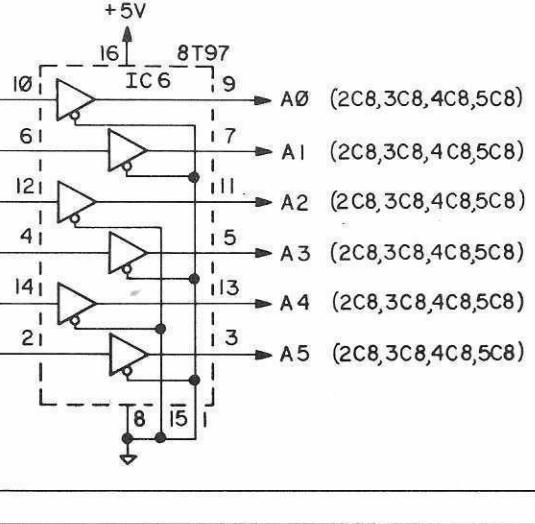
IC8 (9) → 7400 (8)

7400 (4) → +5V

7400 (5) → IC5 (16)

7400 (6) → IC5 (8)

7400 (7) → GND



5

8

7

6

6

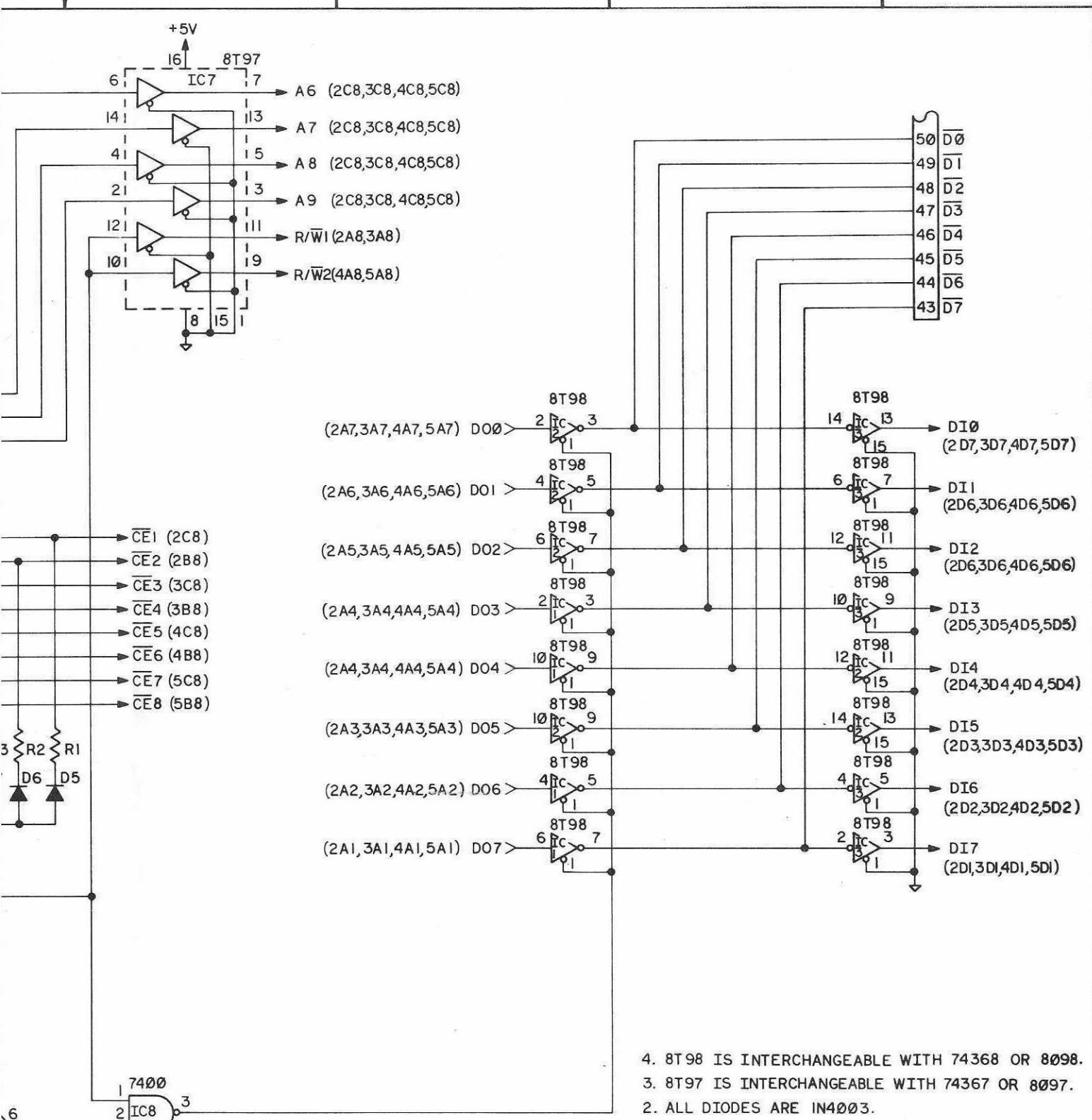
4

2

10

1

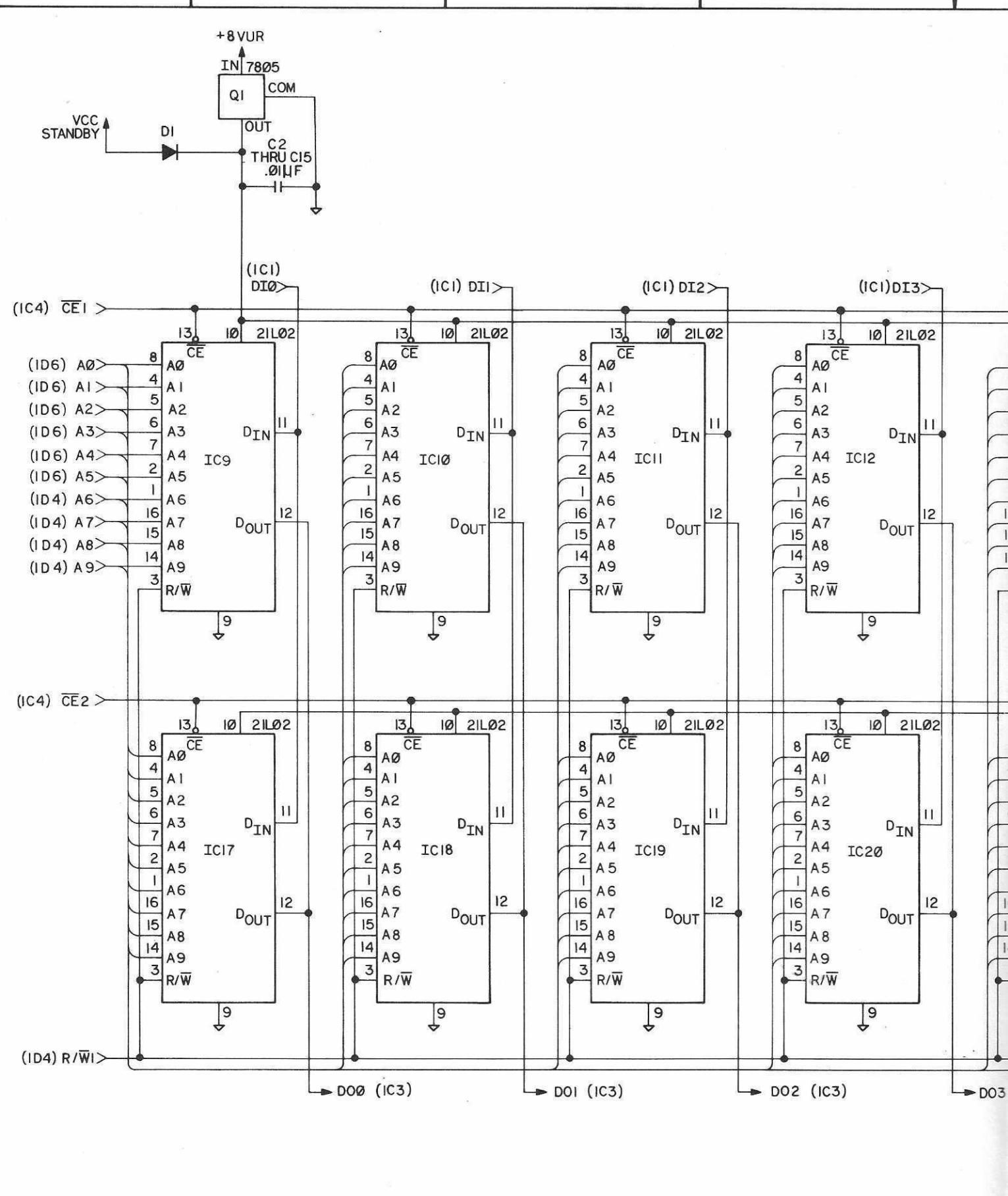
2



4. 8T98 IS INTERCHANGEABLE WITH 74368 OR 8098.
3. 8T97 IS INTERCHANGEABLE WITH 74367 OR 8097.
2. ALL DIODES ARE IN4003.
1. ALL RESISTORS ARE 6.8K OHMS, $\pm 10\%$, 1/4W.

NOTES: UNLESS OTHERWISE SPECIFIED

DRAWN K. Orlin	DATE 12-7-77	Midwest Scientific Instruments	
CHK K. Orlin	DATE 12-15-77	Olathe, Kansas	
APPR C.C. Chidress	DATE 12-15-77	TITLE MSI 6800 COMPUTER SCHEM, RAM-68, 8K RAM	
MATERIAL		SIZE 24 36	MSI PART NO. REF 967
		SCALE	DRWG NO. 100040
			REV -
		SHEET	1 OF 5



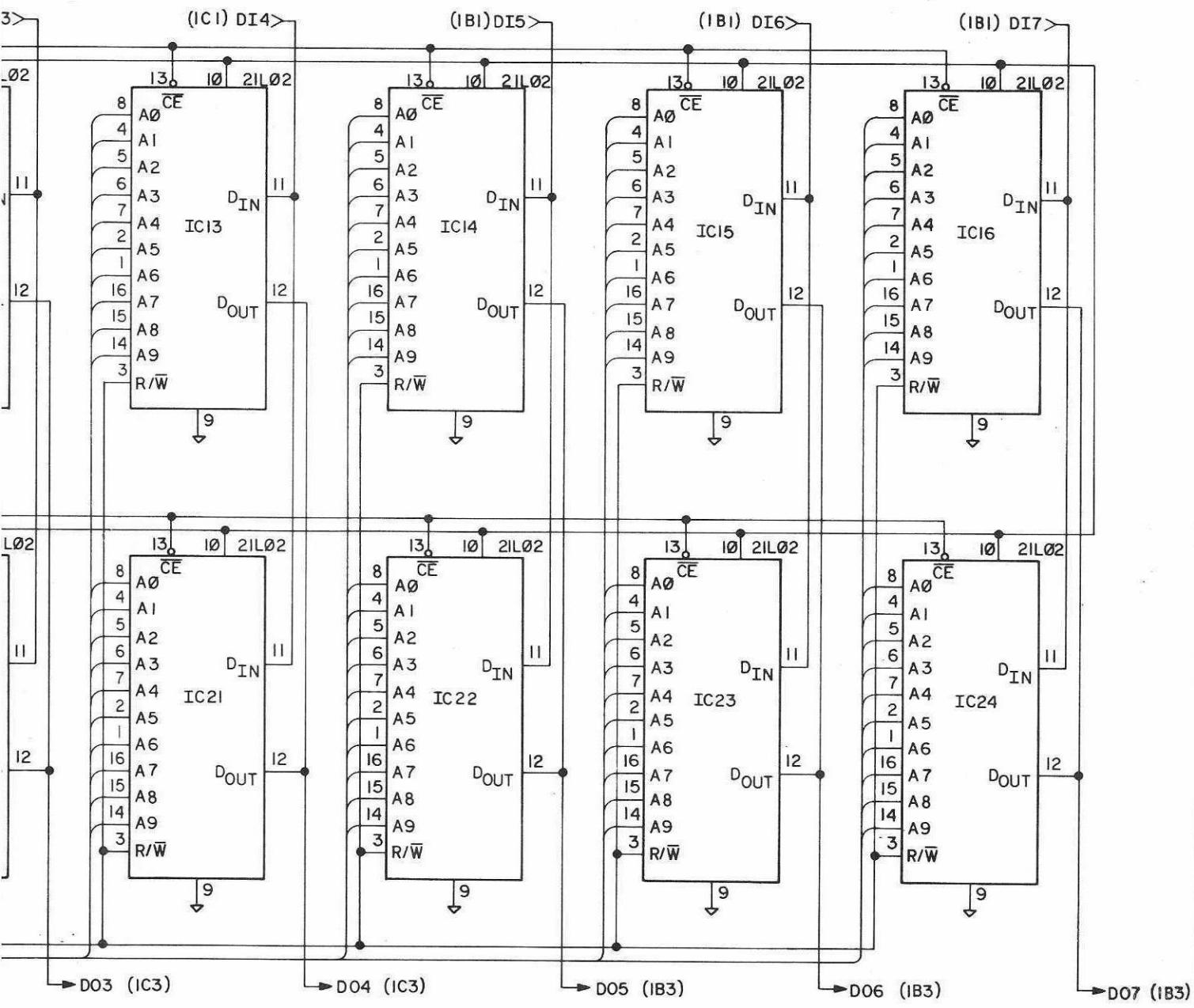
8

7

6

5

D



DRWG NO.	100040	REV
SHEET	2	OF

A

C

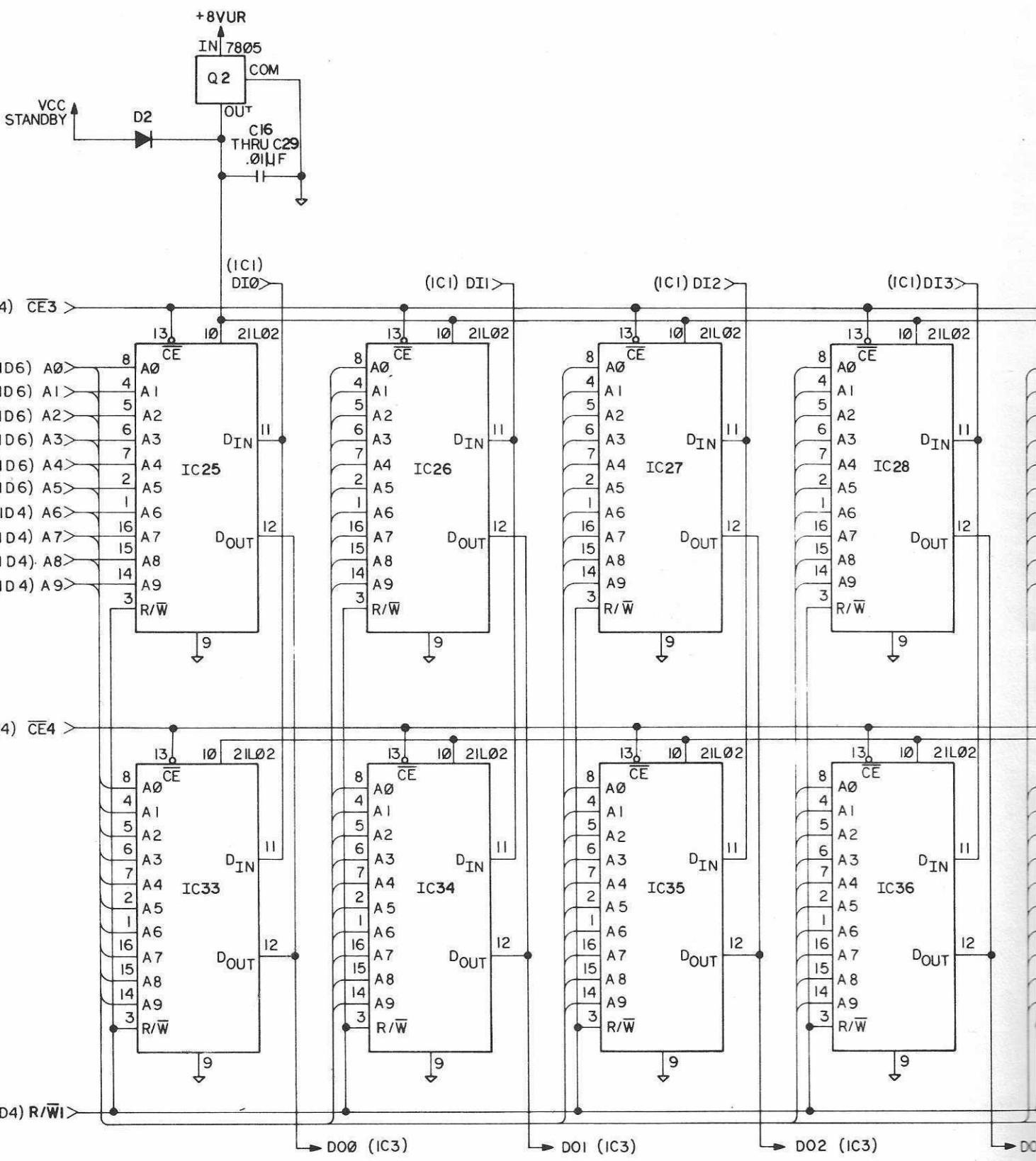
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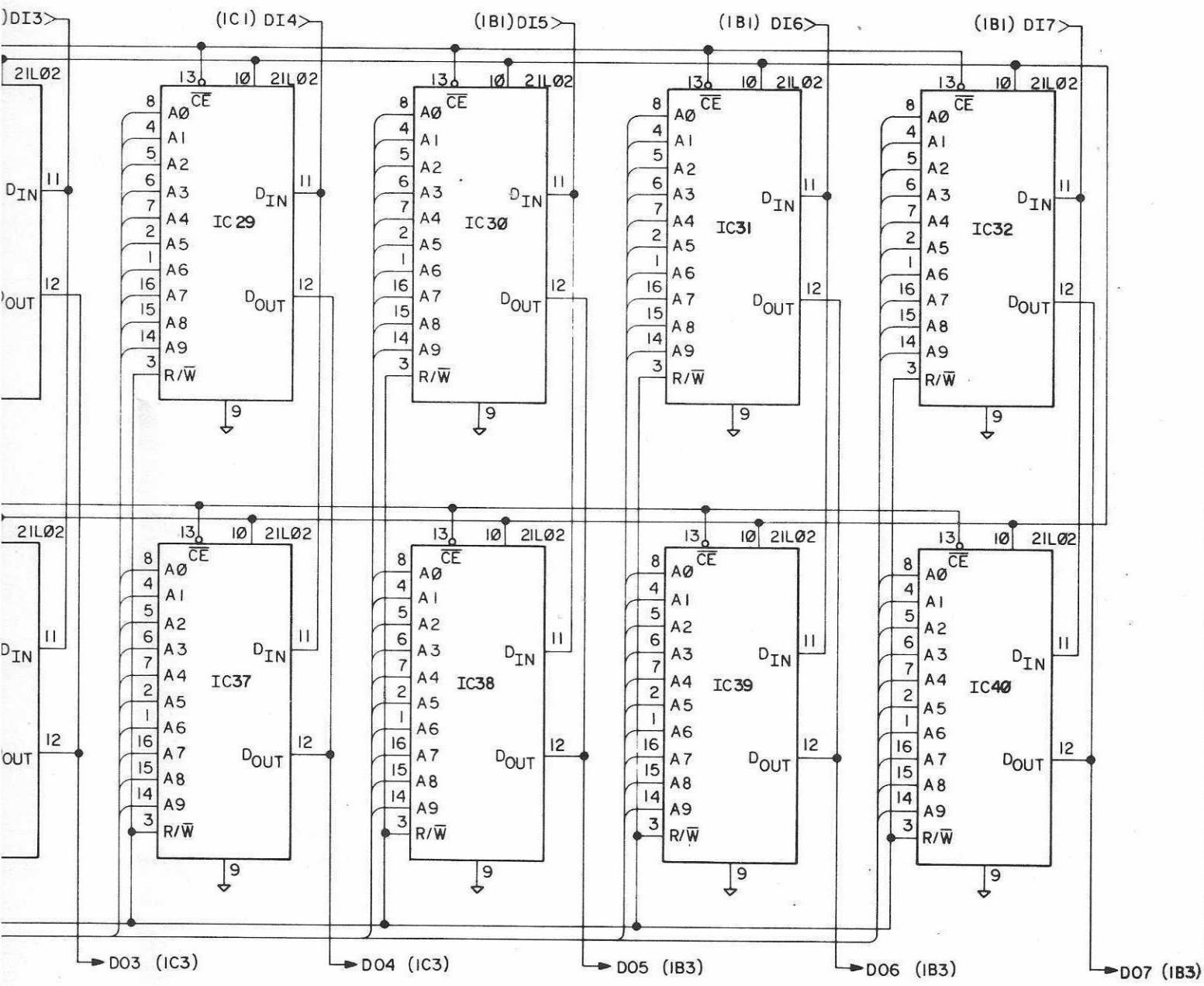


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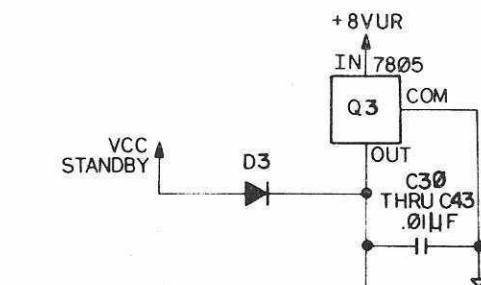
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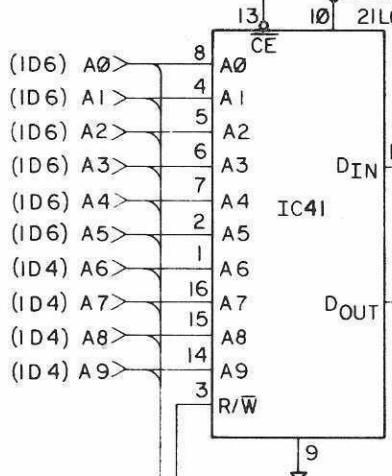
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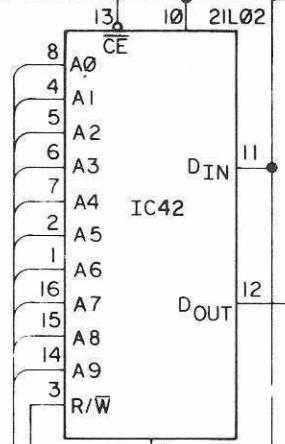
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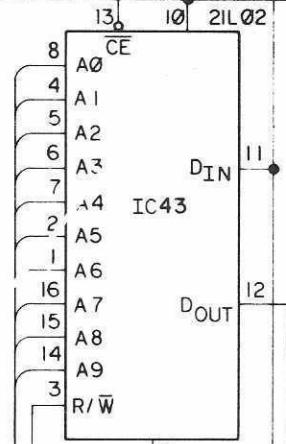
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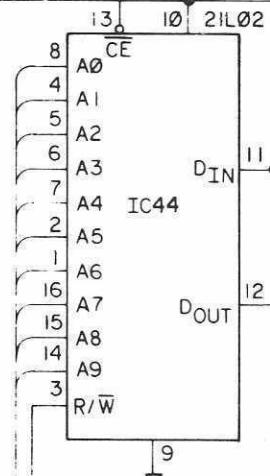
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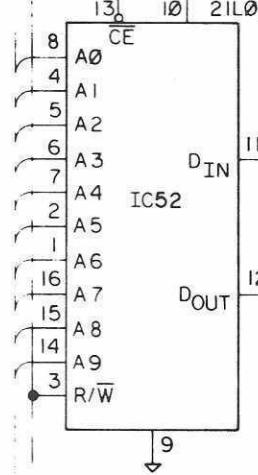
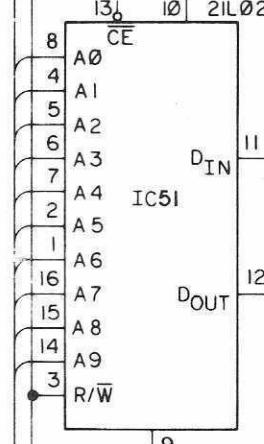
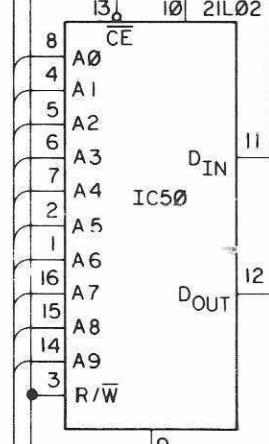
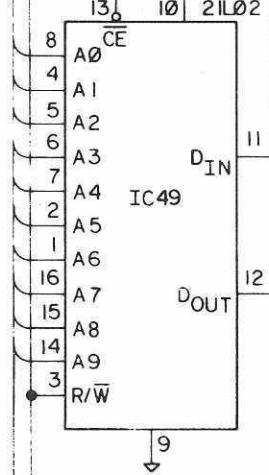
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(IC1) DI3 >



(IC4) CE6 >



(ID4) R/W2 >

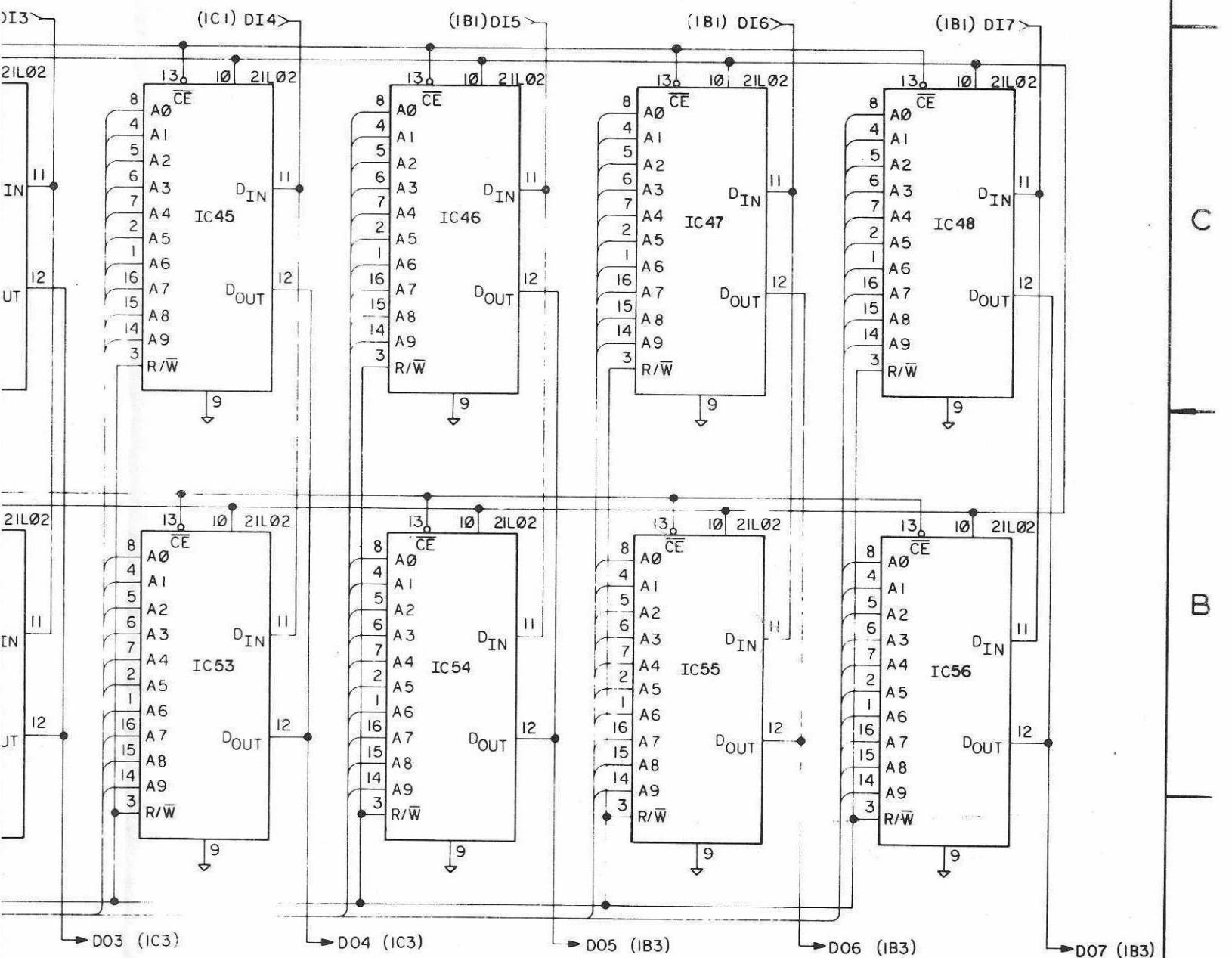
DO0 (IC3)

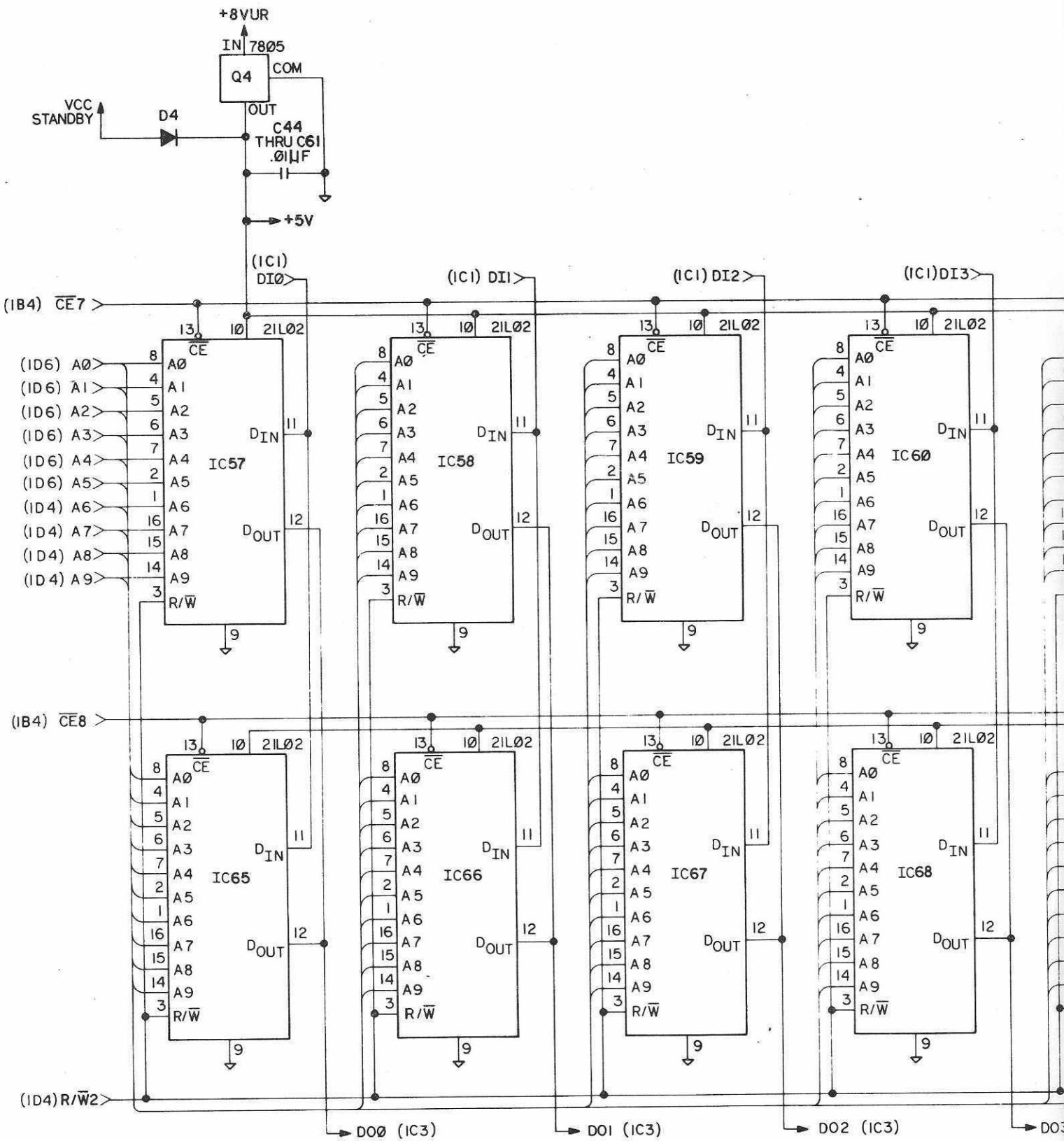
DO1 (IC3)

DO2 (IC3)

DO3

A





UNUSED IC PINS

IC TYPE	REF DES	PIN NUMBERS
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8T98	IC 1	11 THRU 15

