

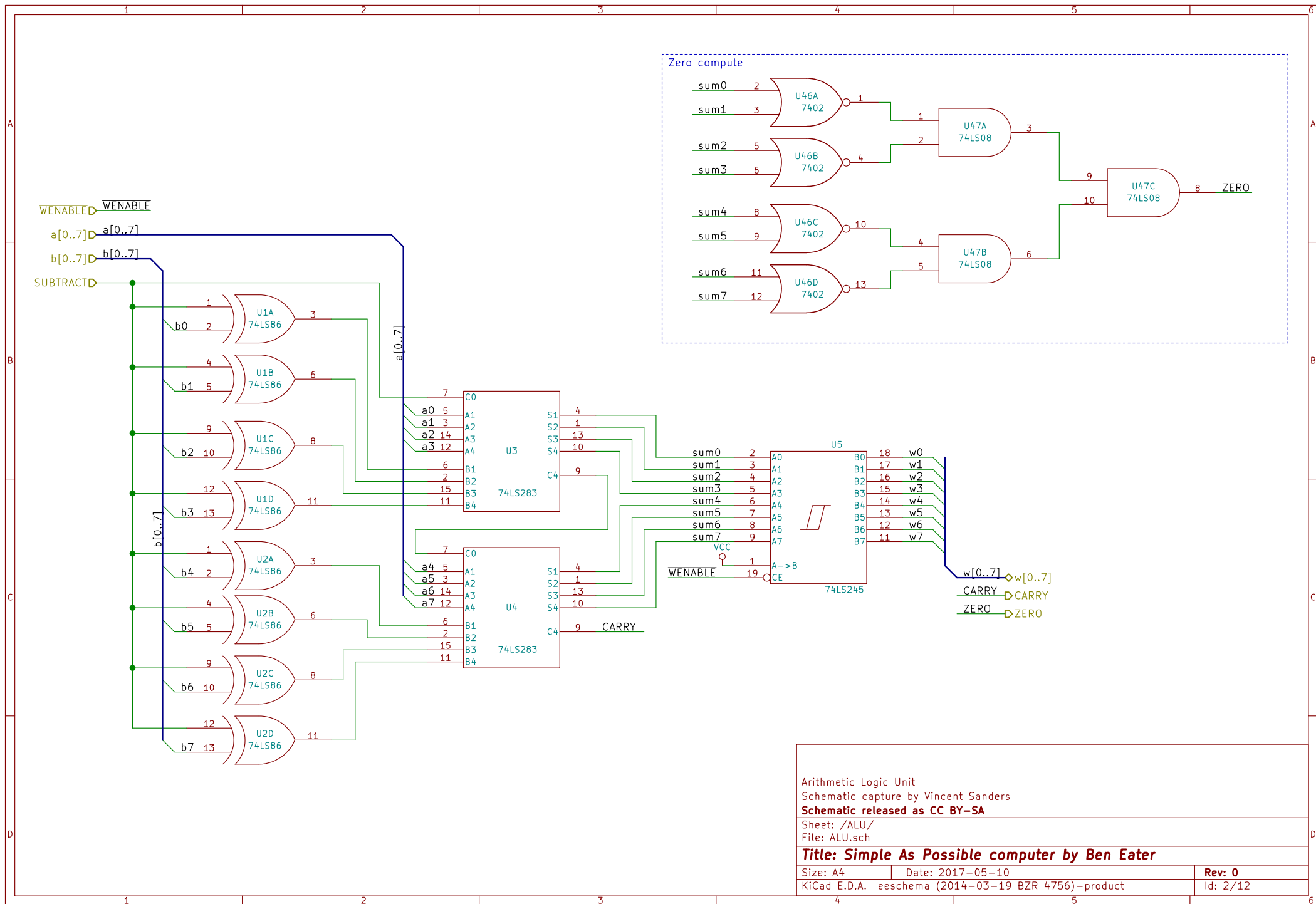
Main w bus and top level view
Schematic capture by Vincent Sanders
Schematic released as CC BY-SA

Sheet: /
File: sap-be.sch

Title: Simple As Possible computer by Ben Eater

Size: A4 Date: 2017-05-10
KiCad E.D.A. eeschema (2014-03-19 BZR 4756)-product

Rev: 0
Id: 1/12



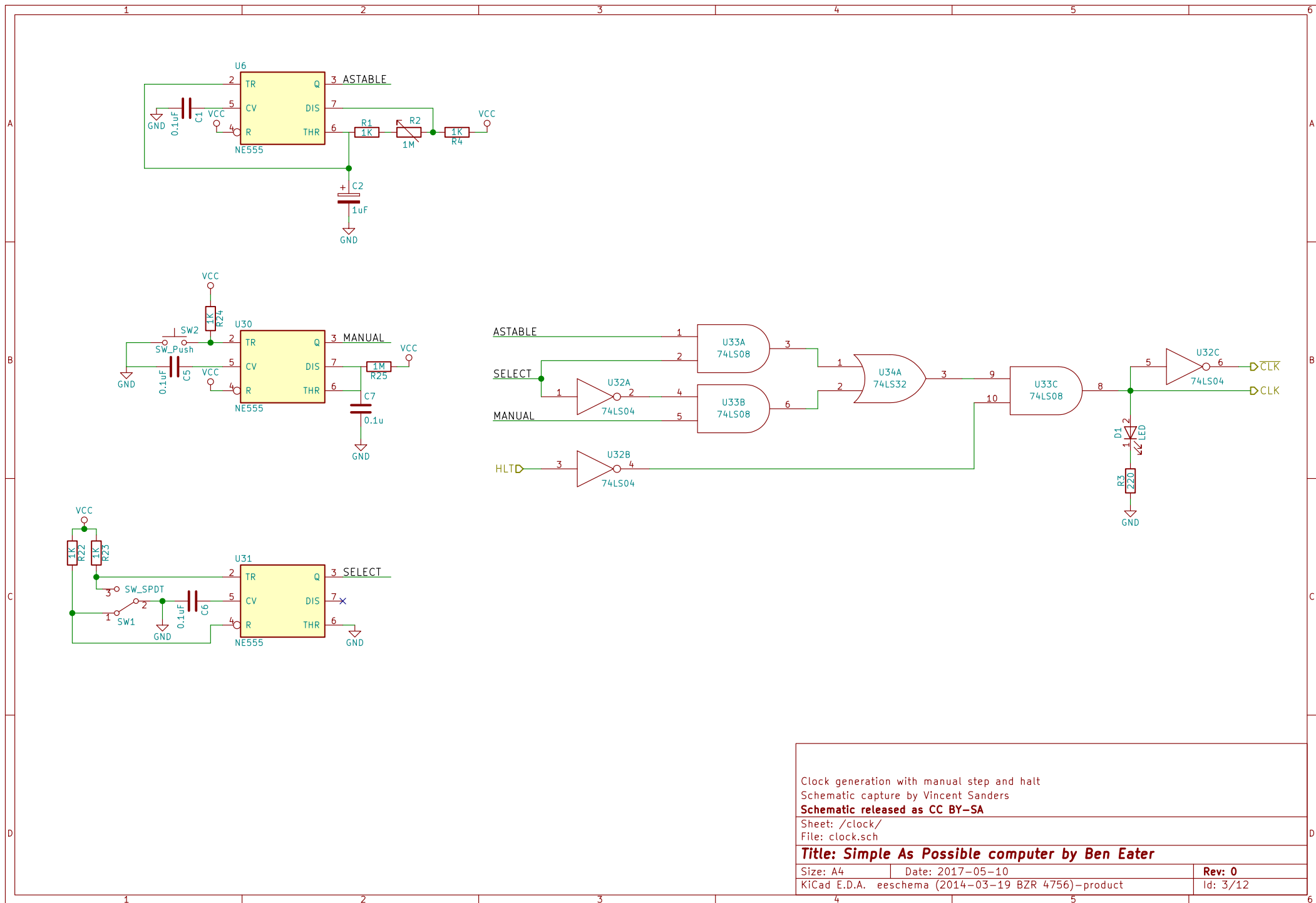
Arithmetic Logic Unit
Schematic capture by Vincent Sanders
Schematic released as CC BY-SA

Sheet: /ALU/
File: ALU.sch

Title: Simple As Possible computer by Ben Eater

Size: A4 Date: 2017-05-10
KiCad E.D.A. eeschema (2014-03-19 BZR 4756)-product

Rev: 0
Id: 2/12



Clock generation with manual step and halt

Schematic capture by Vincent Sanders

Schematic released as CC BY-SA

Sheet: /clock/

File: clock.sch

Title: Simple As Possible computer by Ben Eater

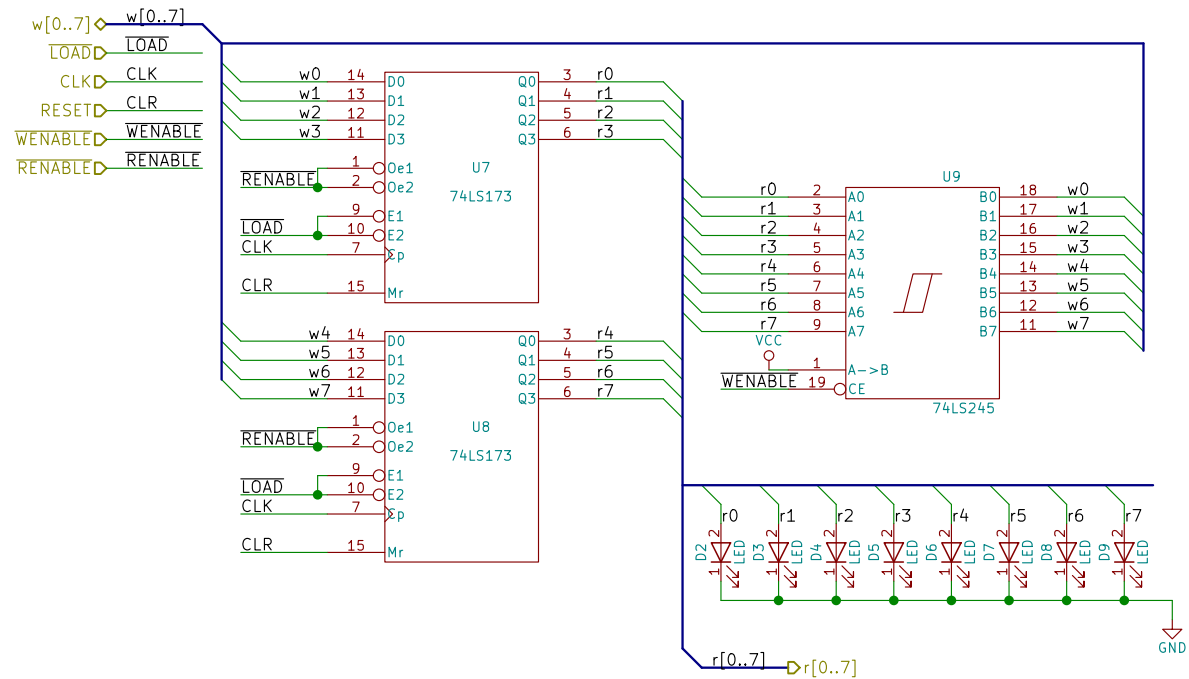
Size: A4

Date: 2017-05-10

Rev: 0

KiCad E.D.A. eeschema (2014-03-19 BZR 4756)-product

Id: 3/12



Schematic capture by Vincent Sanders

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Sheet: /RegisterB/

File: register.sch

Title: Simple As Possible computer by Ben Eater

Size: A4

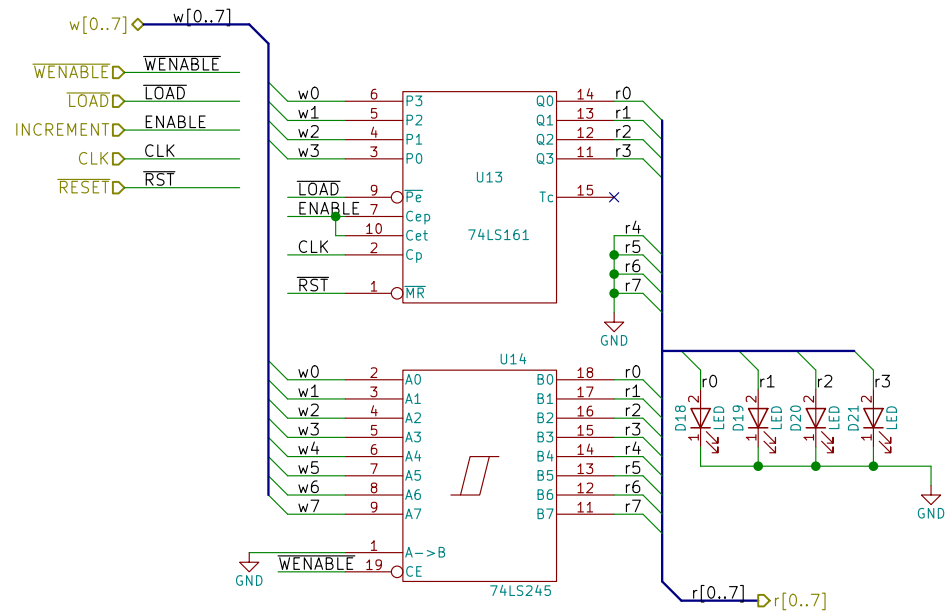
Date: 2017-05-10

Rev: 0

KiCad E.D.A. eeschema (2014-03-19 BZR 4756)-product

Id: 4/12

Id: 5/12



Schematic capture by Vincent Sanders

Schematic released as CC BY-SA

Sheet: /PC/

File: programcounter.sch

Title: Simple As Possible computer by Ben Eater

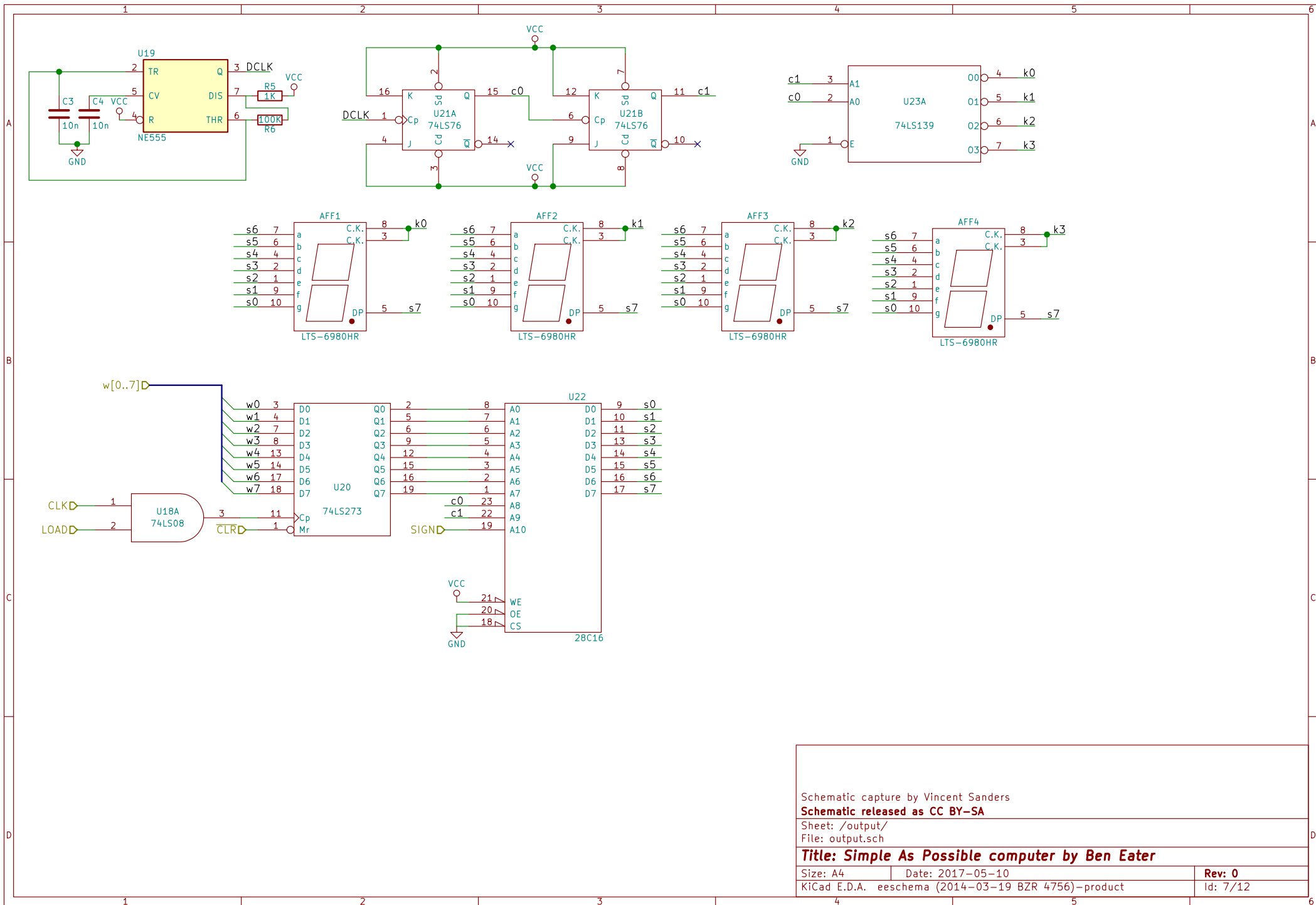
Size: A4

Date: 2017-05-10

Rev: 0

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Id: 6/12



Schematic capture by Vincent Sanders

Schematic released as CC BY-SA

Sheet: /output/

File: output.sch

Title: Simple As Possible computer by Ben Eater

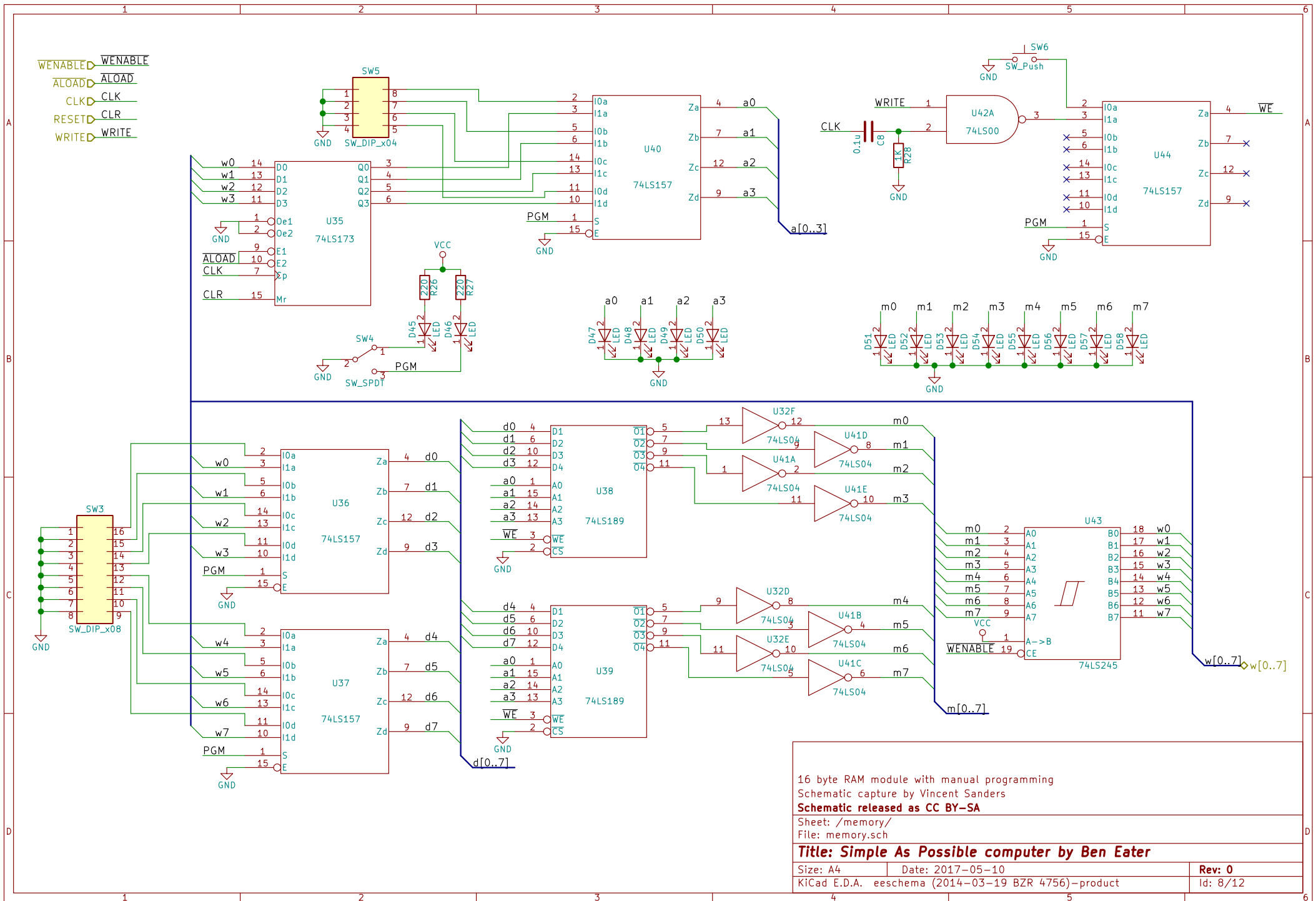
Size: A4

Date: 2017-05-10

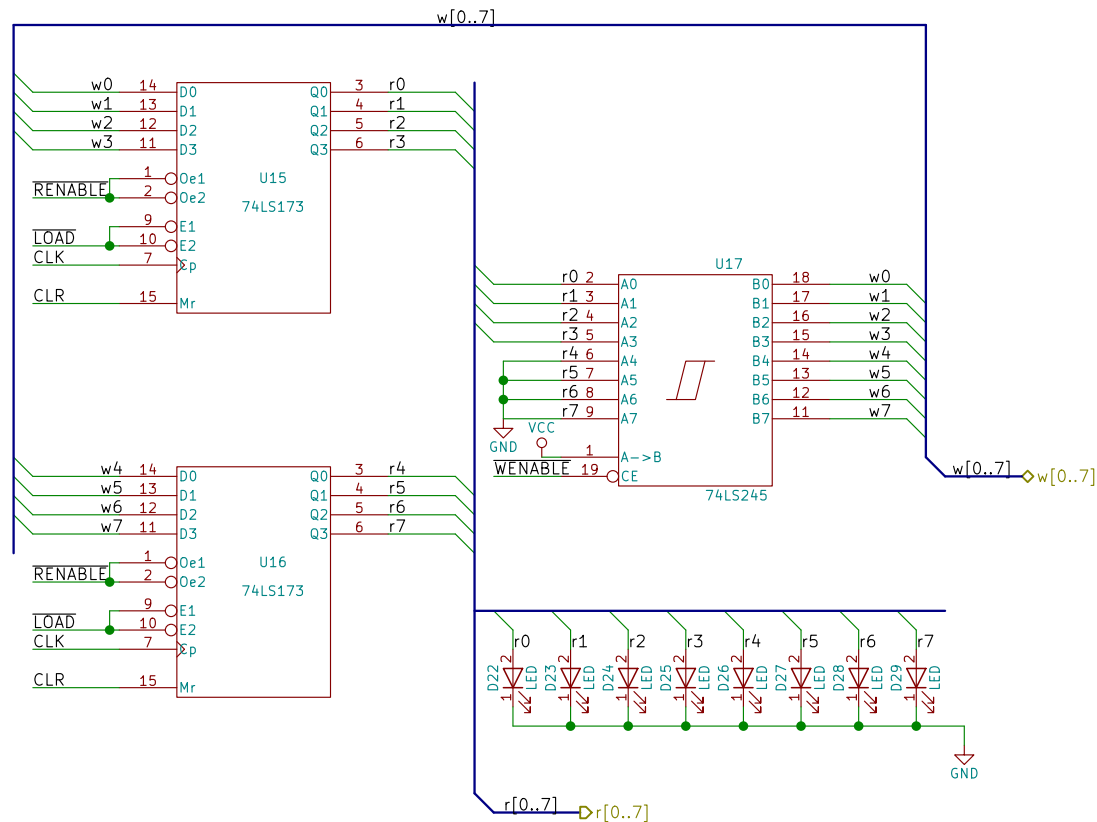
Rev: 0

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Id: 7/12



LOAD \triangleright LOAD
 CLK \triangleright CLK
 RESET \triangleright CLR
 WENABLE \triangleright WENABLE
 RENABLE \triangleright RENABLE



Schematic capture by Vincent Sanders

Schematic released as CC BY-SA

Sheet: /IR/

File: instructionregister.sch

Title: Simple As Possible computer by Ben Eater

Size: A4

Date: 2017-05-10

Rev: 0

KiCad E.D.A. eeschema (2014-03-19 BZR 4756)-product

Id: 10/12

