

Alternative Implementations

Memory as built in videos

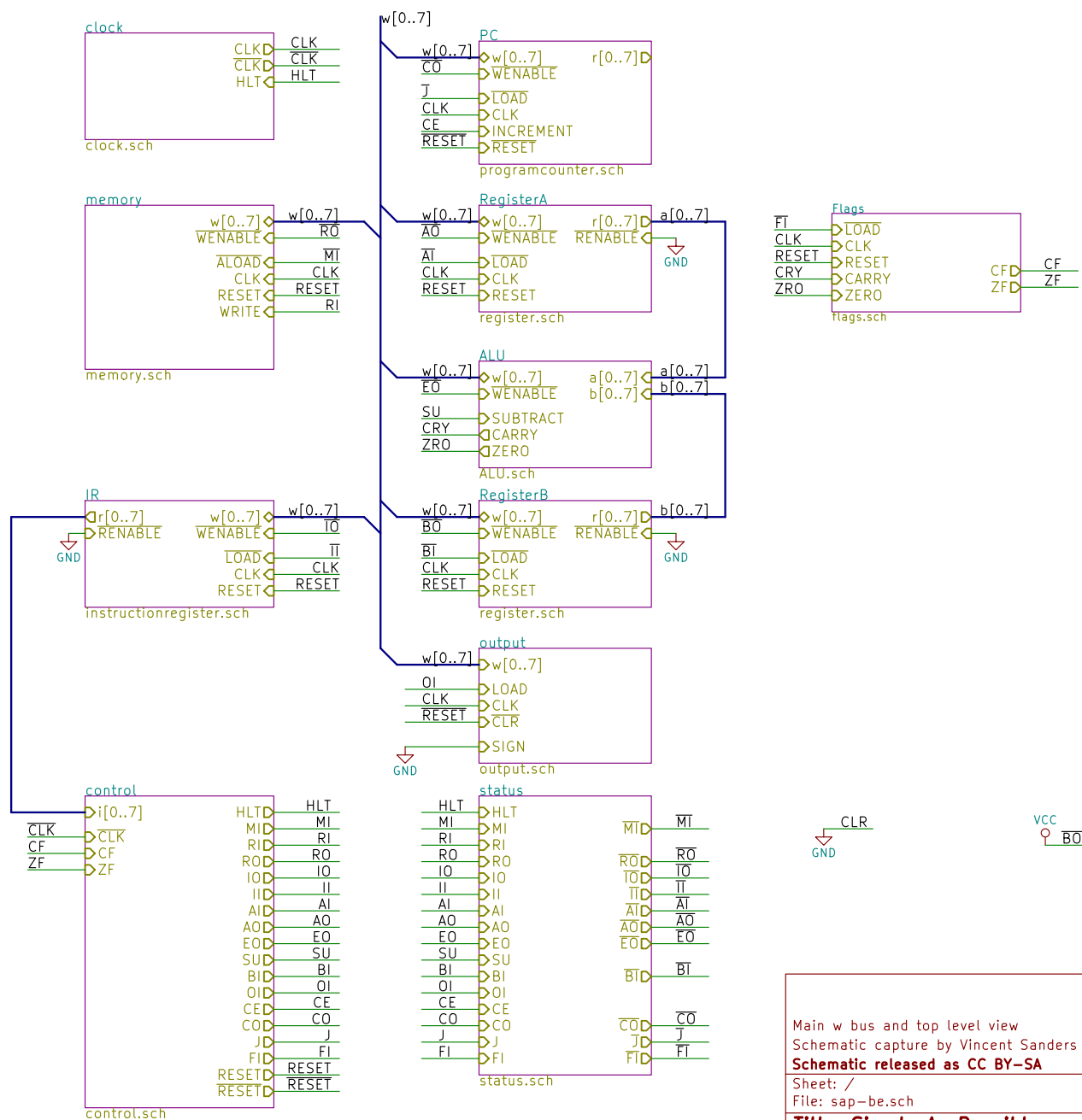
memory-orig

memory-orig.sch

Memory with minor bugfixes

memory-bugfix

memory-bugfix.sch



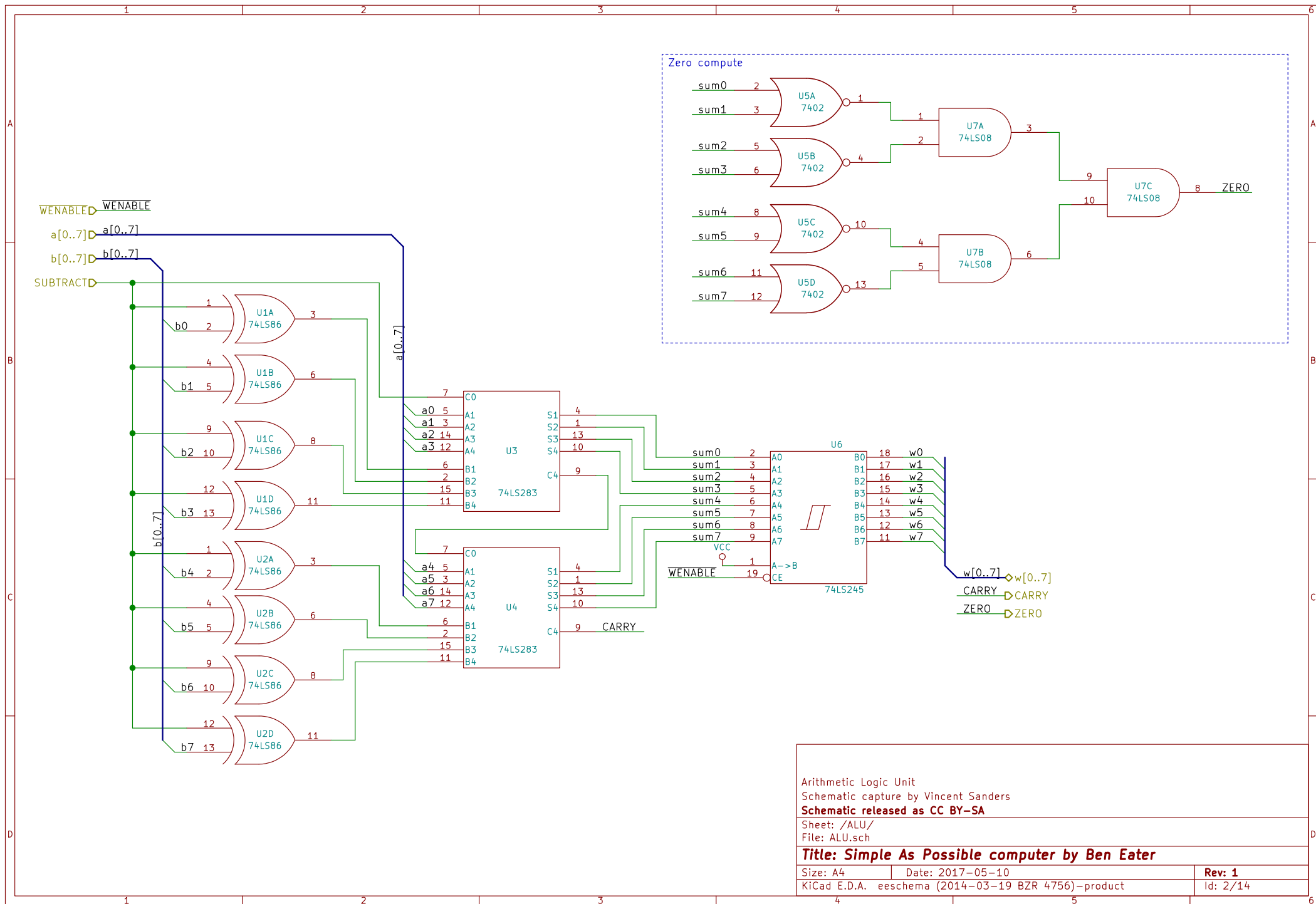
Main w bus and top level view
Schematic capture by Vincent Sanders
Schematic released as CC BY-SA

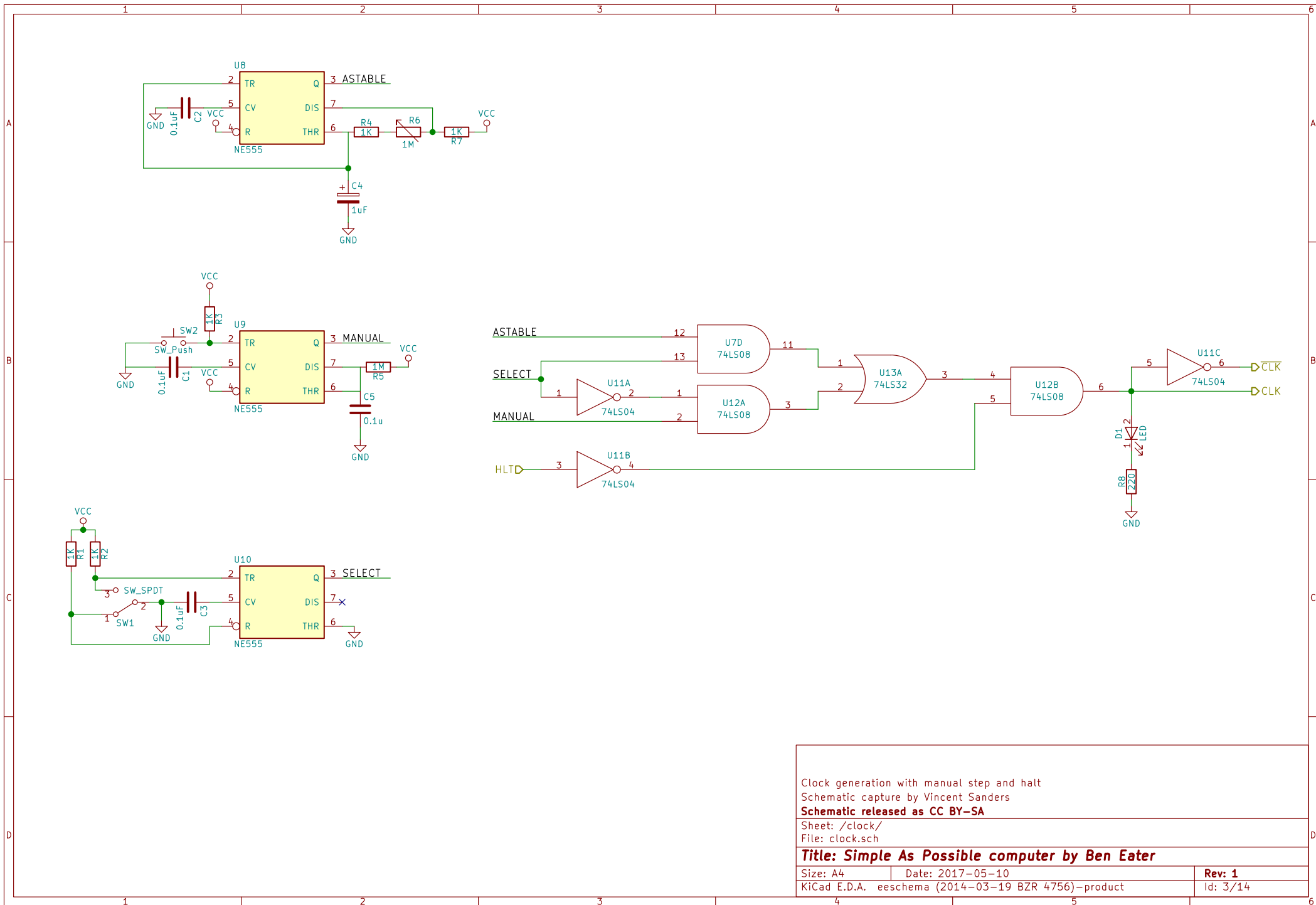
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File: sap-be.sch

Title: Simple As Possible computer by Ben Eater

Size: A4 Date: 2017-05-10
KiCad E.D.A. eeschema (2014-03-19 BZR 4756)-product

Rev: 1
Id: 1/14





Clock generation with manual step and halt

Schematic capture by Vincent Sanders

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Sheet: /clock/

File: clock.sch

Title: Simple As Possible computer by Ben Eater

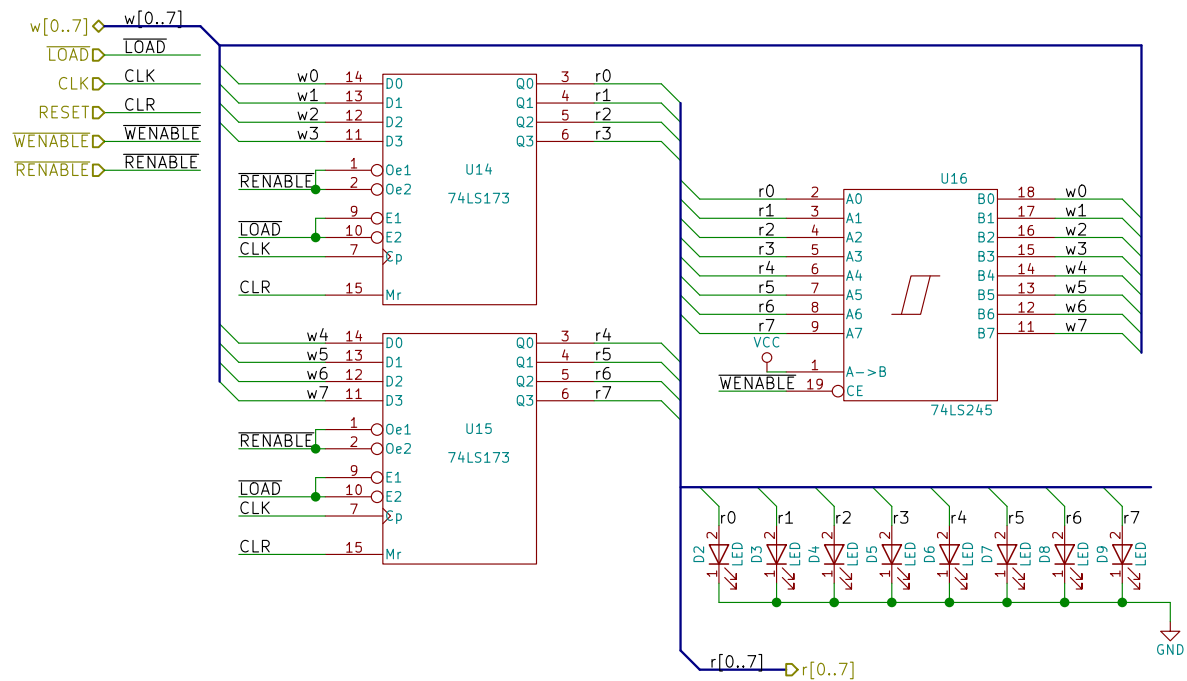
Size: A4

Date: 2017-05-10

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Id: 3/14



Schematic capture by Vincent Sanders

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Sheet: /RegisterB/

File: register.sch

Title: Simple As Possible computer by Ben Eater

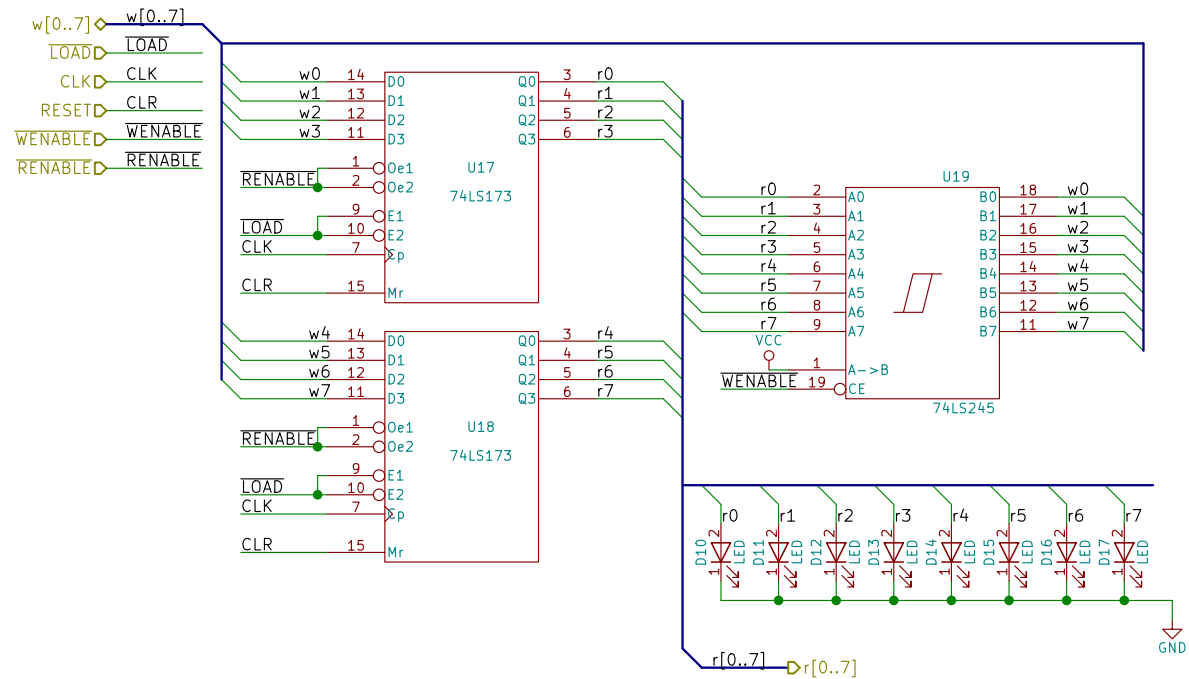
Size: A4

Date: 2017-05-10

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Id: 4/14



Schematic capture by Vincent Sanders

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Sheet: /RegisterA/

File: register.sch

Title: Simple As Possible computer by Ben Eater

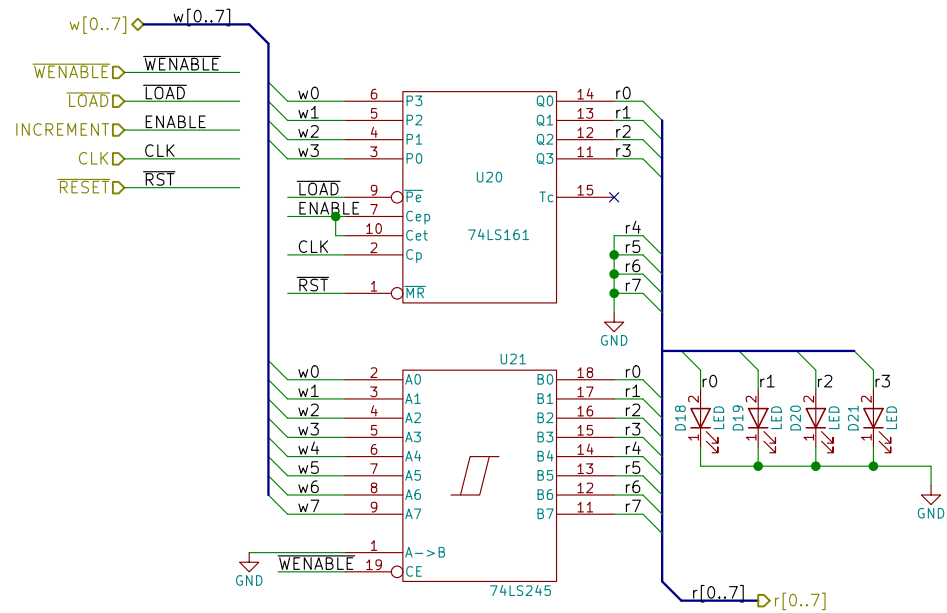
Size: A4

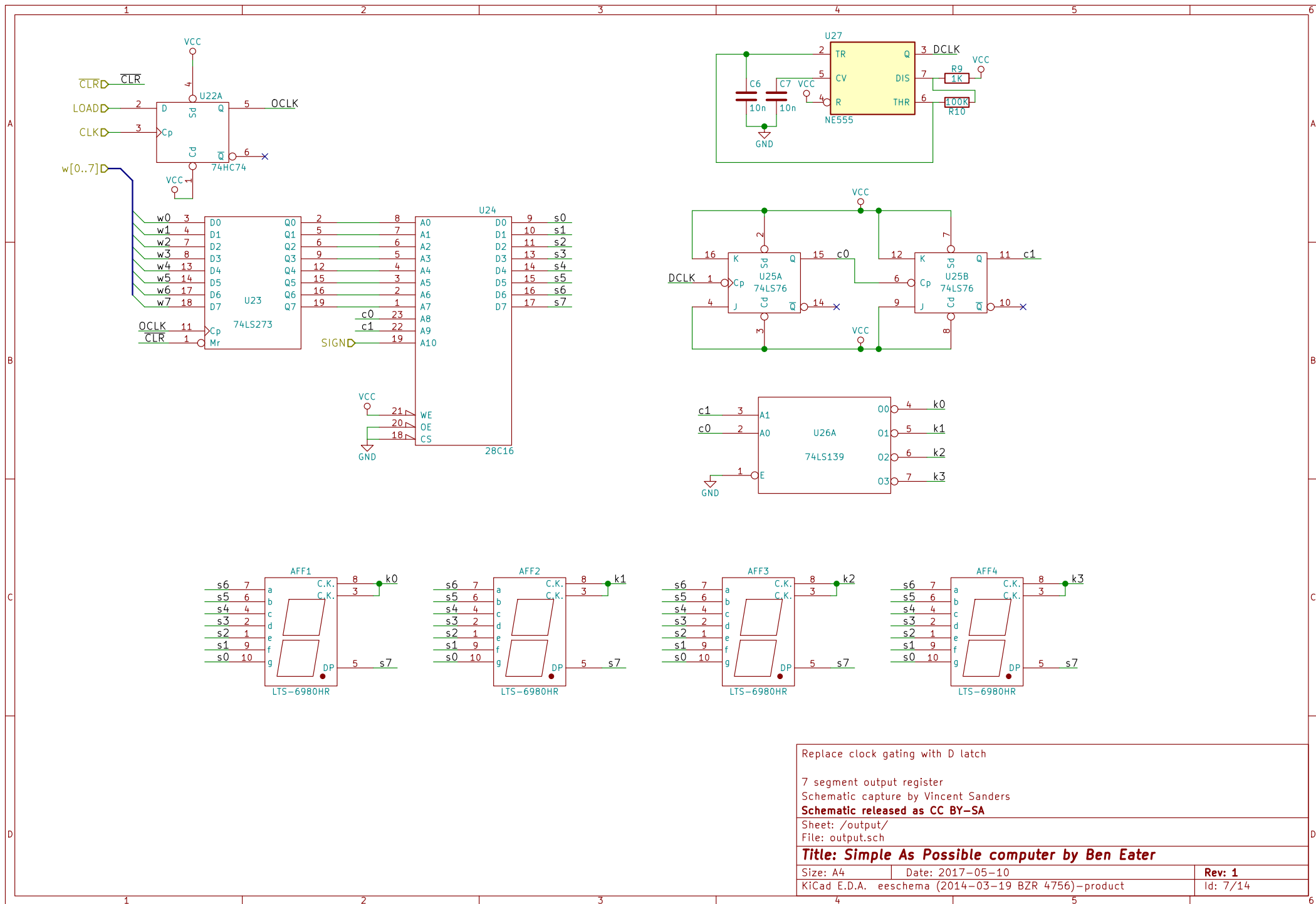
Date: 2017-05-10

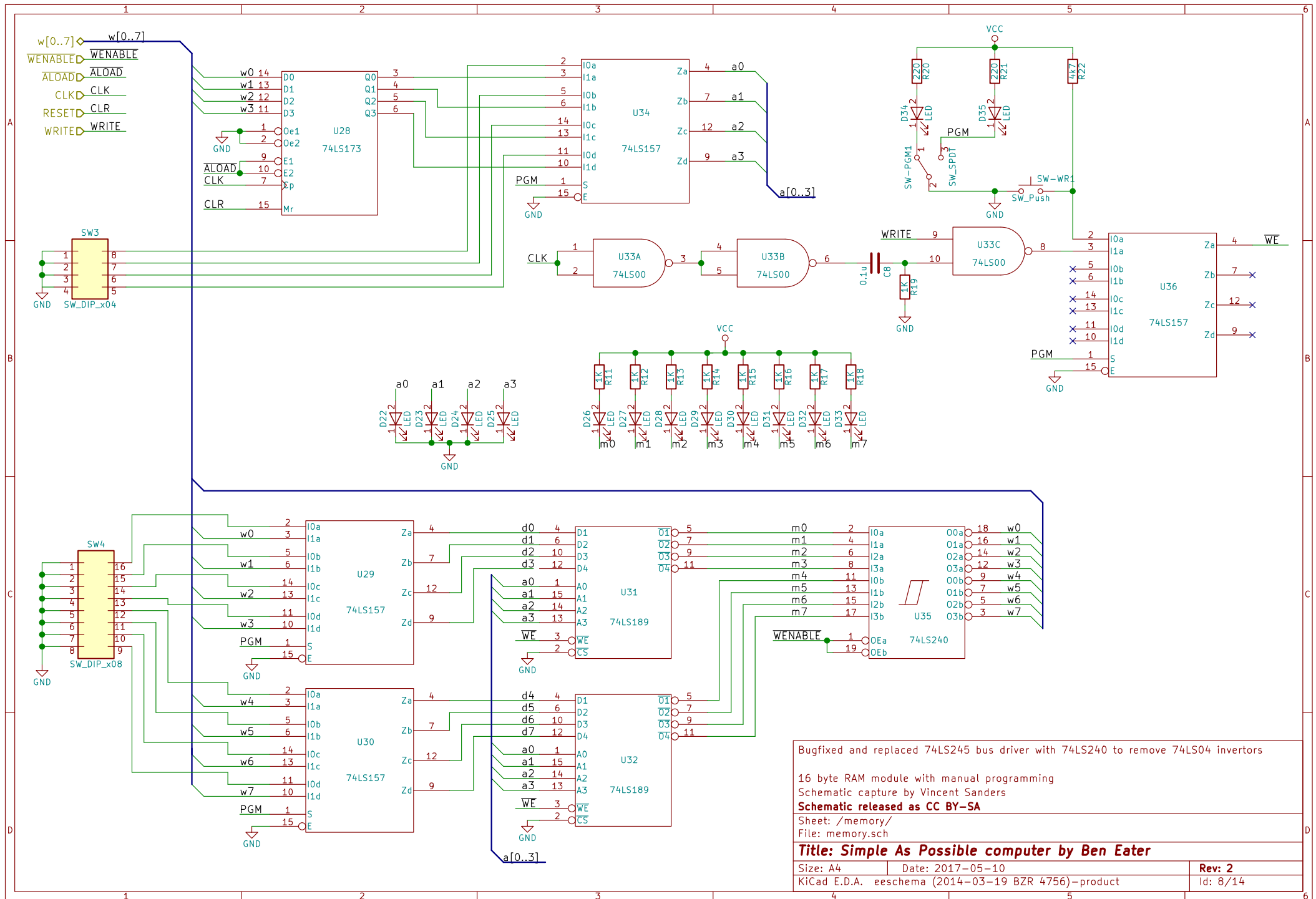
Rev: 1

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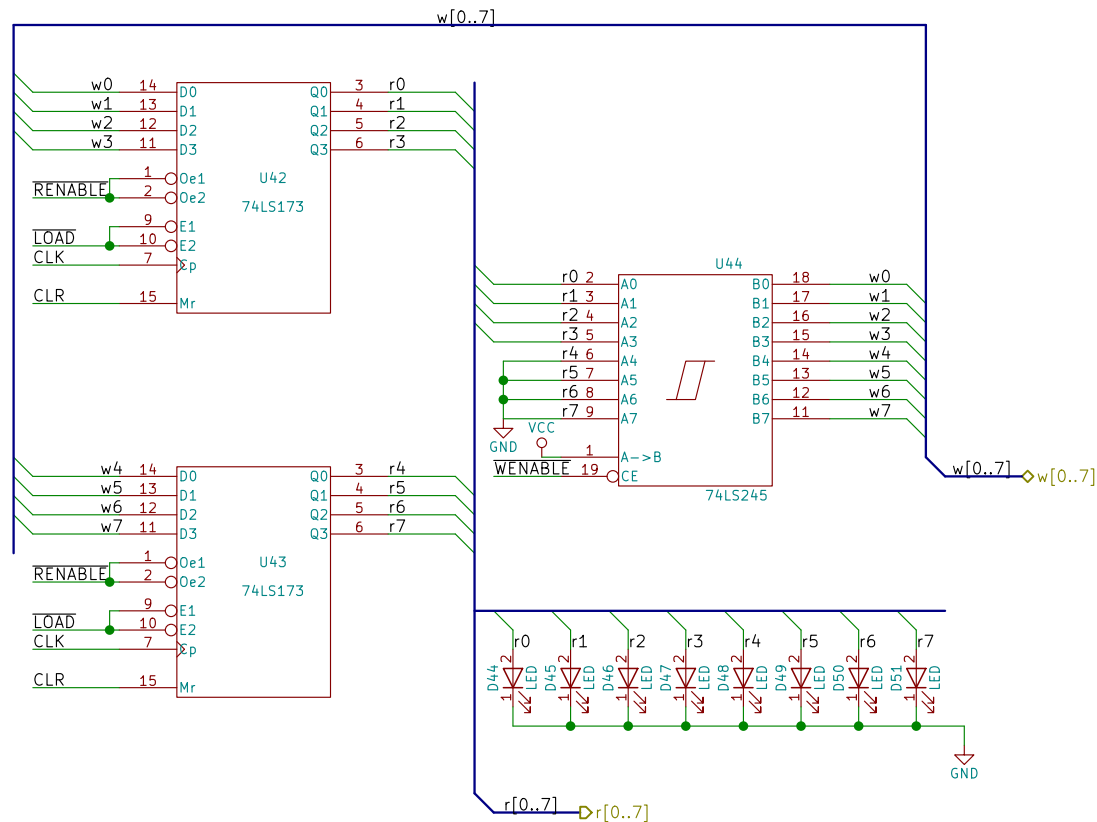
Id: 5/14







LOAD \triangleright $\overline{\text{LOAD}}$
 CLK \triangleright CLK
 RESET \triangleright CLR
 WENABLE \triangleright $\overline{\text{WENABLE}}$
 RENABLE \triangleright $\overline{\text{REENABLE}}$

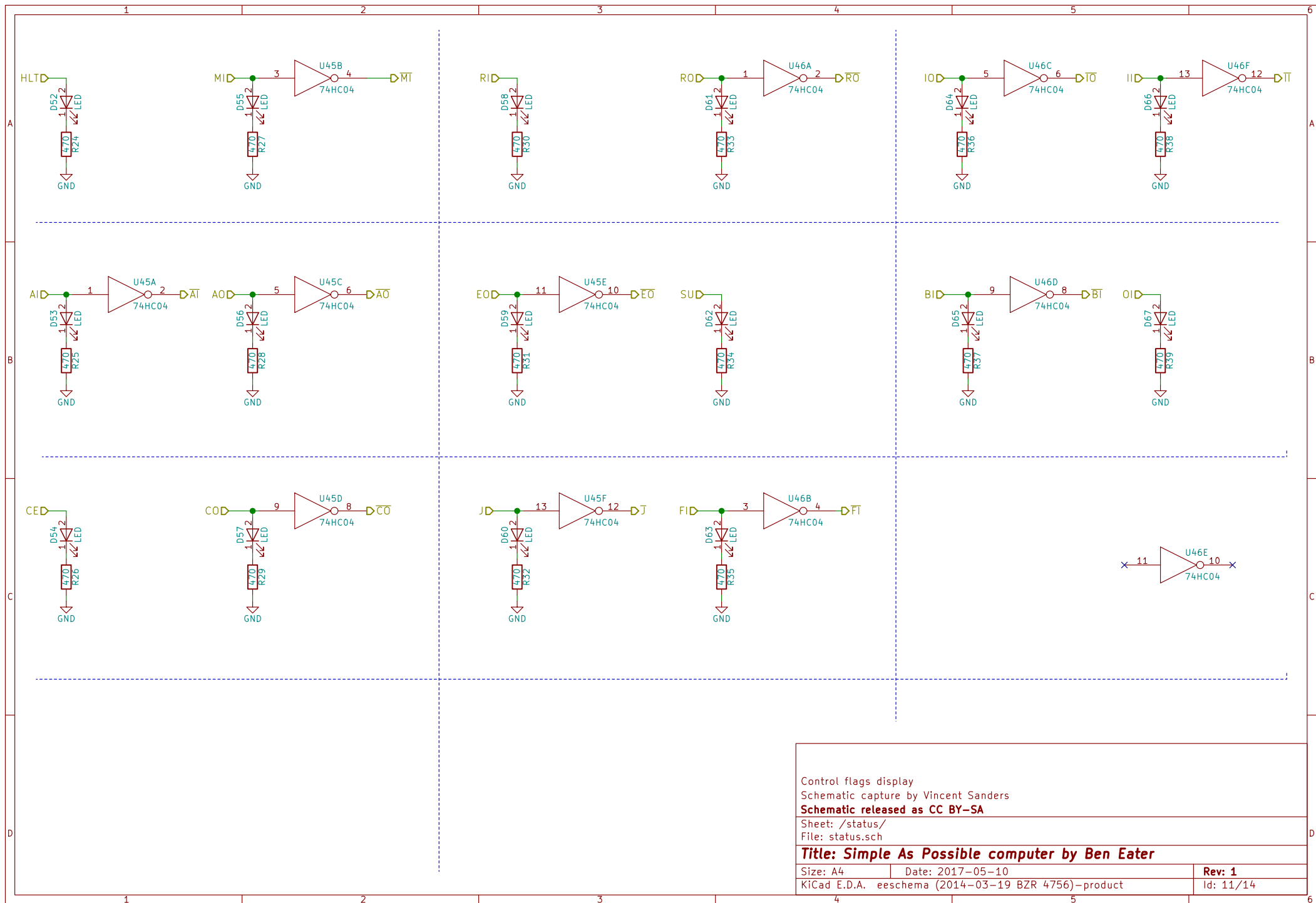


Instruction register
 Schematic capture by Vincent Sanders
Schematic released as CC BY-SA

Sheet: /IR/
 File: instructionregister.sch

Title: Simple As Possible computer by Ben Eater

Size: A4	Date: 2017-05-10	Rev: 1
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Control flags display
Schematic capture by Vincent Sanders
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Sheet: /status/
File: status.sch

Title: Simple As Possible computer by Ben Eater

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