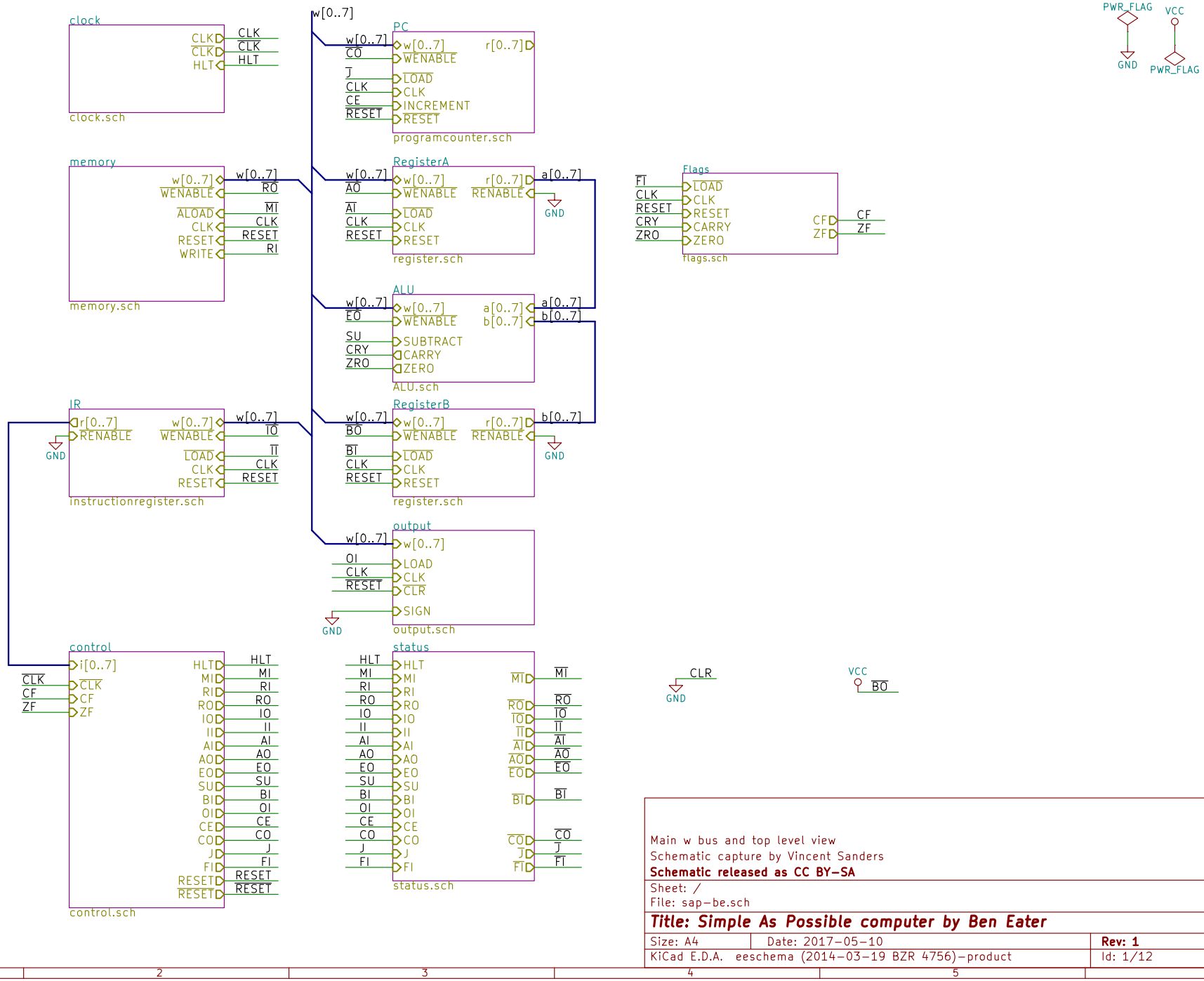
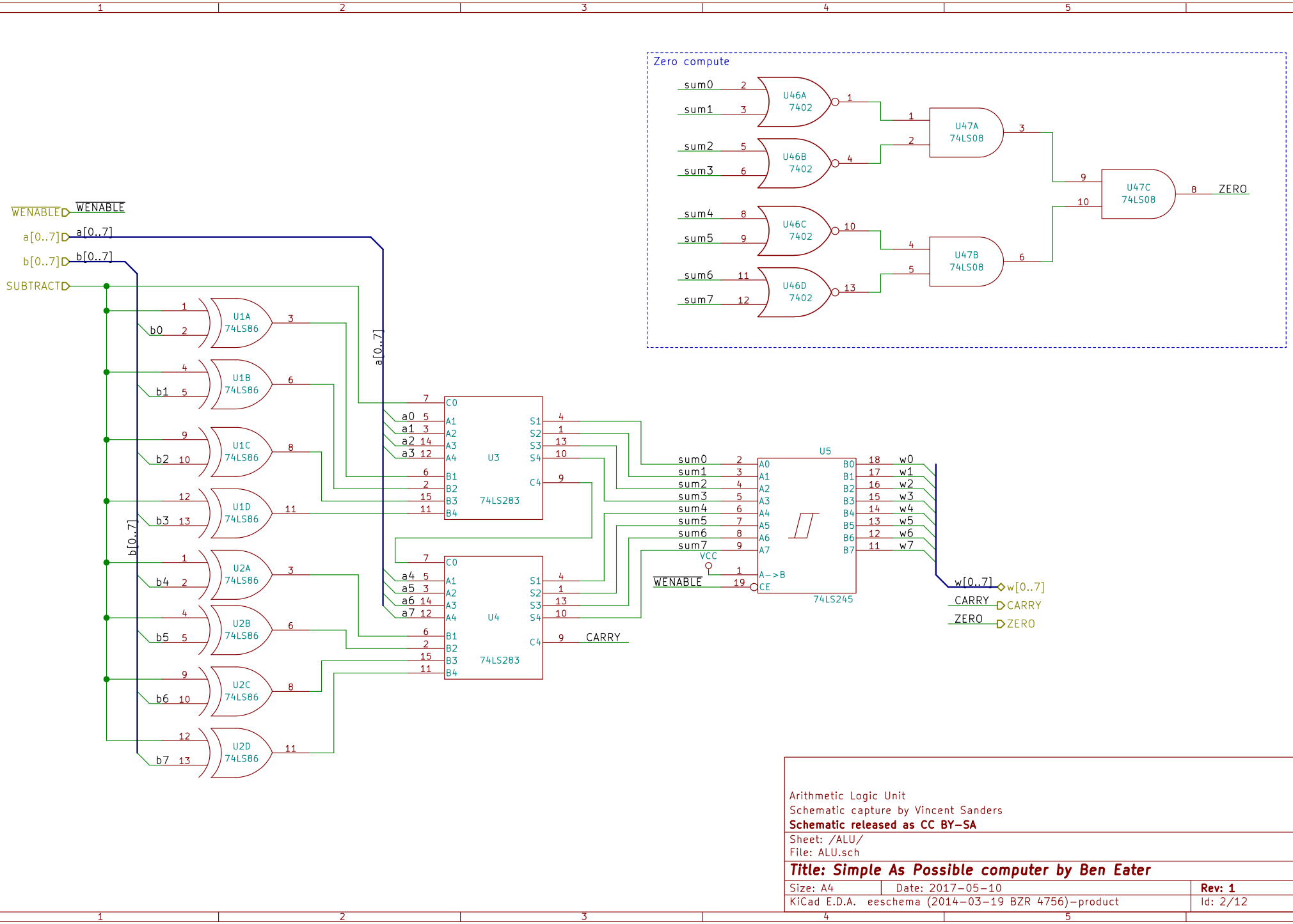
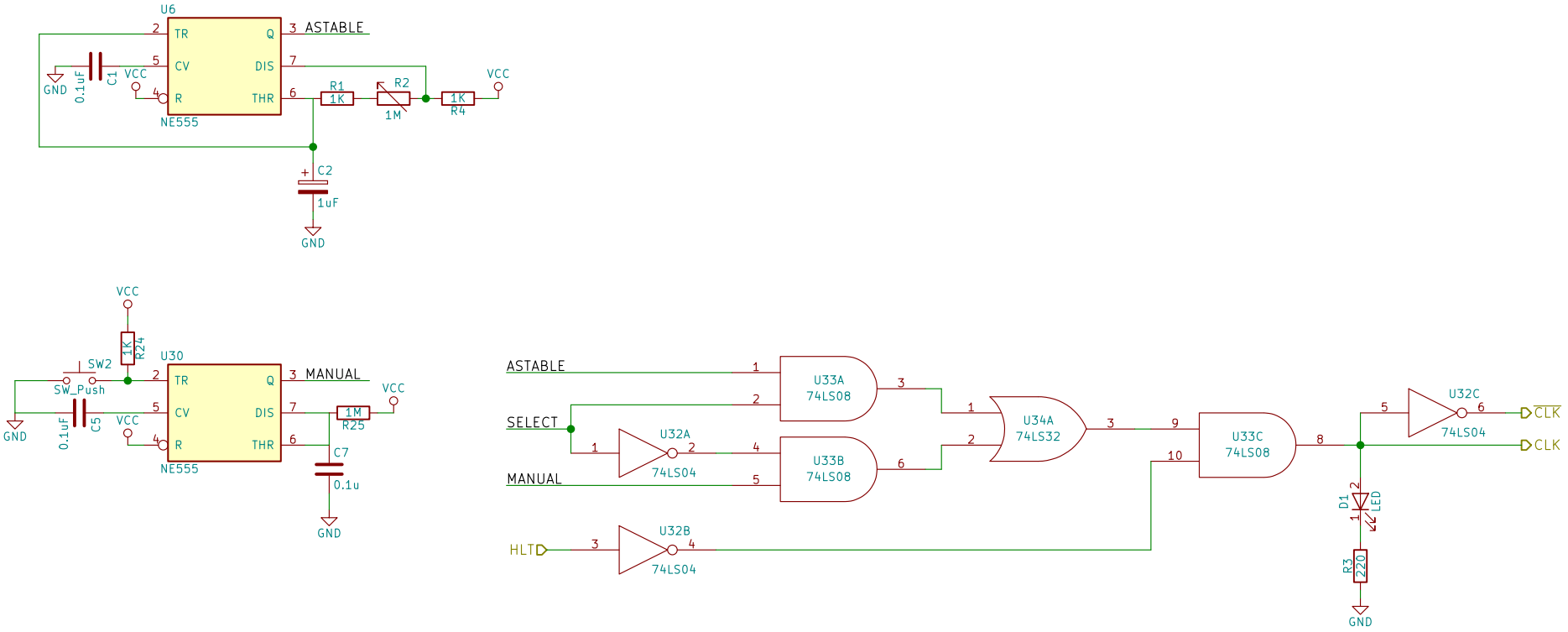

clock
CLK
CLK
HLT
clock.sch
w[0..7]
PC
w[0..7]
CO
J
CLK
CE
RESET
r[0..7]
WENABLE
LOAD
CLK
INCREMENT
RESET
programcounter.sch
memory
w[0..7]
WENABLE
ALOAD
CLK
RESET
WRITE
RO
MI
CLK
RESET
RI
memory.sch
RegisterA
AO
AI
CLK
RESET
RENABLE
a[0..7]
register.sch
Flags
FI
CLK
RESET
CRY
ZRO
LOAD
CARRY
ZERO
CF
ZF
flags.sch
ALU
EO
SU
CRY
ZRO
SUBTRACT
CARRY
ZERO
b[0..7]
ALU.sch
IR
r[0..7]
RENABLE
IO
II
instructionregister.sch
RegisterB
BO
BI
register.sch
output
OI
SIGN
output.sch
GND
PWR_FLAG
VCC
control
i[0..7]
HLT
MI
RI
RO
IO
II
AI
AO
EO
SU
BI
OI
CE
CO
J
FI
control.sch
status
status.sch
CLR
Main w bus and top level view
Schematic capture by Vincent Sanders
Schematic released as CC BY-SA
Sheet: /
File: sap-be.sch
Title: Simple As Possible computer by Ben Eater
Size: A4
Date: 2017-05-10
Rev: 1
KiCad E.D.A. eeschema (2014-03-19 BZR 4756)-product
Id: 1/12


Zero compute
sum0
sum1
sum2
sum3
sum4
sum5
sum6
sum7
U46A 7402
U46B 7402
U46C 7402
U46D 7402
U47A 74LS08
U47B 74LS08
U47C 74LS08
ZERO
WENABLE
a[0..7]
b[0..7]
SUBTRACT
U1A 74LS86
U1B 74LS86
U1C 74LS86
U1D 74LS86
U2A 74LS86
U2B 74LS86
U2C 74LS86
U2D 74LS86
b0
b1
b2
b3
b4
b5
b6
b7
U3 74LS283
U4 74LS283
C0
C4
CARRY
U5 74LS245
A->B
CE
VCC
w0
w1
w2
w3
w4
w5
w6
w7
w[0..7]
CARRY
ZERO
Arithmetic Logic Unit
Schematic capture by Vincent Sanders
Schematic released as CC BY-SA
Sheet: /ALU/
File: ALU.sch
Title: Simple As Possible computer by Ben Eater
Size: A4
Date: 2017-05-10
Rev: 1
KiCad E.D.A. eeschema (2014-03-19 BZR 4756)-product
Id: 2/12

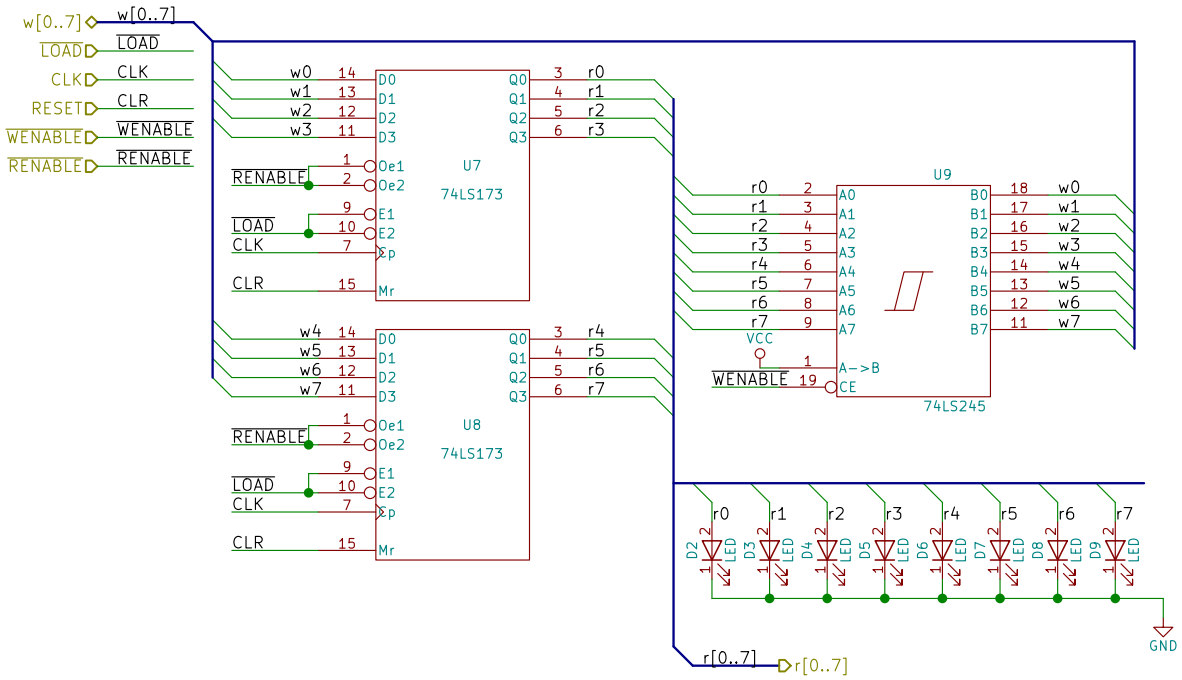


Clock generation with manual step and halt
Schematic capture by Vincent Sanders
Schematic released as CC BY-SA

Sheet: /clock/
File: clock.sch

Title: Simple As Possible computer by Ben Eater

Size: A4	Date: 2017-05-10	**Rev: 1**
KiCad E.D.A. eeschema (2014-03-19 BZR 4756)-product		Id: 3/12



Schematic capture by Vincent Sanders

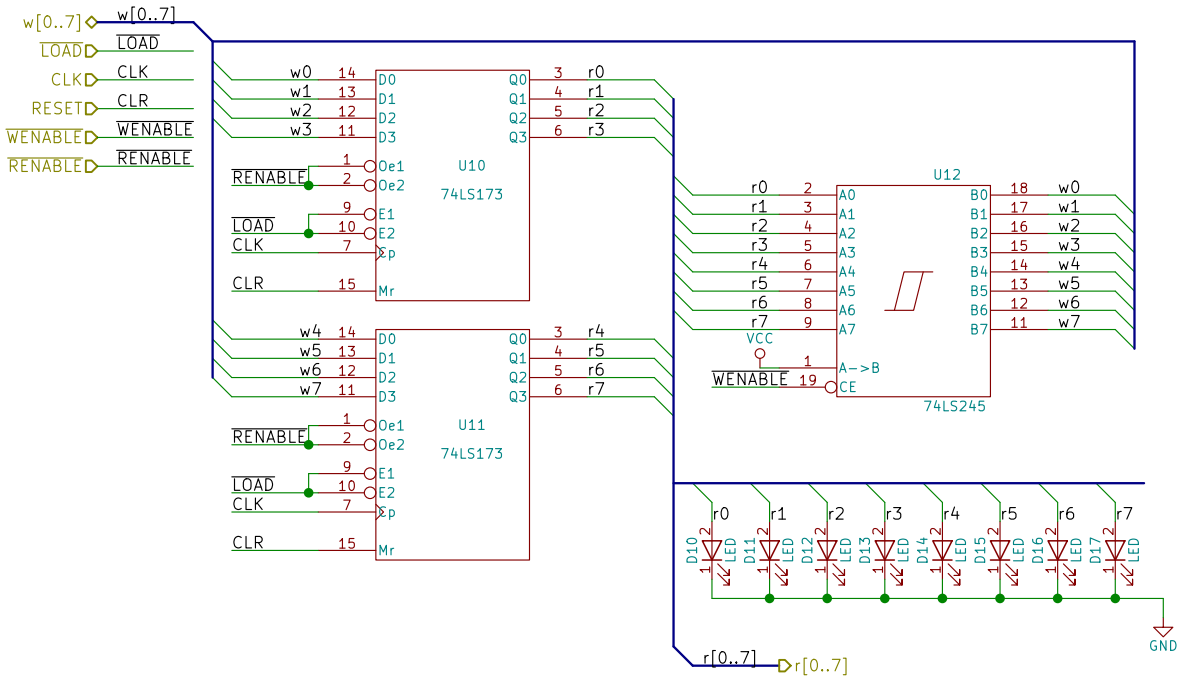
Schematic released as CC BY-SA

Sheet: /RegisterB/

File: register.sch

Title: Simple As Possible computer by Ben Eater

Size: A4	Date: 2017-05-10	**Rev: 1**
KiCad E.D.A. eeschema (2014-03-19 BZR 4756)-product		Id: 4/12



Schematic capture by Vincent Sanders

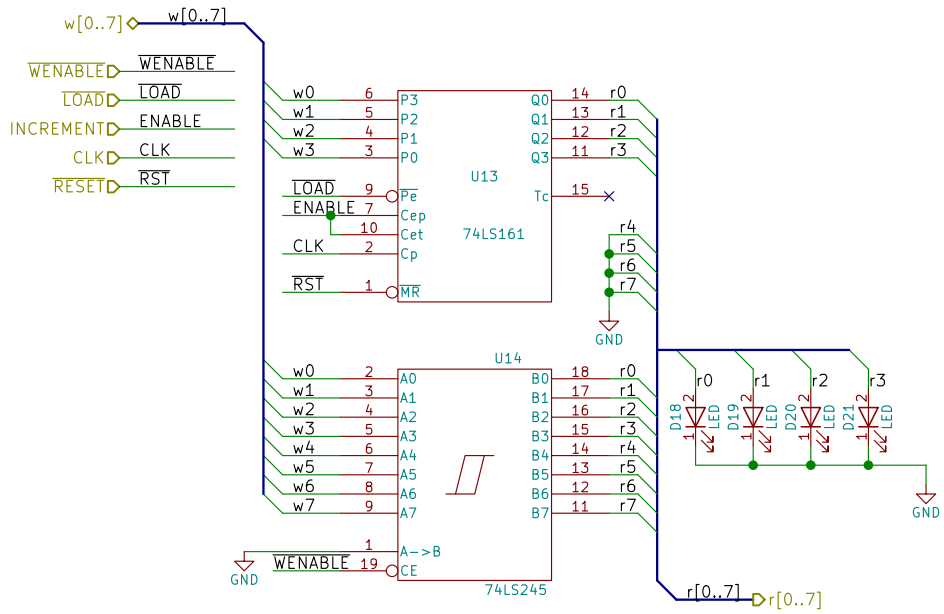
Schematic released as CC BY-SA

Sheet: /RegisterA/

File: register.sch

Title: Simple As Possible computer by Ben Eater

Size: A4	Date: 2017-05-10	**Rev: 1**
KiCad E.D.A. eeschema (2014-03-19 BZR 4756)-product		Id: 5/12

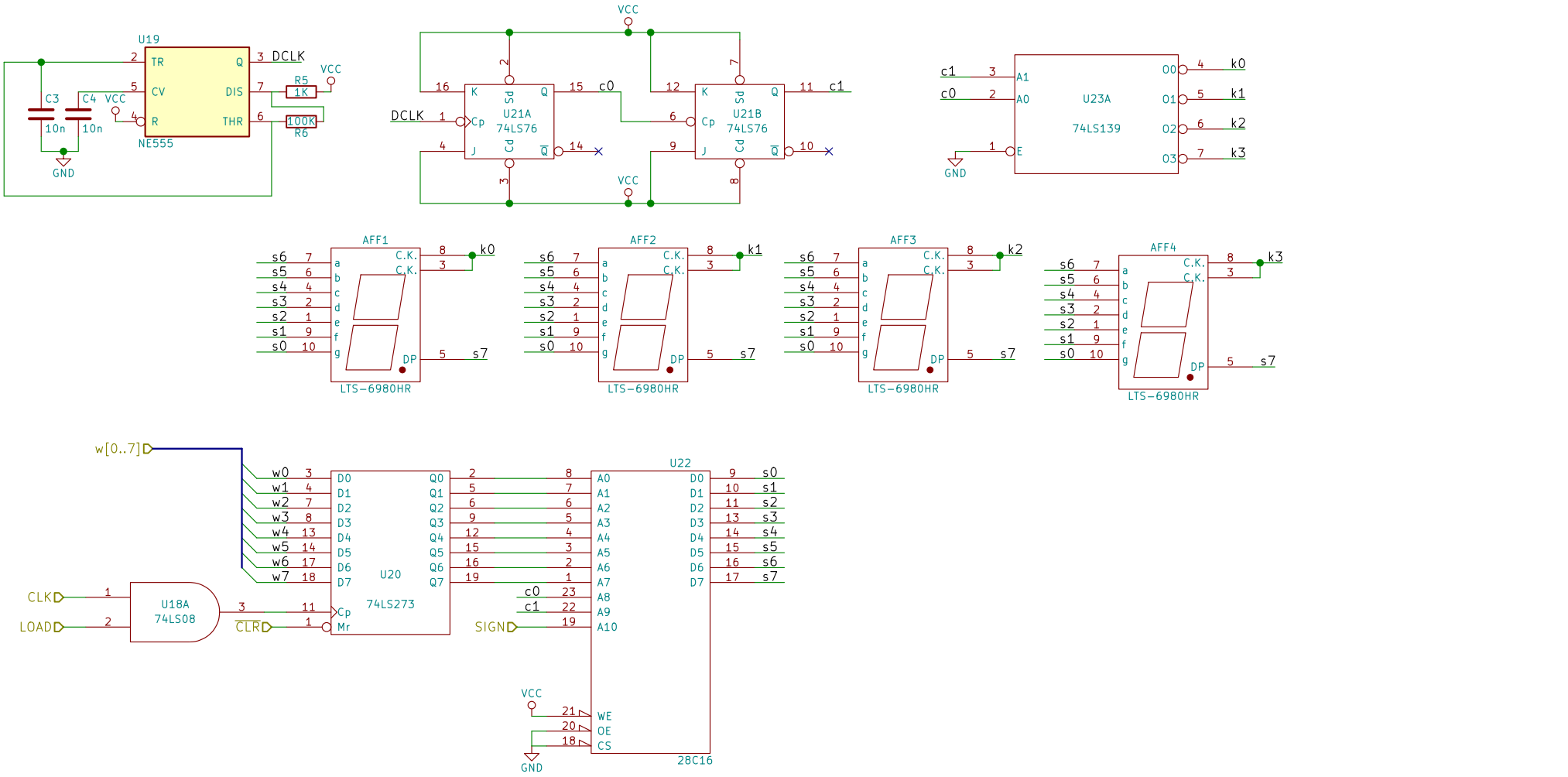


Program counter
Schematic capture by Vincent Sanders
Schematic released as CC BY-SA

Sheet: /PC/
File: programcounter.sch

Title: Simple As Possible computer by Ben Eater

Size: A4	Date: 2017-05-10	**Rev: 1**
KiCad E.D.A. eeschema (2014-03-19 BZR 4756)-product		Id: 6/12

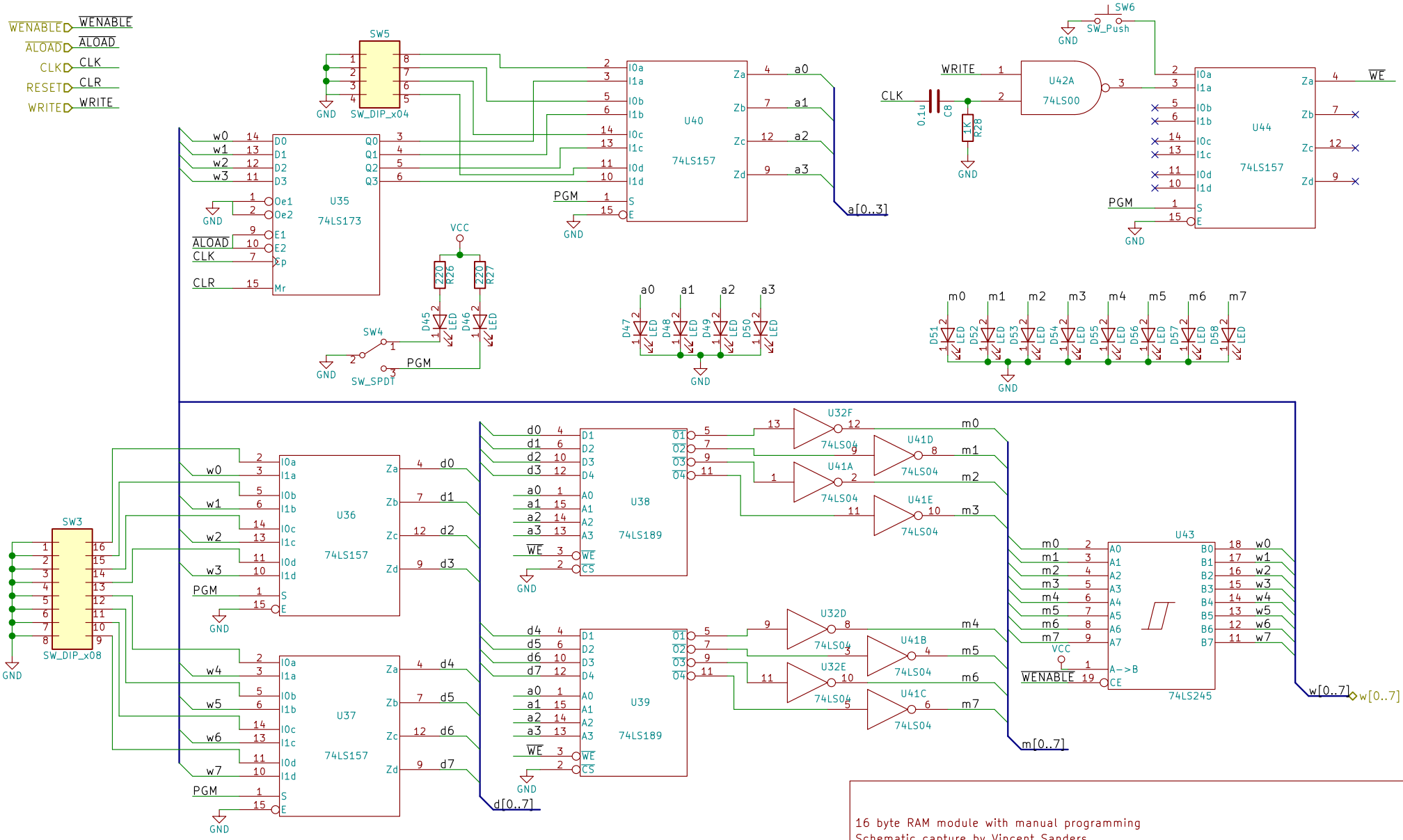


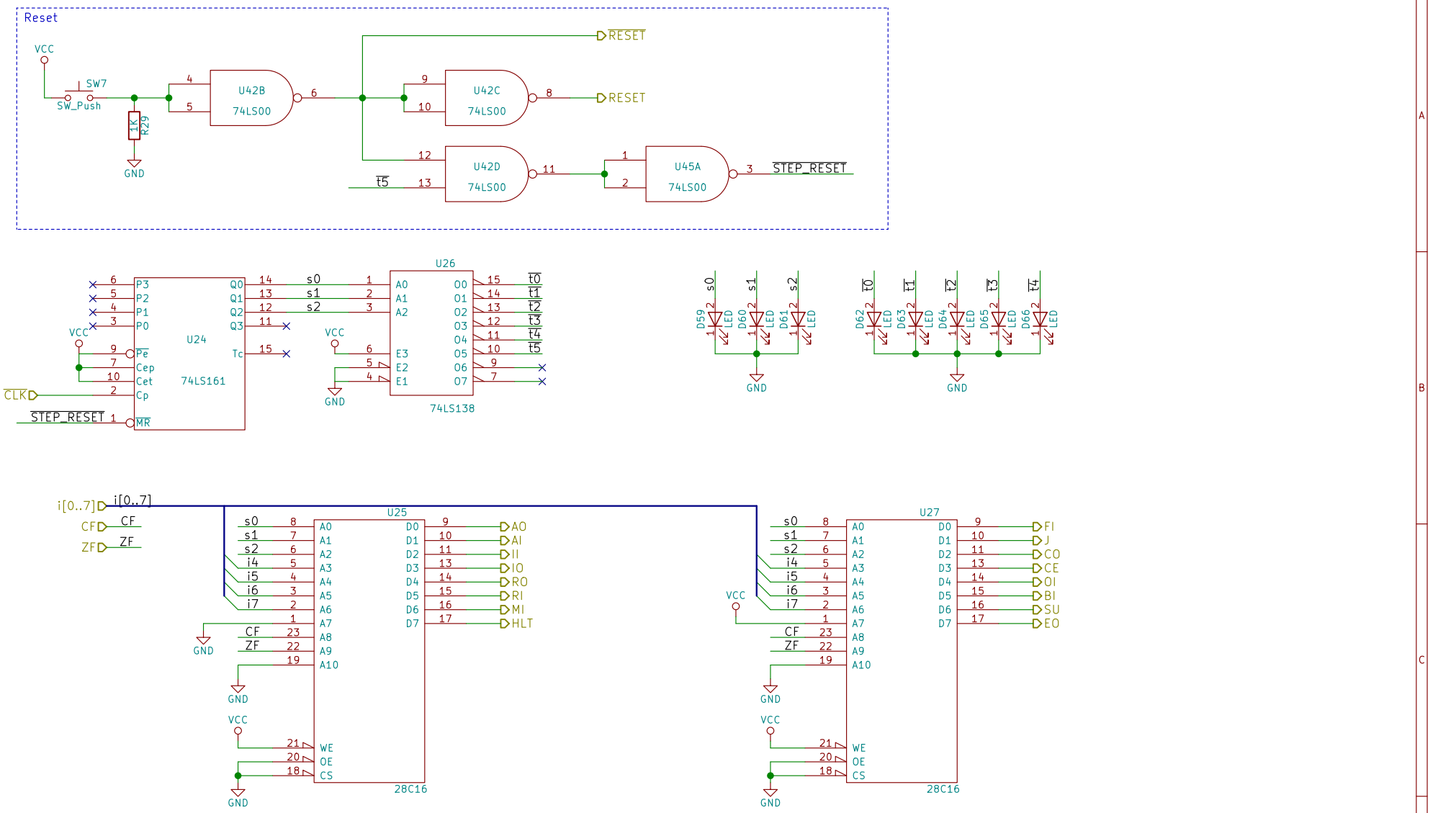
7 segment output register
Schematic capture by Vincent Sanders
Schematic released as CC BY-SA

Sheet: /output/
File: output.sch

Title: Simple As Possible computer by Ben Eater

Size: A4	Date: 2017-05-10	**Rev: 1**
KiCad E.D.A. eeschema (2014-03-19 BZR 4756)-product		Id: 7/12


WENABLE
ALOAD
CLK
RESET
WRITE
SW5
SW_DIP_x04
U40
74LS157
U35
74LS173
SW6
SW_Push
U42A
74LS00
U44
SW4
SW_SPDT
PGM
VCC
a[0..3]
SW3
SW_DIP_x08
U36
U37
U38
U39
74LS189
U32F
U41D
U41A
U41E
U32D
U32E
U41B
U41C
74LS04
U43
74LS245
d[0..7]
m[0..7]
w[0..7]
16 byte RAM module with manual programming
Schematic capture by Vincent Sanders
Schematic released as CC BY-SA
Sheet: /memory/
File: memory.sch
Title: Simple As Possible computer by Ben Eater
Size: A4
Date: 2017-05-10
Rev: 1
KiCad E.D.A. eeschema (2014-03-19 BZR 4756)-product
Id: 8/12

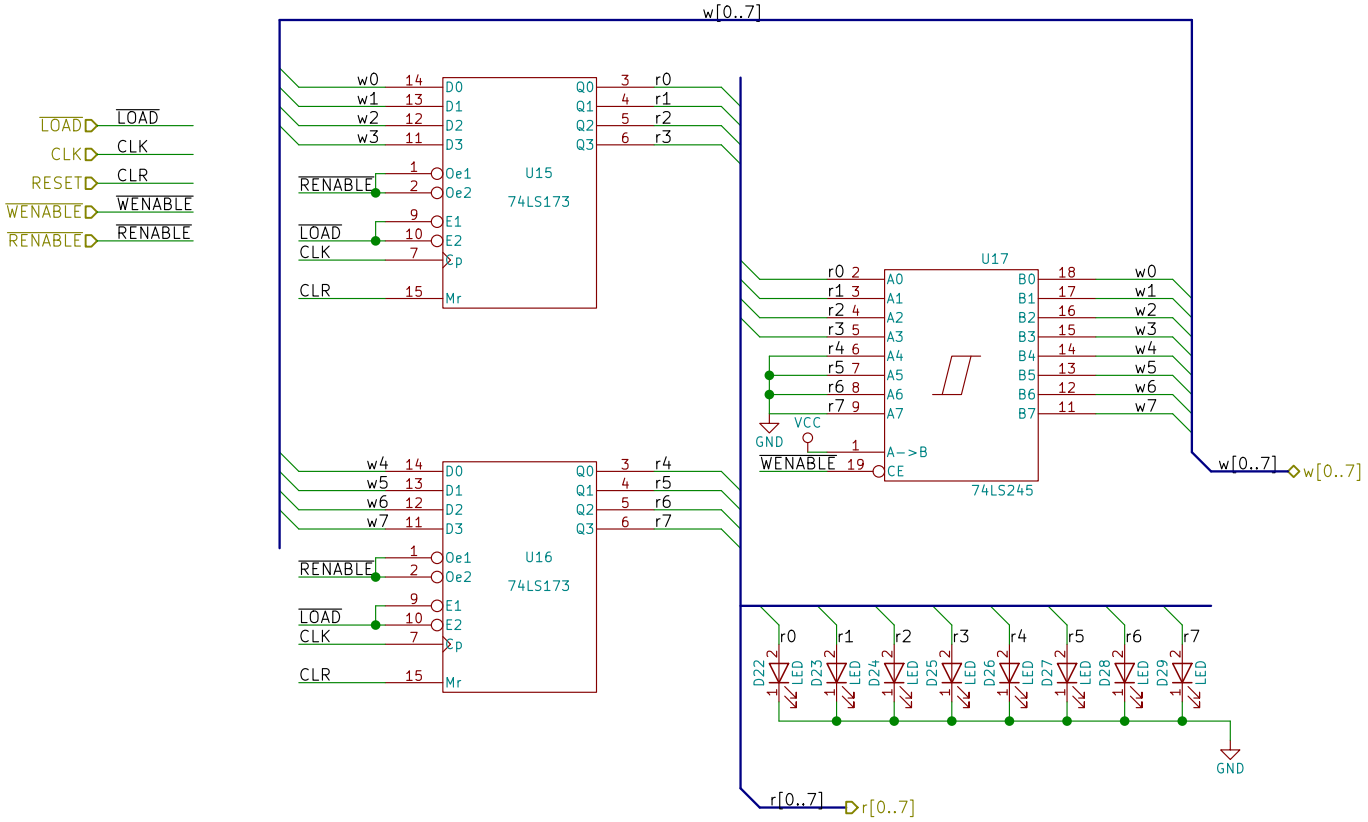


Control
Schematic capture by Vincent Sanders
Schematic released as CC BY-SA

Sheet: /control/
File: control.sch

Title: Simple As Possible computer by Ben Eater

Size: A4	Date: 2017-05-10	**Rev: 1**
KiCad E.D.A. eeschema (2014-03-19 BZR 4756)-product		Id: 9/12



Instruction register

Schematic capture by Vincent Sanders

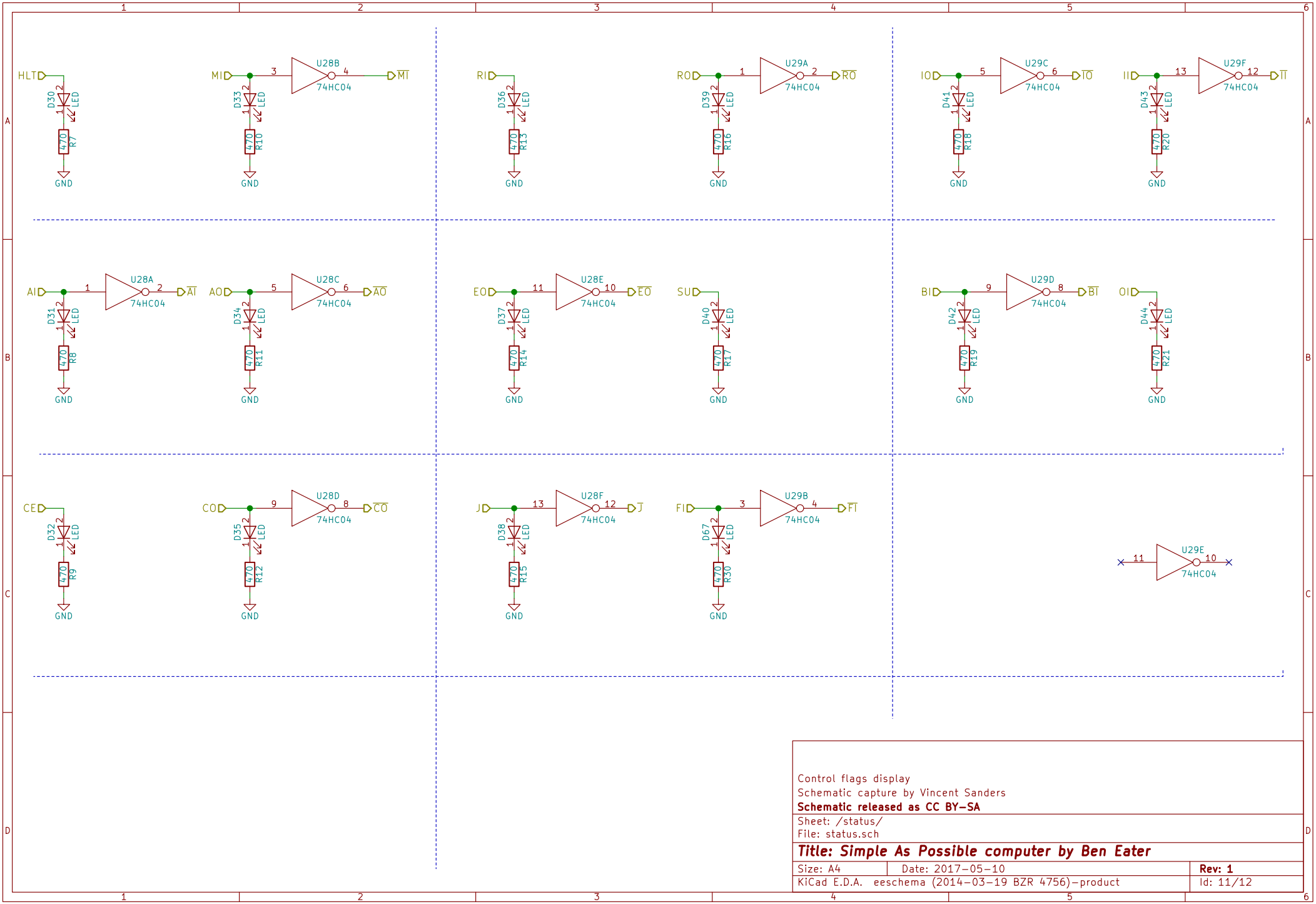
Schematic released as CC BY-SA

Sheet: /IR/

File: instructionregister.sch

Title: Simple As Possible computer by Ben Eater

Size: A4	Date: 2017-05-10	**Rev: 1**
KiCad E.D.A. eeschema (2014-03-19 BZR 4756)-product		Id: 10/12

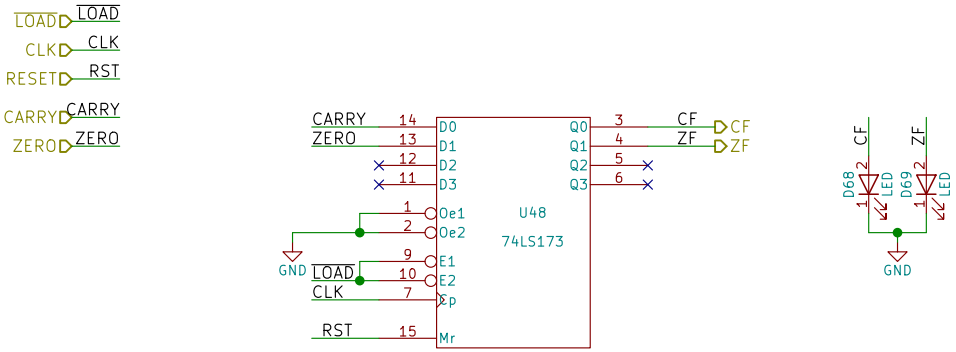


Control flags display
Schematic capture by Vincent Sanders
Schematic released as CC BY-SA

Sheet: /status/
File: status.sch

Title: Simple As Possible computer by Ben Eater

Size: A4	Date: 2017-05-10	**Rev: 1**
KiCad E.D.A. eeschema (2014-03-19 BZR 4756)-product		Id: 11/12



Flags register
Schematic capture by Vincent Sanders

Sheet: /Flags/
File: flags.sch

Title: Simple As Possible computer by Ben Eater

Size: A4	Date: 2017-05-10	**Rev: 1**
KiCad E.D.A. eeschema (2014-03-19 BZR 4756)-product		Id: 12/12