

Computer Engineering

Electronic and Communication Systems

Error correction code

Project Report

Federica Perrone

Summary

[Introduction 3](#_Toc91490875)

[Overview of Hamming Code 3](#_Toc91490876)

[General Algorithm 4](#_Toc91490877)

[Hamming Encoder 5](#_Toc91490878)

[Hamming Decoder 5](#_Toc91490879)

[Extended Hamming Code 5](#_Toc91490880)

[Applications 5](#_Toc91490881)

[Architecture description 6](#_Toc91490882)

[Encoder Architecture 7](#_Toc91490883)

[Decoder Architecture 7](#_Toc91490884)

[Error Injector 9](#_Toc91490885)

[VHDL Code 10](#_Toc91490886)

[Modules List 10](#_Toc91490887)

[ECC 10](#_Toc91490888)

[Encoder 12](#_Toc91490889)

[Decoder 13](#_Toc91490890)

[Test-plan 16](#_Toc91490891)

[Unit tests 16](#_Toc91490892)

[ECC 16](#_Toc91490893)

[Encoder 16](#_Toc91490894)

[Decoder 17](#_Toc91490895)

[Final test 20](#_Toc91490896)

[Synthesis 24](#_Toc91490897)

[RTL Analysis 24](#_Toc91490898)

[Timing Report 24](#_Toc91490899)

[Resource Utilization Report 25](#_Toc91490900)

[Power Consumption Report 25](#_Toc91490901)

[Warning Messages 25](#_Toc91490902)

[Conclusion 26](#_Toc91490903)

# Introduction

An error correcting code is an algorithm for expressing a sequence of numbers such that any errors, which are introduced, can be detected and corrected (within certain limitations) based on the remaining numbers.

The error correcting codes are used for controlling errors in data over unreliable or noisy communication channels.

The central idea is the sender encodes the message with redundant information in the form of an ECC. The redundancy allows the receiver to detect a limited number of errors that may occur anywhere in the message, and often to correct these errors without retransmission.

The two main categories of ECC codes are block codes and convolutional codes.

Hamming codes are a family of linear error-correcting block codes. Richard Hamming invented Hamming codes in 1950 as a way of automatically correcting errors introduced by punched card readers. The scheme invented by Hamming adds additional parity bits (k) to the information bits (n), and can self-detect and self-correct any single-event effect (SEE) error that occurs during transmission. Once the location of the error is identified and located, the code inverts the bit, returning it to its original form.

Hamming codes form the foundation of other more complex error correction schemes. The original scheme allows **single-error correction single-error detection** (**SECSED**), but with an addition of one parity bit, an extended Hamming version allows **single-error correction and double-error detection** (**SECDED**).

The extended Hamming code is popular in computer memory systems.

## Overview of Hamming Code

Hamming codes tend to follow the process illustrated in Figure 1. The input is errorless information of n-bits long which is sent to the encoder. The encoder then applies Hamming theorems, calculates the parity bits (k), and attaches them to the received information data, to form a codeword of (n + k)-bits. The processed information which contains additional parity bits is now ready for storage or transmission.

Figure 1- General layout of Hamming code

The decoder is responsible for checking and correcting any errors contained within the requested data. This is done by applying the Hamming theorem to calculate the syndrome. The decoder checks, locates, and corrects the errors contained in the codeword before extracting the new error-free information data.

### General Algorithm

As mentioned previously, Hamming code uses parity bits to perform error detection and correction. Bit position (codeword) is dependent on the amount of data bits protected. Parity bit positions are placed according to, 2 to the power of parity bit:

A general algorithm can be deduced from the following description:

1. Number the bits starting from 1: bit 1, 2, 3, 4, 5, 6, 7, etc.
2. Write the bit numbers in binary: 1, 10, 11, 100, 101, 110, 111, etc.
3. All bit positions that are powers of two (have a single 1 bit in the binary form of their position) are parity bits: 1, 2, 4, 8, etc. (1, 10, 100, 1000)
4. All other bit positions, with two or more 1 bits in the binary form of their position, are data bits.
5. Each data bit is included in a unique set of 2 or more parity bits, as determined by the binary form of its bit position:

* Parity bit 1 (P1) covers all bit positions which have the least significant bit set: bit 1 (the parity bit itself P1), 3, 5, 7, 9, etc. (all the odd numbers);
* Parity bit 2 (P2) covers all bit positions which have the second least significant bit set: bits 2 (P2), 3, 6, 7, 10, 11, etc. (sets of 2);
* Parity bit 4 (P4) covers all bit positions which have the third least significant bit set: bits 4 (P4), 5, 6, 7, 12, 13, 14, 15, etc. (sets of 4);
* Parity bit 8 (P8) covers all bit positions which have the fourth least significant bit set: bits 8 (P8), 9, 10, 11, 12, 13, 14, 15, etc. (sets of 8);
* Parity bit 16 (P16) covers all bit positions which have the fifth least significant bit set: bits 16 (P16), 17, 18, 19, 20, 21, 22, 23, etc. (sets of 16);

In the following table (Table 1), a typical codeword layout is shown.

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bit position | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |
| Encoded data bits | | **P1** | **P2** | **D1** | **P4** | **D2** | **D3** | **D4** | **P8** | **D5** | **D6** | **D7** | **D8** | **D9** | **D10** | **D11** | **P16** |
| Encoded data coverage | **P1** |  |  | ✓ |  | ✓ |  | ✓ |  | ✓ |  | ✓ |  | ✓ |  | ✓ |  |
| **P2** |  |  | ✓ |  |  | ✓ | ✓ |  |  | ✓ | ✓ |  |  | ✓ | ✓ |  |
| **P4** |  |  |  |  | ✓ | ✓ | ✓ |  |  |  |  |  | ✓ | ✓ | ✓ |  |
| **P8** |  |  |  |  |  |  |  |  | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |  |
| **P16** | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |

Table 1- bit layout of Hamming code

The layout makes each column have a unique parity bit combination, for each bit position. This unique parity bit combination in known as the syndrome value. The syndrome allows errors to be located and corrected.

### Hamming Encoder

Figure 2 - Encoder block diagram

n

Encoder

n+k

The Hamming encoder is responsible for generating the codeword (n + k - bits long) from the information bits. Once generated the codeword contains both the information bits and parity bits. The codeword is calculated as shown in the following figure (Figure 3).

Figure 3 - Graphical expression of Hamming encoder

Information bits (n-bits)

XOR gate

Codeword (n+ k-bits)

### Hamming Decoder

Figure 4 - Decoder block diagram

n+k

Decoder

n

The Hamming decoder is responsible for generating the syndrome (k-bits long) from the codeword (n +k -bits long). Once generated, the syndrome contains the error pattern that allows the error to be located and corrected. The syndrome is calculated as shown in the following figure (Figure 5).

Codeword (n + k-bits)

XOR gate

Syndrome (k-bits)

Figure 5 - Graphical expression of Hamming decoder

### Extended Hamming Code

The extended Hamming code makes use of an additional parity bit, which increases the Hamming code capabilities to SECDED.

In Table 1, P16 is the added parity bit that allows double error detection.

## Applications

The Error Correcting Codes (ECC), and more specifically Hamming codes, are used in many applications, such us:

* Telecommunication industry;
* Computer memory, modems and embedded processors;
* Nano Satellites.

# Architecture description

In this chapter will be discussed deeply the architecture of the Error Correcting Code (ECC).

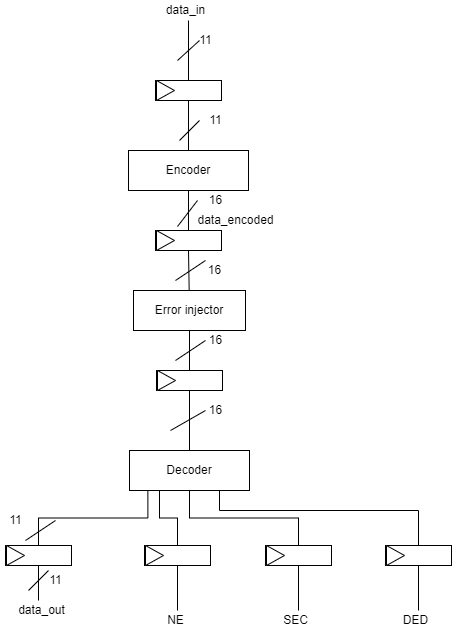
The general structure could be summarized by the following schema (Figure 6):

Figure 6 - General schema

## Encoder Architecture

As shown in Figure 7, the data word (11 bits long) is applied as an input to the encoder circuit, which performs XOR operations on the given data word and thus the required parity bits (5 bits long) are generated. In this way, the output bits of the encoder consist 16 bits, i.e. 11-bits of data (from D1 to D11) and 5-bits of parity (P1, P2, P4, P8, P16).

Figure 7 - Encoder block diagram

The 5 parity bits, for 11 data bits, are calculated as follows:

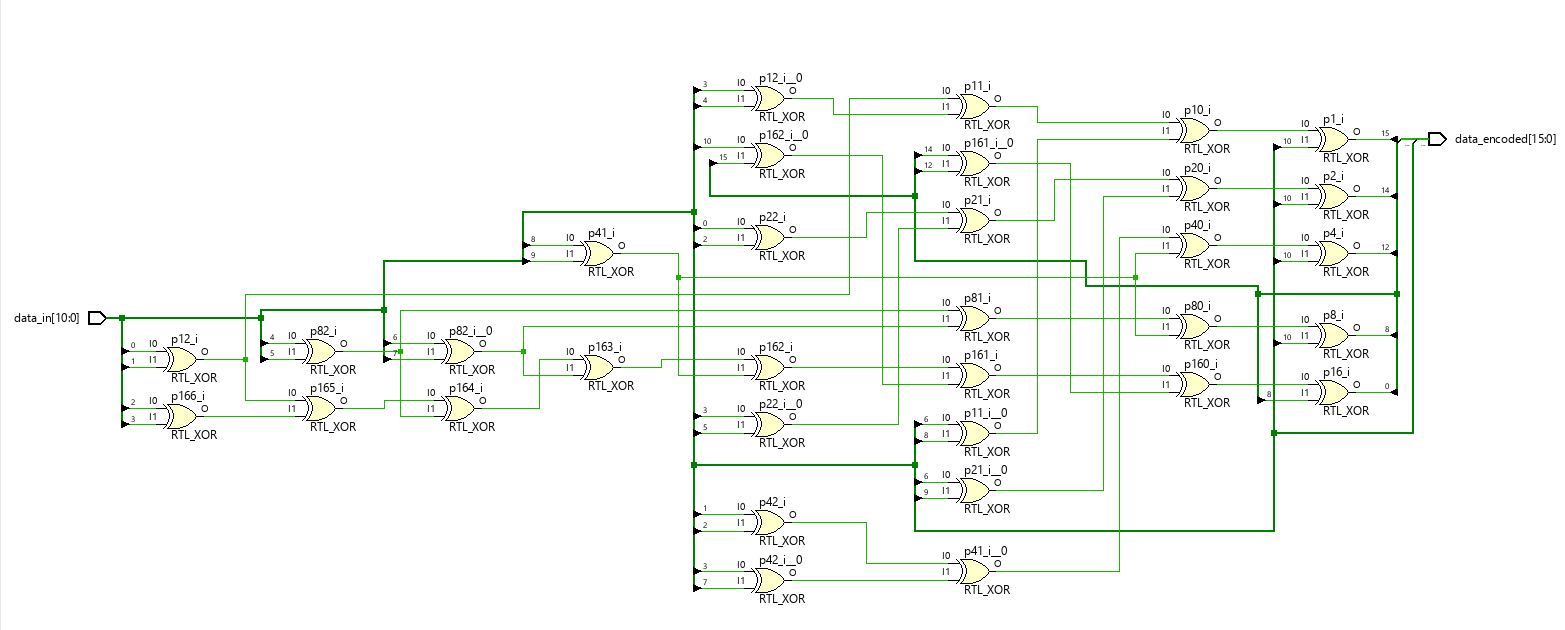
The following figure (Figure 8) shows the encoder circuit:

Figure 8 - Encoder circuit

## Decoder Architecture

The decoder must be able to detect a double error and correct a single error (SECDED 🡪single error correction, double error detection).

As shown in Figure 9, the decoder has the code word as input (16-bits long) and outputs the original word (possibly correct) (11-bits long), a NE bit indicating that there was no error, a SEC bit indicating single correct error and a DED bit indicating double error detection.

Figure 9 - Decoder block diagram

In order to correct a single error and detect a double error the decoder must calculate control bits as follows:

In general, the can be the following four cases:

1. C=0 and P=0 🡪 No error occurred, so the code word is taken as valid information;
2. C≠0 and P=1 🡪 A single bit error occurred that can be detected and corrected;
3. C≠0 and P=0 🡪 Double bit error occurred that can be detected, but cannot be corrected, so the code word is taken as invalid information;
4. C=0 and P=1 🡪 A single bit error occurred in the bit P16, that can be detected and corrected.

In the first case, since there was not no error, the output bit NE is set to 1.

In the second case, it is necessary to find the position of the wrong bit so that it can be corrected. Looking at C as a 4-bits word, its decimal decoding gives us exactly the position of the wrong bit. In this way, it is possible to flip the wrong bit and to output the corrected word. Furthermore, the output bit SEC is set to 1.

In the third case, since there was double bit error, the output bit DED is set to 1.

In the fourth case, the correction of the wrong bit is easy, because we know already the wrong bit, that is P16. As in the second case, also in this case the output bit SEC is set to 1.

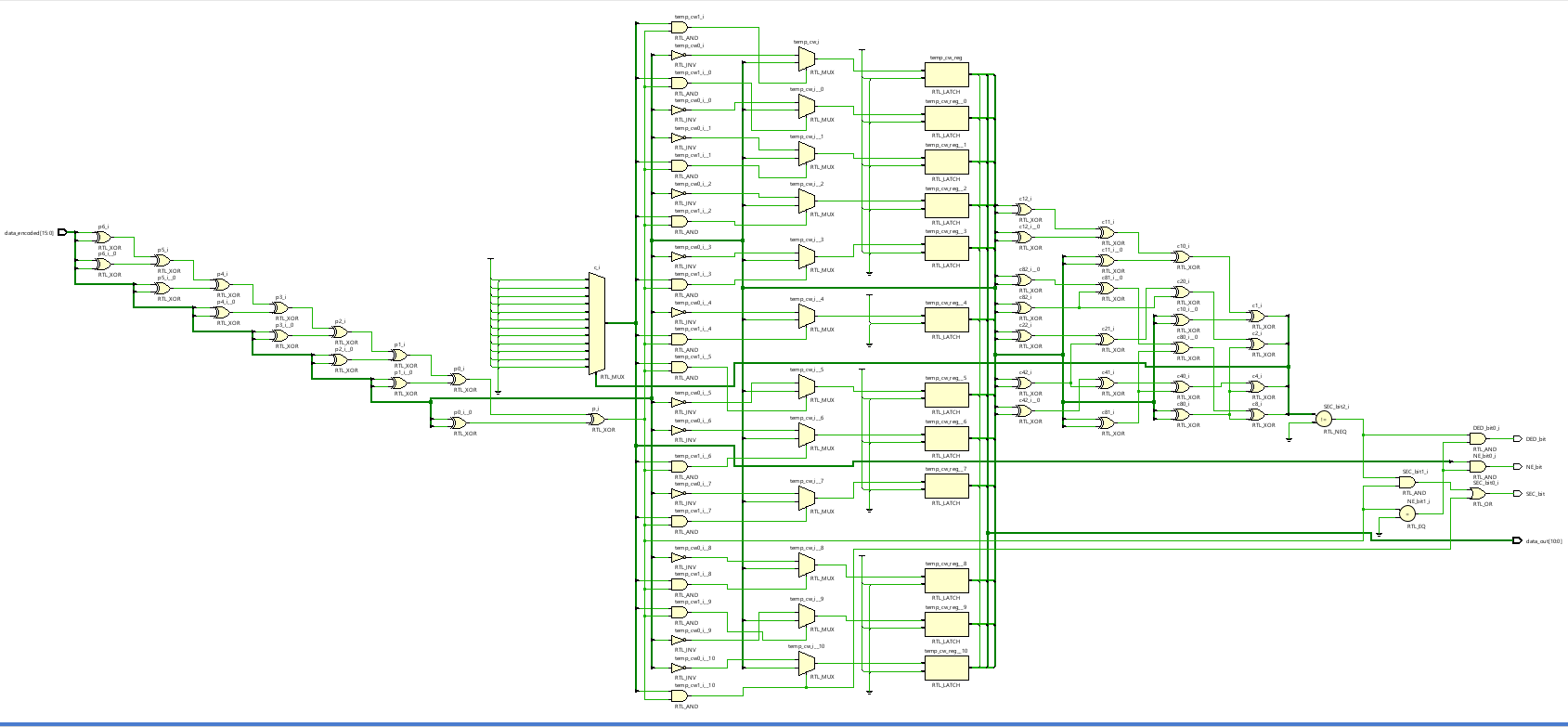
The following figure (Figure 10) shows the decoder circuit:

Figure 10 - Decoder circuit

## Error Injector

The Error injector is implemented by flipping the bits of the code word on the flow, in the testbench. In this way, the behavior of an unreliable transmission channel or a storage is simulated.

# VHDL Code

In this chapter will be presented the main modules that compose the architecture of the **Error Correcting Code** (**ECC**).

## Modules List

The following modules were created:

* ECC
  + Encoder
  + Decoder
  + DFF\_N

A **bottom-up strategy** was followed in order to build up the architecture.

## ECC

The main hardware description of the architecture. This module will connect all the other modules in order to create the correct architecture.

**library** ieee**;**

**use** ieee**.**std\_logic\_1164**.all;**

**entity** ECC **is**

**port(**

clk **:** **in** std\_logic**;**

resetn **:** **in** std\_logic**;**

data\_in **:** **in** std\_logic\_vector**(**10 **downto** 0**);**

data\_out **:** **out** std\_logic\_vector**(**10 **downto** 0**);**

NE\_bit **:** **out** std\_logic**;**

SEC\_bit **:** **out** std\_logic**;**

DED\_bit **:** **out** std\_logic

**);**

**end** ECC**;**

**architecture** beh **of** ECC **is**

**signal** output\_inputreg **:** std\_logic\_vector**(**10 **downto** 0**);**

**signal** output\_encoder **:** std\_logic\_vector**(**15 **downto** 0**);**

**signal** output\_encoder\_reg **:** std\_logic\_vector**(**15 **downto** 0**);**

**signal** output\_decoder\_data **:** std\_logic\_vector**(**10 **downto** 0**);**

**signal** output\_decoder\_NE **:** std\_logic\_vector**(**0 **downto** 0**);**

**signal** output\_decoder\_SEC **:** std\_logic\_vector**(**0 **downto** 0**);**

**signal** output\_decoder\_DED **:** std\_logic\_vector**(**0 **downto** 0**);**

**signal** output\_decoderreg\_data **:** std\_logic\_vector**(**10 **downto** 0**);**

**signal** output\_decoderreg\_NE **:** std\_logic\_vector**(**0 **downto** 0**);**

**signal** output\_decoderreg\_SEC **:** std\_logic\_vector**(**0 **downto** 0**);**

**signal** output\_decoderreg\_DED **:** std\_logic\_vector**(**0 **downto** 0**);**

**component** Encoder **is**

**port(**

data\_in **:** **in** std\_logic\_vector**(**10 **downto** 0**);**

data\_encoded **:** **out** std\_logic\_vector**(**15 **downto** 0**)**

**);**

**end** **component** Encoder**;**

**component** Decoder **is**

**port(**

data\_encoded **:** **in** std\_logic\_vector**(**15 **downto** 0**);**

data\_out **:** **out** std\_logic\_vector**(**10 **downto** 0**);**

NE\_bit **:** **out** std\_logic**;**

SEC\_bit **:** **out** std\_logic**;**

DED\_bit **:** **out** std\_logic

**);**

**end** **component** Decoder**;**

**component** DFF\_N **is**

**generic(** N **:** natural **:=** 8**);**

**port(**

clk **:** **in** std\_logic**;**

a\_rstn **:** **in** std\_logic**;**

en **:** **in** std\_logic**;**

d **:** **in** std\_logic\_vector**(**N **-** 1 **downto** 0**);**

q **:** **out** std\_logic\_vector**(**N **-** 1 **downto** 0**)**

**);**

**end** **component** DFF\_N**;**

**begin**

--register for data\_in bit

input\_reg**:** DFF\_N

**generic** **map(** N **=>** 11**)**

**port** **map(**

clk **=>** clk**,**

a\_rstn **=>** resetn**,**

en **=>** '1'**,**

d **=>** data\_in**,**

q **=>** output\_inputreg

**);**

--encoder

encoder\_block**:** Encoder

**port** **map(**

data\_in **=>** output\_inputreg**,**

data\_encoded **=>** output\_encoder

**);**

--register for output of the encoder

out\_encoder\_reg**:** DFF\_N

**generic** **map(** N **=>** 16**)**

**port** **map(**

clk **=>** clk**,**

a\_rstn **=>** resetn**,**

en **=>** '1'**,**

d **=>** output\_encoder**,**

q **=>** output\_encoder\_reg

**);**

--decoder

decoder\_block**:** Decoder

**port** **map(**

data\_encoded **=>** output\_encoder\_reg**,**

data\_out **=>** output\_decoder\_data**,**

NE\_bit **=>** output\_decoder\_NE**(**0**),**

SEC\_bit **=>** output\_decoder\_SEC**(**0**),**

DED\_bit **=>** output\_decoder\_DED**(**0**)**

**);**

--register for output of the decoder (data)

out\_decoder\_reg\_data**:** DFF\_N

**generic** **map(** N **=>** 11**)**

**port** **map(**

clk **=>** clk**,**

a\_rstn **=>** resetn**,**

en **=>** '1'**,**

d **=>** output\_decoder\_data**,**

q **=>** output\_decoderreg\_data

**);**

data\_out **<=** output\_decoderreg\_data**;**

--register for output of the decoder (NE)

out\_decoder\_reg\_NE**:** DFF\_N

**generic** **map(** N **=>** 1**)**

**port** **map(**

clk **=>** clk**,**

a\_rstn **=>** resetn**,**

en **=>** '1'**,**

d **=>** output\_decoder\_NE**,**

q **=>** output\_decoderreg\_NE

**);**

NE\_bit **<=** output\_decoderreg\_NE**(**0**);**

--register for output of the decoder (SEC)

out\_decoder\_reg\_SEC**:** DFF\_N

**generic** **map(** N **=>** 1**)**

**port** **map(**

clk **=>** clk**,**

a\_rstn **=>** resetn**,**

en **=>** '1'**,**

d **=>** output\_decoder\_SEC**,**

q **=>** output\_decoderreg\_SEC

**);**

SEC\_bit **<=** output\_decoderreg\_SEC**(**0**);**

--register for output of the decoder (DED)

out\_decoder\_reg\_DED**:** DFF\_N

**generic** **map(** N **=>** 1**)**

**port** **map(**

clk **=>** clk**,**

a\_rstn **=>** resetn**,**

en **=>** '1'**,**

d **=>** output\_decoder\_DED**,**

q **=>** output\_decoderreg\_DED

**);**

DED\_bit **<=** output\_decoderreg\_DED**(**0**);**

**end** beh**;**

## Encoder

This module has the task of creating the code word (16-bits long), having the 11-bits as input.

**library** ieee**;**

**use** ieee**.**std\_logic\_1164**.all;**

**entity** Encoder **is**

**port(**

data\_in **:** **in** std\_logic\_vector**(**10 **downto** 0**);**

data\_encoded **:** **out** std\_logic\_vector**(**15 **downto** 0**)**

**);**

**end** Encoder**;**

**architecture** beh **of** Encoder **is**

**signal** p1 **:** std\_logic**;**

**signal** p2 **:** std\_logic**;**

**signal** p4 **:** std\_logic**;**

**signal** p8 **:** std\_logic**;**

**signal** p16 **:** std\_logic**;**

**begin**

-- generation of parity bits

p1 **<=** data\_in**(**0**)** **xor** data\_in**(**1**)** **xor** data\_in**(**3**)** **xor** data\_in**(**4**)** **xor**

data\_in**(**6**)** **xor** data\_in**(**8**)** **xor** data\_in**(**10**);**

p2 **<=** data\_in**(**0**)** **xor** data\_in**(**2**)** **xor** data\_in**(**3**)** **xor** data\_in**(**5**)** **xor**

data\_in**(**6**)** **xor** data\_in**(**9**)** **xor** data\_in**(**10**);**

p4 **<=** data\_in**(**1**)** **xor** data\_in**(**2**)** **xor** data\_in**(**3**)** **xor** data\_in**(**7**)** **xor**

data\_in**(**8**)** **xor** data\_in**(**9**)** **xor** data\_in**(**10**);**

p8 **<=** data\_in**(**4**)** **xor** data\_in**(**5**)** **xor** data\_in**(**6**)** **xor** data\_in**(**7**)** **xor**

data\_in**(**8**)** **xor** data\_in**(**9**)** **xor** data\_in**(**10**);**

-- generation of extra parity bit

p16 **<=** data\_in**(**0**)** **xor** data\_in**(**1**)** **xor** data\_in**(**2**)** **xor** data\_in**(**3**)** **xor**

data\_in**(**4**)** **xor** data\_in**(**5**)** **xor** data\_in**(**6**)** **xor** data\_in**(**7**)** **xor**

data\_in**(**8**)** **xor** data\_in**(**9**)** **xor** data\_in**(**10**)** **xor** p1 **xor** p2 **xor**

p4 **xor** p8**;**

--set output bits

data\_encoded **<=** p16 **&** data\_in**(**10**)** **&** data\_in**(**9**)** **&** data\_in**(**8**)** **&** data\_in**(**7**)**

**&** data\_in**(**6**)** **&** data\_in**(**5**)** **&** data\_in**(**4**)** **&**p8 **&** data\_in**(**3**)**

**&** data\_in**(**2**)** **&** data\_in**(**1**)** **&** p4 **&** data\_in**(**0**)** **&** p2 **&** p1**;**

**end** beh**;**

## Decoder

This module has the task of decoding the code word. In more detail, it has the task of detecting a double bit error and correcting a single bit error.

**library** ieee**;**

**use** ieee**.**std\_logic\_1164**.all;**

**entity** Decoder **is**

**port(**

data\_encoded **:** **in** std\_logic\_vector**(**15 **downto** 0**);**

data\_out **:** **out** std\_logic\_vector**(**10 **downto** 0**);**

NE\_bit **:** **out** std\_logic**;**

SEC\_bit **:** **out** std\_logic**;**

DED\_bit **:** **out** std\_logic

**);**

**end** Decoder**;**

**architecture** beh **of** Decoder **is**

**signal** c1 **:** std\_logic**;**

**signal** c2 **:** std\_logic**;**

**signal** c4 **:** std\_logic**;**

**signal** c8 **:** std\_logic**;**

**signal** p **:** std\_logic**;**

**signal** c **:** std\_logic\_vector**(**3 **downto** 0**);**

**signal** temp\_cw **:** std\_logic\_vector**(**15 **downto** 0**);**

**begin**

--\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

-- ERROR DETECTION

--\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

-- generation of control bits

c1 **<=** **(**data\_encoded**(**0**)** **xor** data\_encoded**(**2**))** **xor** **(**data\_encoded**(**4**)** **xor**

data\_encoded**(**6**))** **xor** **(**data\_encoded**(**8**)** **xor** data\_encoded**(**10**))** **xor**

**(**data\_encoded**(**12**)** **xor** data\_encoded**(**14**));**

c2 **<=** **(**data\_encoded**(**1**)** **xor** data\_encoded**(**2**))** **xor** **(**data\_encoded**(**5**)** **xor**

data\_encoded**(**6**))** **xor** **(**data\_encoded**(**9**)** **xor** data\_encoded**(**10**))** **xor**

**(**data\_encoded**(**13**)** **xor** data\_encoded**(**14**));**

c4 **<=** **(**data\_encoded**(**3**)** **xor** data\_encoded**(**4**))** **xor** **(**data\_encoded**(**5**)** **xor**

data\_encoded**(**6**))** **xor** **(**data\_encoded**(**11**)** **xor** data\_encoded**(**12**))** **xor**

**(**data\_encoded**(**13**)** **xor** data\_encoded**(**14**));**

c8 **<=** **(**data\_encoded**(**7**)** **xor** data\_encoded**(**8**))** **xor** **(**data\_encoded**(**9**)** **xor**

data\_encoded**(**10**))** **xor** **(**data\_encoded**(**11**)** **xor** data\_encoded**(**12**))** **xor**

**(**data\_encoded**(**13**)** **xor** data\_encoded**(**14**));**

p **<=** **(**data\_encoded**(**0**)** **xor** data\_encoded**(**1**))** **xor** **(**data\_encoded**(**2**)** **xor**

data\_encoded**(**3**))** **xor** **(**data\_encoded**(**4**)** **xor** data\_encoded**(**5**))** **xor**

**(**data\_encoded**(**6**)** **xor** data\_encoded**(**7**))** **xor** **(**data\_encoded**(**8**)** **xor**

data\_encoded**(**9**))** **xor** **(**data\_encoded**(**10**)** **xor** data\_encoded**(**11**))** **xor**

**(**data\_encoded**(**12**)** **xor** data\_encoded**(**13**))** **xor** **(**data\_encoded**(**14**)** **xor**

data\_encoded**(**15**));**

c **<=** c8 **&** c4 **&** c2 **&** c1**;**

--\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

-- ERROR CORRECTION

--\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

-- when c=0 and p=1 there was an error in p16

temp\_cw**(**15**)** **<=** **not(**data\_encoded**(**15**))** **when** c**=**"0000" **and** p**=**'1' **else**

data\_encoded**(**15**);**

--it must be taken into account that the position of the bits in

data\_encoded is shifted by 1 as it goes from 0 to 15

--when c="1111" (15) there was an error in 14-bit

temp\_cw**(**14**)** **<=** **not(**data\_encoded**(**14**))** **when** c**=**"1111" **and** p**=**'1' **else**

data\_encoded**(**14**);**

--when c="1110" (14) there was an error in 13-bit

temp\_cw**(**13**)** **<=** **not(**data\_encoded**(**13**))** **when** c**=**"1110" **and** p**=**'1' **else**

data\_encoded**(**13**);**

--when c="1101" (13) there was an error in 12-bit

temp\_cw**(**12**)** **<=** **not(**data\_encoded**(**12**))** **when** c**=**"1101" **and** p**=**'1' **else**

data\_encoded**(**12**);**

--when c="1100" (12) there was an error in 11-bit

temp\_cw**(**11**)** **<=** **not(**data\_encoded**(**11**))** **when** c**=**"1100" **and** p**=**'1' **else**

data\_encoded**(**11**);**

--when c="1011" (11) there was an error in 10-bit

temp\_cw**(**10**)** **<=** **not(**data\_encoded**(**10**))** **when** c**=**"1011" **and** p**=**'1' **else**

data\_encoded**(**10**);**

--when c="1010" (10) there was an error in 9-bit

temp\_cw**(**9**)** **<=** **not(**data\_encoded**(**9**))** **when** c**=**"1010" **and** p**=**'1' **else**

data\_encoded**(**9**);**

--when c="1001" (9) there was an error in 8-bit

temp\_cw**(**8**)** **<=** **not(**data\_encoded**(**8**))** **when** c**=**"1001" **and** p**=**'1' **else**

data\_encoded**(**8**);**

--when c="0111" (7) there was an error in 6-bit

temp\_cw**(**6**)** **<=** **not(**data\_encoded**(**6**))** **when** c**=**"0111" **and** p**=**'1' **else**

data\_encoded**(**6**);**

--when c="0110" (6) there was an error in 5-bit

temp\_cw**(**5**)** **<=** **not(**data\_encoded**(**5**))** **when** c**=**"0110" **and** p**=**'1' **else**

data\_encoded**(**5**);**

--when c="0101" (5) there was an error in 4-bit

temp\_cw**(**4**)** **<=** **not(**data\_encoded**(**4**))** **when** c**=**"0101" **and** p**=**'1' **else**

data\_encoded**(**4**);**

--when c="0011" (3) there was an error in 2-bit

temp\_cw**(**2**)** **<=** **not(**data\_encoded**(**2**))** **when** c**=**"0011" **and** p**=**'1' **else**

data\_encoded**(**2**);**

temp\_cw**(**7**)** **<=** data\_encoded**(**7**);**

temp\_cw**(**3**)** **<=** data\_encoded**(**3**);**

temp\_cw**(**1 **downto** 0**)** **<=** data\_encoded**(**1 **downto** 0**);**

--set outputs

data\_out **<=** temp\_cw**(**14 **downto** 8**)** **&** temp\_cw**(**6 **downto** 4**)** **&** temp\_cw**(**2**);**

NE\_bit **<=** '1' **when** c**=**"0000" **and** p**=**'0' **else** '0'**;**

SEC\_bit **<=** '1' **when** **(**c**/=**"0000" **and** p**=**'1'**)** **or** **(**c**=**"0000" **and** p**=**'1'**)** **else**

'0'**;**

DED\_bit **<=** '1' **when** c**/=**"0000" **and** p**=**'0' **else** '0'**;**

**end** beh**;**

# Test-plan

In order to verify the correctness of the system the following tests were made:

1. **Unit tests**: following the bottom-up strategy, each sub-module, after completing the implementation, has a dedicated testbench in order to check the correctness of the single sub-module in isolation.
2. A test with **two** **Device Under Test** (**DUT**): the encoder and the decoder. In this way, it was possible to insert errors on the flow in the decoder input.

## Unit tests

### ECC

The ECC testbench is not shown because it is not relevant, in fact what is given in input is returned in output (it is not possible to insert the errors in the decoder input due to how the ECC is structured).

In order to test the correct functioning of the overall architecture, it is necessary to do a testbench in which there are two Device Under Test (see later).

### Encoder

**library** ieee**;**

**use** ieee**.**std\_logic\_1164**.all;**

--entity declaration

**entity** Encoder\_tb **is**

**end** Encoder\_tb**;**

--architecture body

**architecture** rtl **of** Encoder\_tb **is**

**constant** clk\_period **:** time **:=** 8 ns**;**

**component** Encoder **is**

**port(**

data\_in **:** **in** std\_logic\_vector**(**10 **downto** 0**);**

data\_encoded **:** **out** std\_logic\_vector**(**15 **downto** 0**)**

**);**

**end** **component;**

**signal** clk **:** std\_logic **:=** '0'**;**

**signal** data\_in**:** std\_logic\_vector**(**10 **downto** 0**)** **:=** **(others** **=>**

'0'**);**

**signal** data\_encoded**:** std\_logic\_vector**(**15 **downto** 0**);**

**signal** testing **:** boolean **:=** true**;**

**begin**

clk **<=** **not** clk **after** clk\_period**/**2 **when** testing **else** '0'**;**

dut**:** Encoder

**port** **map(**

data\_in **=>** data\_in**,**

data\_encoded **=>** data\_encoded

**);**

stimulus **:** **process**

**begin**

data\_in **<=** **(others** **=>** '0'**);**

**wait** **for** 16 ns**;**

data\_in **<=** "01010101011"**;**

--expected output "0010101011010101" -> 10965

**wait** **for** 16 ns**;**

data\_in **<=** "11100011100"**;**

--expected output "1111000101101000" -> 61800

**wait** **for** 16 ns**;**

data\_in **<=** "10101010101"**;**

--expected output "0101010100101101" -> 21805

**wait** **for** 16 ns**;**

data\_in **<=** "00000000000"**;**

--expected output "0000000000000000" -> 0

**wait** **for** 16 ns**;**

data\_in **<=** "11111111111"**;**

--expected output "1111111111111111" -> 65535

**wait** **for** 16 ns**;**

**wait** **until** **rising\_edge(**clk**);**

testing **<=** false**;**

**end** **process;**

**end** rtl**;**

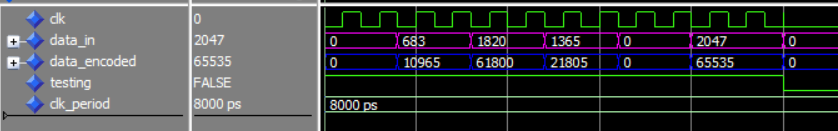
In the Figure 11 is shown the output of the encoder simulation obtained with Modelsim.

Figure 11 - Encoder simulation

### Decoder

**library** ieee**;**

**use** ieee**.**std\_logic\_1164**.all;**

--entity declaration

**entity** Decoder\_tb **is**

**end** Decoder\_tb**;**

--architecture body

**architecture** rtl **of** Decoder\_tb **is**

**constant** clk\_period **:** time **:=** 8 ns**;**

**component** Decoder **is**

**port(**

data\_encoded **:** **in** std\_logic\_vector**(**15 **downto** 0**);**

data\_out **:** **out** std\_logic\_vector**(**10 **downto** 0**);**

NE\_bit **:** **out** std\_logic**;**

SEC\_bit **:** **out** std\_logic**;**

DED\_bit **:** **out** std\_logic

**);**

**end** **Component;**

**signal** clk **:** std\_logic **:=** '0'**;**

**signal** data\_encoded**:** std\_logic\_vector**(**15 **downto** 0**)** **:=** **(others**

**=>** '0'**);**

**signal** data\_out**:** std\_logic\_vector**(**10 **downto** 0**);**

**signal** NE\_bit **:** std\_logic**;**

**signal** SEC\_bit **:** std\_logic**;**

**signal** DED\_bit **:** std\_logic**;**

**signal** testing **:** boolean **:=** true**;**

**begin**

clk **<=** **not** clk **after** clk\_period**/**2 **when** testing **else** '0'**;**

dut**:** Decoder

**port** **map(**

data\_encoded **=>** data\_encoded**,**

data\_out **=>** data\_out**,**

NE\_bit **=>** NE\_bit**,**

SEC\_bit **=>** SEC\_bit**,**

DED\_bit **=>** DED\_bit

**);**

stimulus **:** **process**

**begin**

data\_encoded **<=** **(others** **=>** '0'**);**

**wait** **for** 32 ns**;**

-- correct input-> "0010101011010101" (10965)

--assume that there was not an error

-- expected out -> data\_out= "01010101011" (683),

NE=1, SEC=DED=0

data\_encoded **<=** "0010101011010101"**;**

**wait** **for** 32 ns**;**

--assume that there was a single error in p16

-- expected out -> data\_out= "01010101011" (683),

NE=0, SEC=1, DED=0

data\_encoded **<=** "0010101011010100"**;**

**wait** **for** 32 ns**;**

--assume that there was a single error in d10

-- expected out -> data\_out= "01010101011" (683),

NE=0, SEC=1, DED=0

data\_encoded **<=** "0000101011010101"**;**

**wait** **for** 32 ns**;**

--assume that there was a single error in d11

-- expected out -> data\_out= "01010101011" (683),

NE=0, SEC=1, DED=0

data\_encoded **<=** "0110101011010101"**;**

**wait** **for** 32 ns**;**

--assume that there was a single error in d3

-- expected out -> data\_out= "01010101011" (683),

NE=0, SEC=1, DED=0

data\_encoded **<=** "0010101011110101"**;**

**wait** **for** 32 ns**;**

--assume that there was a single error in p8

-- expected out -> data\_out= "01010101011" (683),

NE=0, SEC=1, DED=0

data\_encoded **<=** "0010101001010101"**;**

**wait** **for** 32 ns**;**

--assume that there was a double error in p8 and d1

-- expected out -> data\_out=invalid info, NE=0, SEC=0,

DED=1

data\_encoded **<=** "0010101001010001"**;**

**wait** **for** 32 ns**;**

--assume that there was a double error in d10 and d9

-- expected out -> data\_out=invalid info, NE=0, SEC=0,

DED=1

data\_encoded **<=** "0010110011010101"**;**

**wait** **for** 32 ns**;**

**wait** **until** **rising\_edge(**clk**);**

testing **<=** false**;**

**end** **process;**

**end** rtl**;**

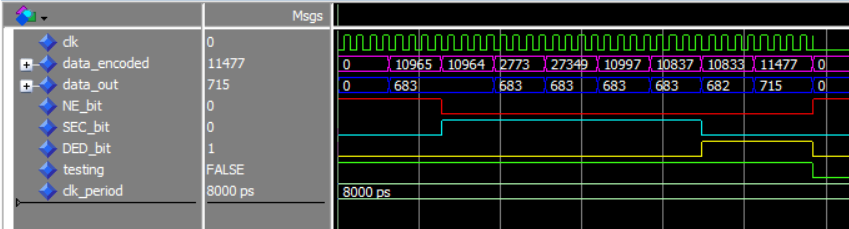
In the Figure 12 is shown the output of the decoder simulation obtained with Modelsim.

Figure 12 - Decoder simulation

## Final test

**library** IEEE**;**

**use** IEEE**.**std\_logic\_1164**.all;**

--entity declaration

**entity** Enc\_Dec\_tb **is**

**end** Enc\_Dec\_tb**;**

--architecture body

**architecture** rtl **of** Enc\_Dec\_tb **is**

**constant** clk\_period **:** time **:=** 8 ns**;**

**component** Encoder **is**

**port(**

data\_in **:** **in** std\_logic\_vector**(**10 **downto** 0**);**

data\_encoded **:** **out** std\_logic\_vector**(**15 **downto** 0**)**

**);**

**end** **component;**

**component** Decoder **is**

**port(**

data\_encoded **:** **in** std\_logic\_vector**(**15 **downto** 0**);**

data\_out **:** **out** std\_logic\_vector**(**10 **downto** 0**);**

NE\_bit **:** **out** std\_logic**;**

SEC\_bit **:** **out** std\_logic**;**

DED\_bit **:** **out** std\_logic

**);**

**end** **component;**

**signal** clk **:** std\_logic **:=** '0'**;**

**signal** data\_in**:** std\_logic\_vector**(**10 **downto** 0**)** **:=** **(others** **=>**

'0'**);**

**signal** data\_encoded\_out**:** std\_logic\_vector**(**15 **downto** 0**)** **:=**

**(others** **=>** '0'**);**

**signal** data\_encoded\_in**:** std\_logic\_vector**(**15 **downto** 0**)** **:=**

**(others** **=>** '0'**);**

**signal** data\_out**:** std\_logic\_vector**(**10 **downto** 0**);**

**signal** NE\_bit **:** std\_logic**;**

**signal** SEC\_bit **:** std\_logic**;**

**signal** DED\_bit **:** std\_logic**;**

**signal** testing **:** boolean **:=** true**;**

**begin**

clk **<=** **not** clk **after** clk\_period**/**2 **when** testing **else** '0'**;**

i\_dut1**:** Encoder

**port** **map(**

data\_in **=>** data\_in**,**

data\_encoded **=>** data\_encoded\_out

**);**

i\_dut2**:** Decoder

**port** **map(**

data\_encoded **=>** data\_encoded\_in**,**

data\_out **=>** data\_out**,**

NE\_bit **=>** NE\_bit**,**

SEC\_bit **=>** SEC\_bit**,**

DED\_bit **=>** DED\_bit

**);**

stimulus **:** **process**

**begin**

data\_in **<=** **(others** **=>** '0'**);**

data\_encoded\_in **<=** **(others** **=>** '0'**);**

**wait** **for** 32 ns**;**

--assume that there was not an error

-- expected out -> data\_out= "01010101011" (683),

NE=1, SEC=DED=0

data\_in **<=** "01010101011"**;**

data\_encoded\_in **<=** data\_encoded\_out**;**

**wait** **for** 32 ns**;**

--assume that there was a single error in p16

-- expected out -> data\_out= "01010101011" (683),

NE=0, SEC=1, DED=0

data\_in **<=** "01010101011"**;**

data\_encoded\_in **<=** **not(**data\_encoded\_out**(**15**))** **&**

data\_encoded\_out**(**14 **downto** 0**);**

**wait** **for** 32 ns**;**

--assume that there was a single error in d10

-- expected out -> data\_out= "01010101011" (683),

NE=0, SEC=1, DED=0

data\_in **<=** "01010101011"**;**

data\_encoded\_in **<=** data\_encoded\_out**(**15 **downto** 14**)** **&**

**not(**data\_encoded\_out**(**13**))** **&**

data\_encoded\_out**(**12 **downto** 0**);**

**wait** **for** 32 ns**;**

--assume that there was a single error in d11

-- expected out -> data\_out= "01010101011" (683),

NE=0, SEC=1, DED=0

data\_in **<=** "01010101011"**;**

data\_encoded\_in **<=** data\_encoded\_out**(**15**)** **&**

**not(**data\_encoded\_out**(**14**))** **&**

data\_encoded\_out**(**13 **downto** 0**);**

**wait** **for** 32 ns**;**

--assume that there was a single error in d3

-- expected out -> data\_out= "01010101011" (683),

NE=0, SEC=1, DED=0

data\_in **<=** "01010101011"**;**

data\_encoded\_in **<=** data\_encoded\_out**(**15 **downto** 6**)** **&**

**not(**data\_encoded\_out**(**5**))** **&**

data\_encoded\_out**(**4 **downto** 0**);**

**wait** **for** 32 ns**;**

--assume that there was a single error in p8

-- expected out -> data\_out= "01010101011" (683),

NE=0, SEC=1, DED=0

data\_in **<=** "01010101011"**;**

data\_encoded\_in **<=** data\_encoded\_out**(**15 **downto** 8**)** **&**

**not(**data\_encoded\_out**(**7**))** **&**

data\_encoded\_out**(**6 **downto** 0**);**

**wait** **for** 32 ns**;**

--assume that there was a double error in p8 and d1

-- expected out -> data\_out=invalid info, NE=0, SEC=0,

DED=1

data\_in **<=** "01010101011"**;**

data\_encoded\_in **<=** data\_encoded\_out**(**15 **downto** 8**)** **&**

**not(**data\_encoded\_out**(**7**))** **&**

data\_encoded\_out**(**6 **downto** 3**)** **&**

**not(**data\_encoded\_out**(**2**))** **&**

data\_encoded\_out**(**1 **downto** 0**);**

**wait** **for** 32 ns**;**

--assume that there was a double error in d10 and d9

-- expected out -> data\_out=invalid info, NE=0, SEC=0,

DED=1

data\_in **<=** "01010101011"**;**

data\_encoded\_in **<=** data\_encoded\_out**(**15 **downto** 14**)** **&**

**not(**data\_encoded\_out**(**13**))** **&**

**not(**data\_encoded\_out**(**12**))** **&**

data\_encoded\_out**(**11 **downto** 0**);**

**wait** **for** 32 ns**;**

--assume that there was a double error in d4 and d7

-- expected out -> data\_out=invalid info, NE=0, SEC=0,

DED=1

data\_in **<=** "01010101011"**;**

data\_encoded\_in **<=** data\_encoded\_out**(**15 **downto** 11**)** **&**

**not(**data\_encoded\_out**(**10**))** **&**

data\_encoded\_out**(**9 **downto** 7**)** **&**

**not(**data\_encoded\_out**(**6**))** **&**

data\_encoded\_out**(**5 **downto** 0**);**

**wait** **for** 32 ns**;**

**wait** **until** **rising\_edge(**clk**);**

testing **<=** false**;**

**end** **process;**

**end** rtl**;**

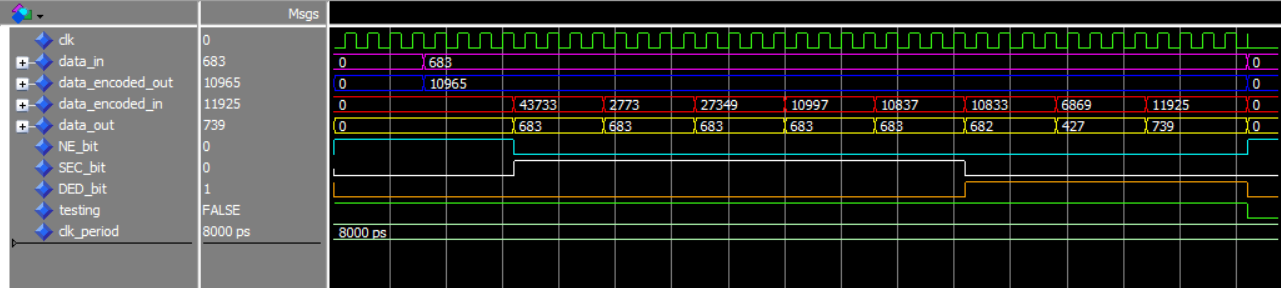
In the Figure 13 is shown the output of the final architecture simulation obtained with Modelsim.

Figure 13 - Architecture simulation

# Synthesis

In this chapter, will be presented the results obtained by creating a project with **Xilinx VIVADO** by selecting the **Zybo Zynq-7000** (xc7z010clg400-1) as working device. The Implementation phase has not been performed because it is not required from the assignment.

## RTL Analysis

Before heading with the Synthesis a preliminary double-check of the correctness of the system has been made by simply opening the schema obtained by the **Elaborated Design**. No problem has been found at this stage.

## Timing Report

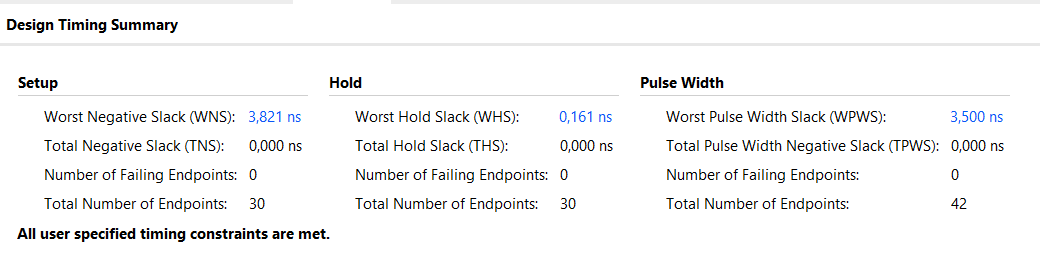
A timing constraint has been added (clock with period of 8ns), and after running the Synthesis command, the following Timing Report has been displayed (Figure 14):

Figure - Timing Report

As we can see, the Worst Negative Slack (WNS) is positive, so we can drive the board at a higher frequency than 125MHz. We can calculate the maximum frequency as:

Tclk is given by the Zybo Board, which operates with 125MHz and, for this reason, will grant a .

The WNS is determined by the Critical Path of the architecture, which is shown in the following picture (Figure 15):

We can state that the Decoder module for the output data calculation has the most impact on the critical path.

Figure 15 - Critical Path Report

## Resource Utilization Report

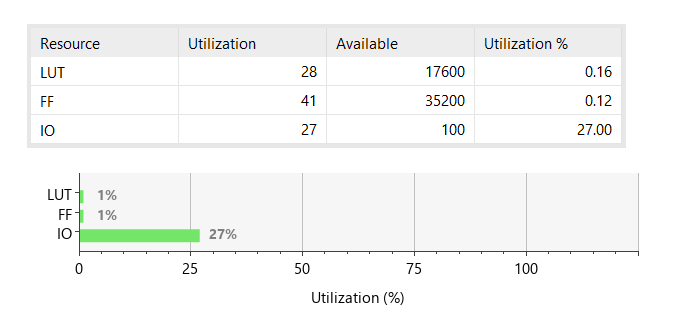
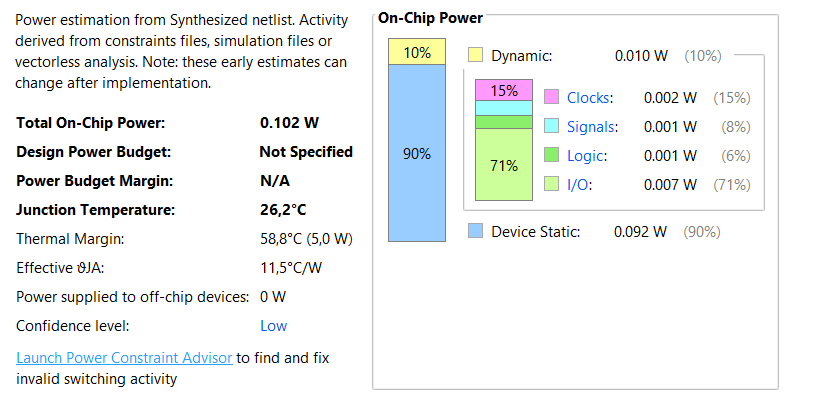
The resource utilized by the architecture synthesized are the following (Figure 16):

Figure 16 - Resource Utilization Report

## Power Consumption Report

The Power Consumption Report is the following (Figure 17):

***Figure 17 - Power Consumption Report*

As we can see, a total of 0.102W of power are needed, which is divided by 10% into dynamic power and 90% into static power. For the dynamic power, consumption the most relevant contribute is from the I/O.

## Warning Messages

# Conclusion

In general, this type of Error Correcting Code is very useful, as it is possible to detect two errors and correct one. It is, therefore, a simple solution to implement and rather effective, ideal for those applications which are not prone to errors in themselves and which require further control that is not too heavy.