

Computer Engineering

Electronic and Communication Systems

Error correction code

Project Report

Federica Perrone

Summary

[Introduction 3](#_Toc90138393)

[Overview of Hamming Code 3](#_Toc90138394)

[General Algorithm 4](#_Toc90138395)

[Hamming Encoder 5](#_Toc90138396)

[Hamming Decoder 5](#_Toc90138397)

[Extended Hamming Code 5](#_Toc90138398)

[Applications 5](#_Toc90138399)

[Architecture description 6](#_Toc90138400)

[Encoder Architecture 7](#_Toc90138401)

[Decoder Architecture 7](#_Toc90138402)

[VHDL Code 8](#_Toc90138403)

[Test-plan 9](#_Toc90138404)

[Synthesis 10](#_Toc90138405)

[Conclusion 11](#_Toc90138406)

# Introduction

An error correcting code is an algorithm for expressing a sequence of numbers such that any errors, which are introduced, can be detected and corrected (within certain limitations) based on the remaining numbers.

The error correcting codes are used for controlling errors in data over unreliable or noisy communication channels.

The central idea is the sender encodes the message with redundant information in the form of an ECC. The redundancy allows the receiver to detect a limited number of errors that may occur anywhere in the message, and often to correct these errors without retransmission.

The two main categories of ECC codes are block codes and convolutional codes.

Hamming codes are a family of linear error-correcting block codes. Richard Hamming invented Hamming codes in 1950 as a way of automatically correcting errors introduced by punched card readers. The scheme invented by Hamming adds additional parity bits (k) to the information bits (n), and can self-detect and self-correct any single-event effect (SEE) error that occurs during transmission. Once the location of the error is identified and located, the code inverts the bit, returning it to its original form.

Hamming codes form the foundation of other more complex error correction schemes. The original scheme allows **single-error correction single-error detection** (**SECSED**), but with an addition of one parity bit, an extended Hamming version allows **single-error correction and double-error detection** (**SECDED**).

The extended Hamming code is popular in computer memory systems.

## Overview of Hamming Code

Hamming codes tend to follow the process illustrated in Figure 1. The input is errorless information of n-bits long which is sent to the encoder. The encoder then applies Hamming theorems, calculates the parity bits (k), and attaches them to the received information data, to form a code word of (n + k)-bits. The processed information which contains additional parity bits is now ready for storage or transmission.

Figure 1- General layout of Hamming code

The decoder is responsible for checking and correcting any errors contained within the requested data. This is done by applying the Hamming theorem to calculate the syndrome. The decoder checks, locates, and corrects the errors contained in the code word before extracting the new error-free information data.

### General Algorithm

As mentioned previously, Hamming code uses parity bits to perform error detection and correction. Bit position (code word) is dependent on the amount of data bits protected. Parity bit positions are placed according to, 2 to the power of parity bit:

A general algorithm can be deduced from the following description:

1. Number the bits starting from 1: bit 1, 2, 3, 4, 5, 6, 7, etc.
2. Write the bit numbers in binary: 1, 10, 11, 100, 101, 110, 111, etc.
3. All bit positions that are powers of two (have a single 1 bit in the binary form of their position) are parity bits: 1, 2, 4, 8, etc. (1, 10, 100, 1000)
4. All other bit positions, with two or more 1 bits in the binary form of their position, are data bits.
5. Each data bit is included in a unique set of 2 or more parity bits, as determined by the binary form of its bit position:

* Parity bit 1 (P1) covers all bit positions which have the least significant bit set: bit 1 (the parity bit itself P1), 3, 5, 7, 9, etc. (all the odd numbers);
* Parity bit 2 (P2) covers all bit positions which have the second least significant bit set: bits 2 (P2), 3, 6, 7, 10, 11, etc. (sets of 2);
* Parity bit 4 (P4) covers all bit positions which have the third least significant bit set: bits 4 (P4), 5, 6, 7, 12, 13, 14, 15, etc. (sets of 4);
* Parity bit 8 (P8) covers all bit positions which have the fourth least significant bit set: bits 8 (P8), 9, 10, 11, 12, 13, 14, 15, etc. (sets of 8);
* Parity bit 16 (P16) covers all bit positions which have the fifth least significant bit set: bits 16 (P16), 17, 18, 19, 20, 21, 22, 23, etc. (sets of 16);

In the following table (Table 1), a typical code word layout is shown.

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Bit position | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |
| Encoded data bits | | **P1** | **P2** | **D1** | **P4** | **D2** | **D3** | **D4** | **P8** | **D5** | **D6** | **D7** | **D8** | **D9** | **D10** | **D11** | **P16** |
| Encoded data coverage | **P1** |  |  | ✓ |  | ✓ |  | ✓ |  | ✓ |  | ✓ |  | ✓ |  | ✓ |  |
| **P2** |  |  | ✓ |  |  | ✓ | ✓ |  |  | ✓ | ✓ |  |  | ✓ | ✓ |  |
| **P4** |  |  |  |  | ✓ | ✓ | ✓ |  |  |  |  |  | ✓ | ✓ | ✓ |  |
| **P8** |  |  |  |  |  |  |  |  | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |  |
| **P16** | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |

Table 1 - bit layout of Hamming code

The layout makes each column have a unique parity bit combination, for each bit position. This unique parity bit combination in known as the syndrome value. The syndrome allows errors to be located and corrected.

### Hamming Encoder

n

Encoder

n+k

Figure 2- Encoder block diagram

The Hamming encoder is responsible for generating the code word (n + k - bits long) from the information bits. Once generated the code word contains both the information bits and parity bits. The code word is calculated as shown in the following figure (Figure 2).

Information bits (n-bits)

XOR gate

Code word (n+ k-bits)

Figure 3 - Graphical expression of Hamming encoder

### Hamming Decoder

Figure 4- Decoder block diagram

n+k

Decoder

n

The Hamming decoder is responsible for generating the syndrome (r-bits long) from the code word (n +k -bits long). Once generated, the syndrome contains the error pattern that allows the error to be located and corrected. The syndrome is calculated as shown in the following figure.

Figure 5- Graphical expression of Hamming decoder

Code word (n + k-bits)

XOR gate

Syndrome (r-bits)

### Extended Hamming Code

The extended Hamming code makes use of an additional parity bit, which increases the Hamming code capabilities to SECDED.

In Table 1, P16 is the added parity bit that allows double error detection.

## Applications

The Error Correcting Codes (ECC), and more specifically Hamming codes, are used in many applications, such us:

* Telecommunication industry;
* Computer memory, modems and embedded processors;
* Nano Satellites.

# Architecture description

In this chapter will be discussed deeply the architecture of the Error Correcting Code (ECC).

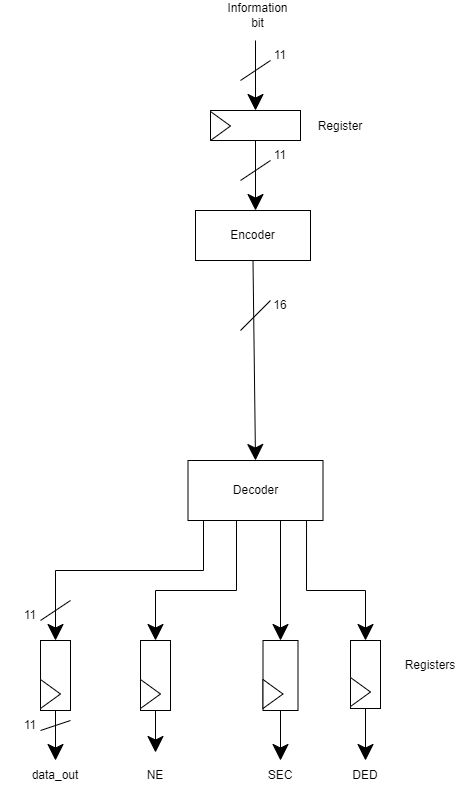
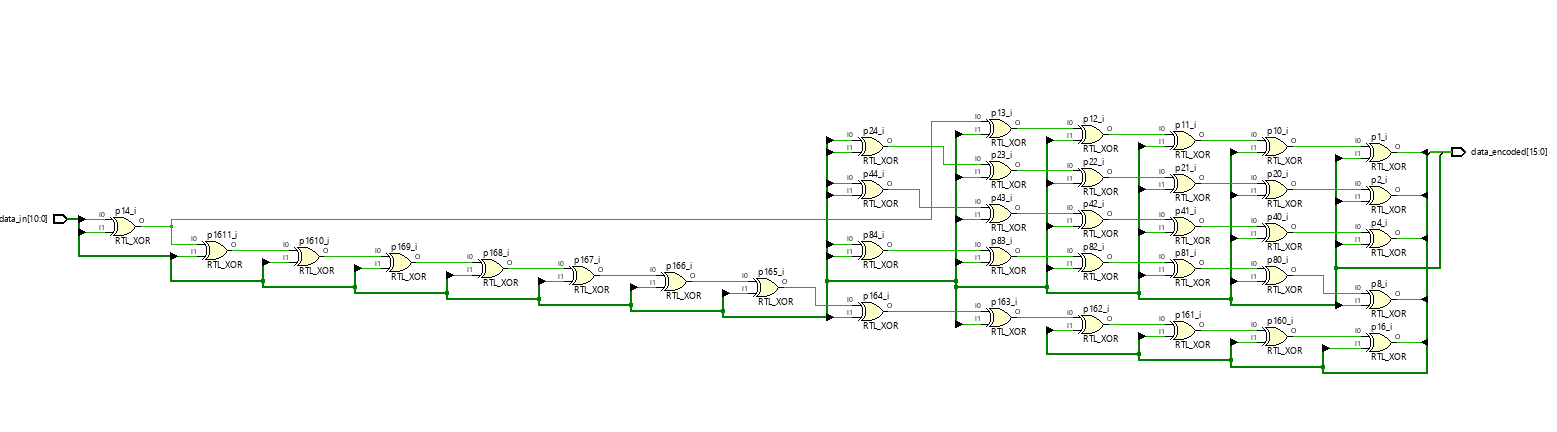
The general structure could be summarized by the following schema (Figure 6):

Figure 6- General schema

## Encoder Architecture

The data word (11 bits long) is applied as an input to the encoder circuit, which performs XOR operations on the given data word and thus the required parity bits (5 bits long) are generated. In this way, the output bits of the encoder consist 16 bits, i.e. 11-bits of data (from D1 to D11) and 5-bits of parity (P1, P2, P4, P8, P16).

The 5 parity bits, for 11 data bits, are calculated as follows:

## Decoder Architecture

# VHDL Code

# Test-plan

# Synthesis

# Conclusion