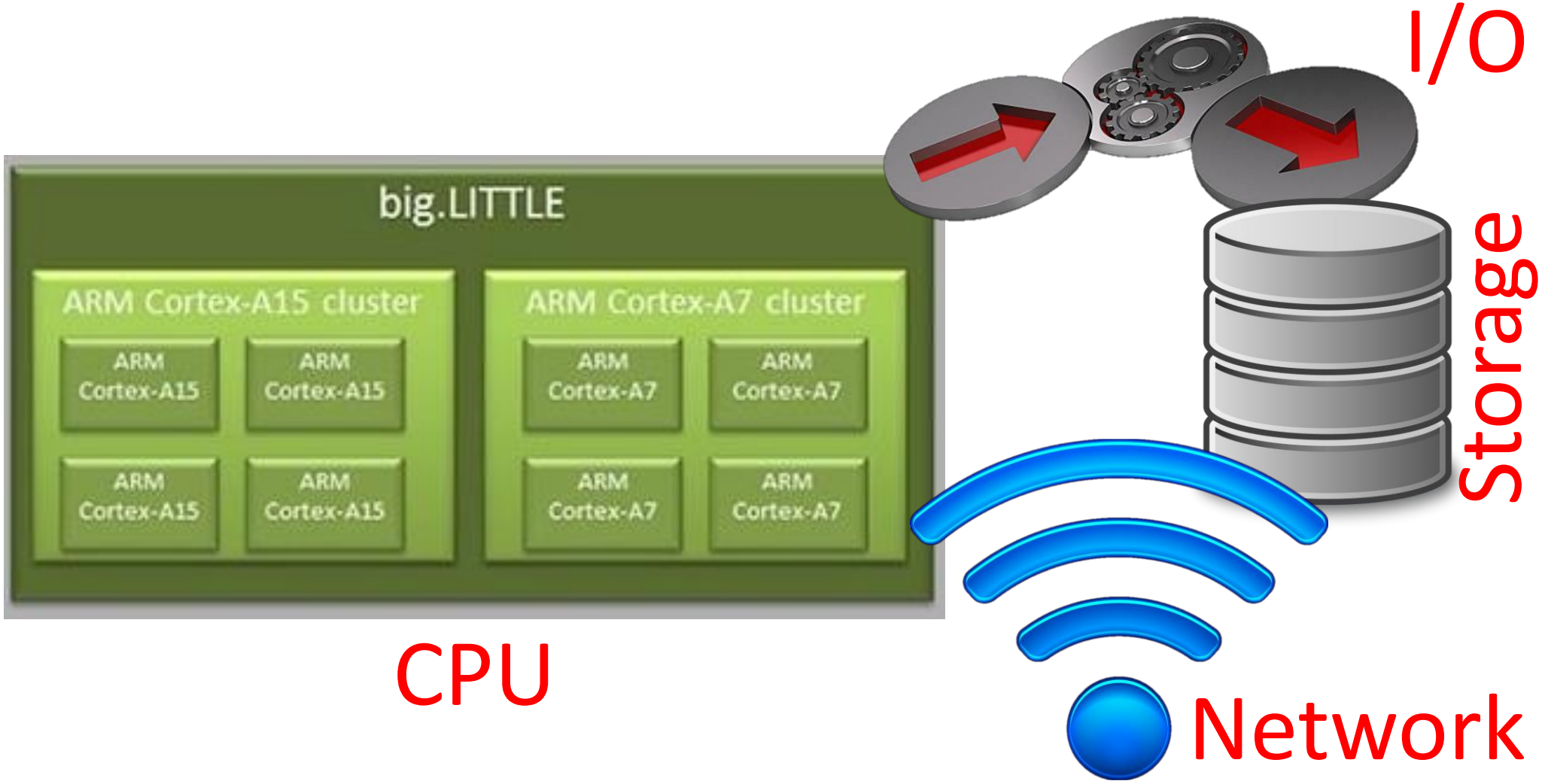
Performance Evaluation and Applications projects

2023 / 2024

Project Type B

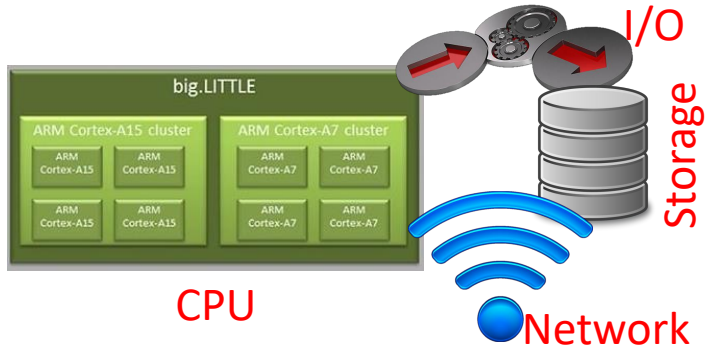
For students with ID (eight digits, “Codice Persona”) ending with 1 or 4

Performance of a Big-Little architecture



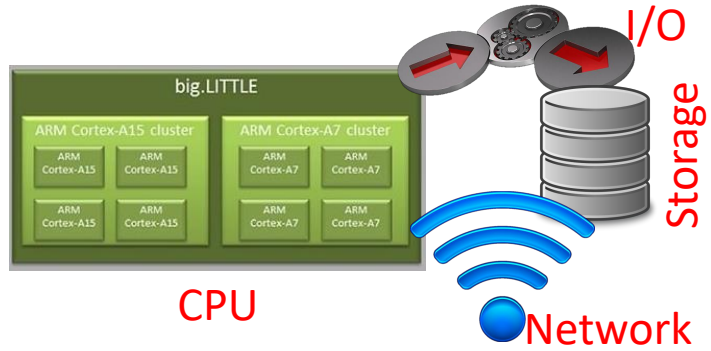
Performance of a Big-Little architecture

- A system characterized by a Big-Little architecture is characterized by *4 high performance* cores, and *8 energy efficient* cores.
- It is used by $N_B = 10$ heavy computation tasks, and $N_L = 32$ low computation tasks.
- The scheduler will mainly schedule heavy computation tasks on the high performance cores, while low computation tasks on the energy efficient cores. However, to better use the resources, there is also a small probability that tasks will be assigned the other way round.



Performance of a Big-Little architecture

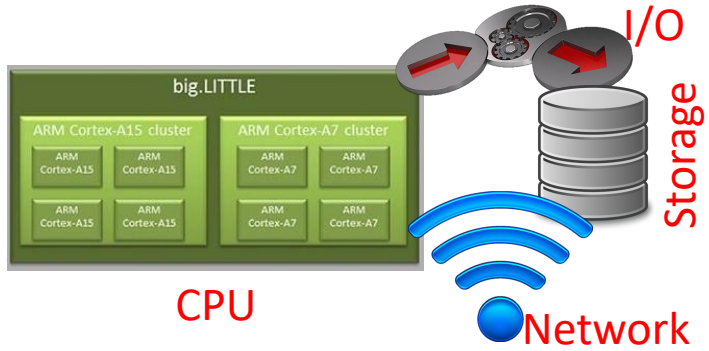
- The execution times of the tasks on the cores are collected in the following traces (all expressed in *sec*):



	High Performance Cores	Energy Efficient Cores
Heavy computation tasks	`TraceB-HH.txt`	`TraceB-HE.txt`
Low computation tasks	`TraceB-LH.txt`	`TraceB-LE.txt`

Performance of a Big-Little architecture

- The system is also composed by an *I/O subsystem*, a *Storage* component and *Network* access.
- All these components can be considered working in processor sharing, with an exponential service time (different per type of job), whose average is described in these tables:



	I/O	Storage	Network
Heavy computation tasks	*50 msec*	*200 msec*	*5 msec*
Low computation tasks	*150 msec*	*10 msec*	*120 msec*

Performance of a Big-Little architecture

- Determine the *best assignment probability distribution*: test a few alternatives of probabilities of assigning a heavy computation task to an efficiency core and of assigning low computation task to a high performance core. Determine the system throughput in each scenario.

- Hint: the two sets of cores can be considered as two independent processor sharing stations.