Multi-Standard Modulator

Design a digital circuit that realises a system able to perform the ASK, FSK, and PSK modulations. Use a LUT-based (Look-Up Table) NCO (Numerically-Controlled Oscillator).

The interface of the circuit to be designed is as follows:

The main characteristics of the system are the following:

- The frequency and the phase are represented with N = 16 bits.
- The amplitude is represented with A = 4 bit.
- The output signal must be represented with O = 16 bits.
- The LUT is represented with P = 7 bits to reduce its resource usage.

You are requested to deal with the various possible error situations, documenting the choices made.

The final project report must contain:

- Introduction (circuit description, possible applications, possible architectures, etc.)
- Description of the architecture designed (block diagram, inputs/outputs, etc.)
- VHDL code (with detailed comments) to be attached to the report.
- Test strategy (Test-plan) and related Testbench for verification; a detailed, though not exhaustive, verification is required, including error situations and borderline cases of functioning
- Interpretation of the results obtained in the automatic synthesis/implementation on a Xilinx FPGA platform in terms of maximum clock frequency (critical path), elements used (slice, LUT, etc.) and estimated power consumption. Comment on any warning messages.
- Conclusions