First Assignment Report

Section 0

Theoretical Peak performance for laptop (Hp-Pavillion):

- CPU: Intel ® Core™ i7-7500U.
- Base frequency 2.70 GHz.
- 2 cores
- Floating point operations per cycle: 16 (Intel Kaby Lake architecture, https://en.wikipedia.org/wiki/FLOPS)

	Model	CPU	Frequency	Cores	Peak performance
Laptop	i7-7500U	1	2.70 GHz	2	86.4 GFLOPS

Sustained and theoretical peak performance for smartphone (Xiaomi Mi A1):

- CPU: Octa core Qualcomm Snapdragon 625.
- Frequency: 2 GHz.
- 2 FLOPS

	Model	Sustained performance	Matrix size	Peak performance	Memory
Smartphone	Qualcomm Snapdragon 625	1209 MFLOPS	2500	32 GFLOPS	4 GB

Top 500:

	Model	Performance	Top 500 year	Number 1 HPC system	Number of processors (TOP500)
Smartphone	Qualcomm Snapdragon 625	1209 MFLOPS	Until November 1994	Until 1985 (Cray-2, 1.9 GFLOPS)	4 (Cray 2)
Laptop	i7-7500U	86.4 GFLOPS	Until November 2001	Until November 1993 (Numerical Wind Tunnel Japan)	140 (Numerical Wind Tunnel Japan)

Section 1

Theoretical model for parallel sum of N numbers.

T_{comp} = Time to compute a floating point operation.

T_{read} = Time to read from file.

T_{comm}=Time for each processor to communicate a message.

Parallel algorithm (master-slave):

- Each processor reads N from input file → $P^* T_{read}$
- N/P sums over each processor (including master) → $T_{comp}*N/P$
- Slaves send partial sums → $(P-1)*T_{comm}$
- Master performs one final sum → $(P-1)*T_{comp}$

Final model: $T_p = P^* T_{read} + T_{comp}*(P-1+N/P) + (P-1)*T_{comm}$