Digital Systems (EE 204)

Assignment-1

3rd March, 2020

Instructions:

1. *This is an individual assignment hence, all of you should attempt it distinctly.*
2. *Copying the code OR submitting it with a mere change will fetch penalty.*
3. *The codes are to be submitted as PDF file on moodle by 5.00 PM of 13th Mar. 2020.*
4. *These codes shall be checked by compiling and executing on ModelSim.*

Q.1 Write a VHDL code to design an arithmetic and logic unit using logic gates that performs the following three operations:

1. 4-bit addition

2. 4-bit subtraction

3. 4-bit multiplication

Write a test bench that includes 10 input combinations for the above program.

Q.2 Write a VHDL code generates parity as 1 if the number of 1's a 4-bit long binary message is even and generates 0 otherwise. Use logic gates to design such parity generator. Also, write a VHDL code designing a circuit for parity checker which consider the 5-bit long binary signal (4-bit message + 1-bit parity) and generates 1 if the number of 1's in the 5-bit binary signal is even and 0 otherwise.

Motivation: If the parity checker generates '1' that means the message signal has error in it.
Assumption: Noise can change only 1-bit of the signal.

Q.3 Write a VHDL code for a 4X1 MUX. Write a test bench and observe the output. Implement the following function using the 4X1 MUX as component in the code.

$$F(A, B, C, D) = \sum(1,2,4,7,10,12,14,15)$$

Q.4 Write a VHDL code for a D-flipflop using behavioural modelling. Use the D-Flipflop as a component to design a 4-bit universal shift register that does the following operation:

A	**B**	**Operation**
1	1	Loads Parallel Data
1	0	Circular Left Shift
0	1	Circular Right Shift

Write a testbench along with a suitable clock input to observe the output.