

1. 1-process fsmd

The image displays two screenshots from a computer screen, showing the simulation and compilation of a 1-process fsmd.

Top Screenshot: ModelSim SE-64 10.5c

The ModelSim window shows the simulation of the fsmd. The left pane lists the objects, including fsm, datapath, lab1, and lab1_tb. The right pane shows the simulation results, including the waveform and the Messages window.

The Messages window displays the following text:

```
# Refreshing /home/UFAD/xuifei/project/lab1/work.asserted_bit_count_fsmd_1p
# Loading work.asserted_bit_count_fsmd_1p
VSIM 13> run -all
# Tests completed: 10002 passed, 0 failed
VSIM 14>
```

The bottom status bar shows the simulation time: 0 ps to 2088960 ps. The project is lab1, and the current time is 7.046,085 ns.

Bottom Screenshot: Quartus Prime Pro Edition

The Quartus Prime Pro Edition window shows the compilation flow for the fsmd. The left pane shows the Project Navigator, and the right pane shows the IP Catalog.

The Compilation Flow window displays the following steps:

- Compile Design
 - IP Generation (00:00:06)
 - Analysis & Synthesis (00:00:10)
 - Fitter
 - Fitter (Implement)
 - Plan
 - Early Place
 - Place
 - Route
 - Fitter (Finalize)
 - Timing Analysis (Signoff)
 - Power Analysis
 - Assembler (Generate programming files)

The Messages window displays the following text:

```
(46) Message
(0) found pre-synthesis snapshots for 1 partition(s)
(0) Synthesizing partition "root_partition"
(0) Timing-Driven Synthesis is running
(0) 1 registers lost all their fanouts during netlist optimizations.
(0) Implemented 130 device resources after synthesis - the final resource count might be different
(0) Successfully synthesized partition
(0) Saving post-synthesis snapshots for 1 partition(s)
(0) Quartus Prime Synthesis was successful. 0 errors, 0 warnings
(0) Quartus Prime Flow was successful. 0 errors, 0 warnings
System (7) Processing (29)
```

The bottom status bar shows the compilation progress: 100% 00:00:16.

2. 2-process fsmd

ModelSim SE-64 10.5c

File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help

Layout Simulate ColumnLayout Default

Objects

- WIDTH
- clk
- rst
- go
- in
- out
- done
- state_r
- next_state
- done_r
- next_done_r
- count_r
- next_count_r
- n_r
- next_n_r

Wave - Default

Msgs

Now: 7.046,085 ns Delta: 1

Transcript

```
sim:/asserted_bit_count_tb/DUT/n_r \
sim:/asserted_bit_count_tb/DUT/next_n_r
VSIM 22> run -all
# Tests completed: 10002 passed, 0 failed
VSIM 23>
```

0 ps to 1024 ns Project: lab1 Now: 7.046,085 ns Delta: 1 sim:/asserted_bit_count_tb/DUT

17°C Sunny

Quartus Prime Pro Edition - /home/UFAD/xufeifan/project/lab1/lab1 - asserted_bit_count @ece-312-sharp7

File Edit View Project Assignments Processing Tools Window Help

Project Navigator

Entity mbinator

Compilation Dashboard

Project Overview

Compilation Flow: During compilation, intermediate Fitter snapshots (planned, placed, routed, and retimed) are

- Compile Design
 - IP Generation 00:00:06
 - Analysis & Synthesis 00:00:12
 - Fitter
 - Fitter (Implement)
 - Plan
 - Early Place
 - Place
 - Route
 - Fitter (Finalize)
 - Timing Analysis (Signoff)
 - Power Analysis
 - Assembler (Generate programming files)

IP Catalog

Installed IP

- Project Directory
 - No Selection Available
- Library
 - Basic Functions
 - Bridges and Adapters
 - DSP
 - Intel FPGA Interconnect
 - Interface Protocols
 - Memory Interfaces and Control
 - Processors and Peripherals
 - University Program

Search for Partner IP

Messages

Message

Expanded entity and wildcard assignments. Elapsed time: 00:00:00

- found pre-synthesis snapshots for 1 partition(s)
- Synthesizing partition "root_partition"
- Timing-Driven Synthesis is running
- 1 registers lost all their fanouts during netlist optimizations.
- Implemented 130 device resources after synthesis - the final resource count might be different
- Successfully synthesized partition
- Saving post-synthesis snapshots for 1 partition(s)
- Quartus Prime Synthesis was successful. 0 errors, 0 warnings

System (13) Processing (22)

100% 00:00:12

17°C Sunny

11:02 AM 2/14/2023

3. fsm_plus_d

ModelSim SE-64 10.5c

File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help

Layout Simulate ColumnLayout Default

Wave - Default

Objects

Instance

asserted_bit_count

model

generate_clock

#ublk#1843528

DUT

CONTROLLER

DATAPATH

std

#vim_capacity#

Width

clk

rst

go

in

out

done

n_en

count_en

count_sel

n_sel

out_en

Messages (Active)

Name

Now: 946065000 ps

Cursor 1: 1521000 ps

Transcript

sim:/asserted_bit_count_tb/DUT/out_en \

sim:/asserted_bit_count_tb/DUT/n_eq_0

VSIM 27> run -all

Tests completed: 10002 passed, 0 failed

VSIM 28>

0 ps to 1310720 ps

Project : lab1

Now: 6.946,065 ns

Delta: 1

sim:/asserted_bit_count_tb/DUT

17°C Sunny

Search

Q Quartus Prime Pro Edition - /home/UFAD/xufeifan/project/lab1/lab1 - asserted_bit_count @ece-312-sharp7

File Edit View Project Assignments Processing Tools Window Help

Search Intel FPGA

Project Navigator

Instance

Entity

mbinat

Cyclone 10 GX: 10CX22...

asserted_bit_count

83 (0)

top

asserted_bit_count_fsm_plus_d

83 (0)

Hierarchy

Files

Design Units

IP Components

Tasks

Project

Revisions...

Project Files

New...

Open...

Add/Remove Files in Project...

Platform Designer

IP Catalog

Compilation Dashboard

Project Overview

Compilation Flow: During compilation, intermediate Fitter snapshots (planned, placed, routed, and retimed) are

Compile Design

IP Generation 00:00:06

Analysis & Synthesis 00:00:10

Fitter

Fitter (Implement)

Plan

Early Place

Place

Route

Fitter (Finalize)

Timing Analysis (Signoff)

Power Analysis

Assembler (Generate programming files)

IP Catalog

Filter

Project Directory

No Selection Available

Library

Basic Functions

Bridges and Adapters

DSP

Intel FPGA Interconnect

Interface Protocols

Memory Interfaces and Control

Processors and Peripherals

University Program

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Messages

Message

Expanding entity and wildcard assignments.

Expanded entity and wildcard assignments. Elapsed time: 00:00:00

found pre-synthesis snapshots for 1 partition(s)

Synthesizing partition "root_partition"

Timing-Driven Synthesis is running

Implemented 133 device resources after synthesis - the final resource count might be different

Successfully synthesized partition

Saving post-synthesis snapshots for 1 partition(s)

Quartus Prime Synthesis was successful. 0 errors, 0 warnings

System (19)

Processing (21)

100% 00:00:10

19°C Sunny

Search

Q Quartus Prime Pro Edition - /home/UFAD/xufeifan/project/lab1/lab1 - asserted_bit_count @ece-312-sharp7

File Edit View Project Assignments Processing Tools Window Help

Search Intel FPGA

Project Navigator

Instance

Entity

mbinat

Cyclone 10 GX: 10CX22...

asserted_bit_count

83 (0)

top

asserted_bit_count_fsm_plus_d

83 (0)

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System (19)

Processing (21)

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19°C Sunny

Search

Q Quartus Prime Pro Edition - /home/UFAD/xufeifan/project/lab1/lab1 - asserted_bit_count @ece-312-sharp7

File Edit View Project Assignments Processing Tools Window Help

Search Intel FPGA

Project Navigator

Instance

Entity

mbinat

Cyclone 10 GX: 10CX22...

asserted_bit_count

83 (0)

top

asserted_bit_count_fsm_plus_d

83 (0)

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Search

4. datapath schematic

