SDLC METHODOLOGY

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SDLC METHODOLOGY

- SDLC is a process that consists of a series of planned activities to develop or alter the Software Products.
- It aims to produce a high-quality software that meets or exceeds customer expectations, reaches completion within times and cost estimates.
- ISO/IEC 12207 is an international standard for software life-cycle processes. It aims to be the standard that defines all the tasks required for developing and maintaining software.

WATERFALL MODEL

- First SDLC model introduced in software engineering.
- Referred to as a linear-sequential life cycle model.
- The whole process of software development is divided into separate phases.
- Each phase must be completed before the next phase can begin and there is no overlapping in the phases.

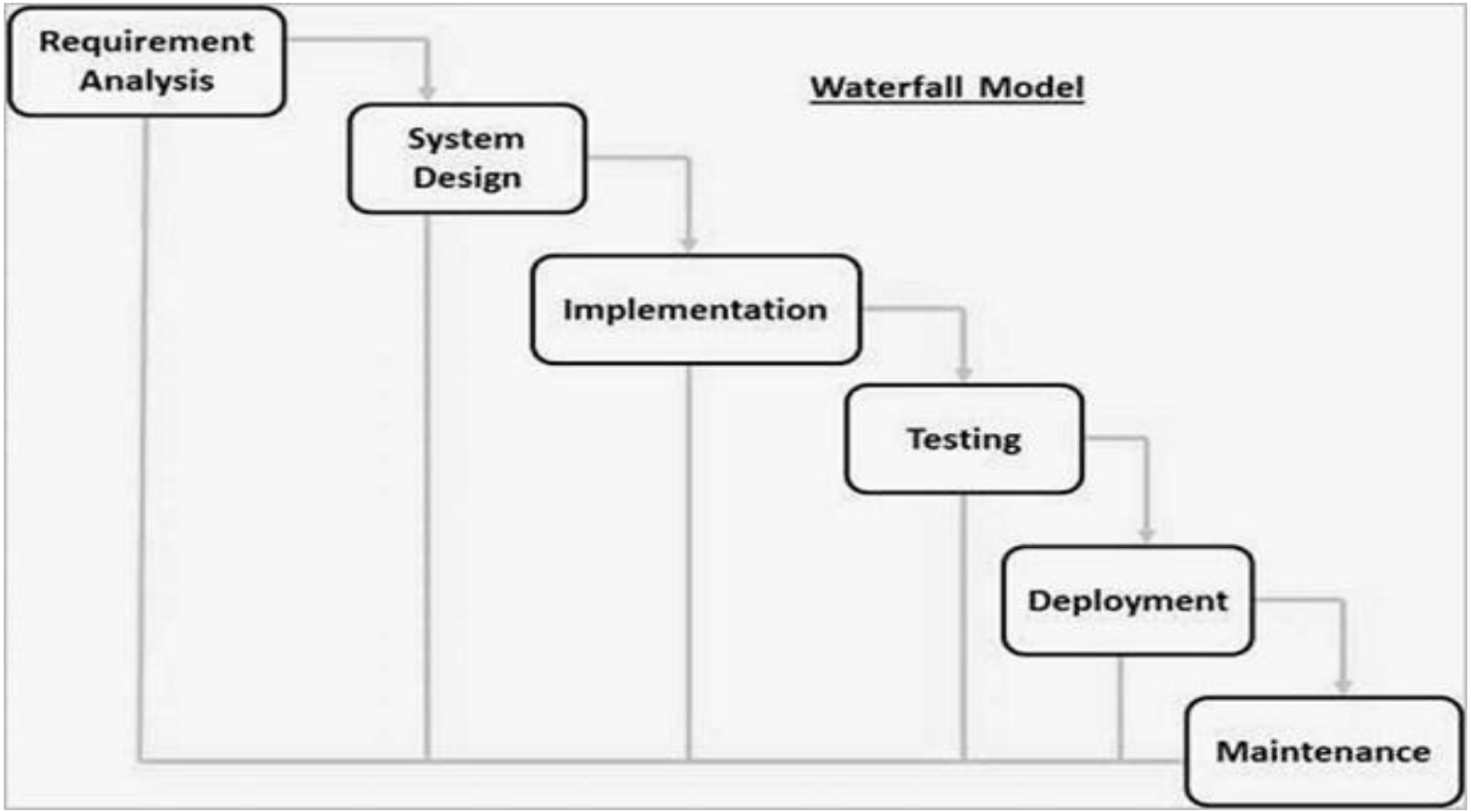

Figure 1 : Waterfall Model

Advantages of Waterfall Model

- Requirements are very well documented, clear and fixed.
- Phases are processed and completed one at a time.
- Works well for smaller projects where requirements are very well understood.

Disadvantages of Waterfall Model

- Cannot accommodate changing requirements.
- Poor model for long and ongoing projects.
- Not suitable for the projects where requirements are at a moderate to high risk of changing. So, risk and uncertainty is high with this process model.
- It is difficult to measure progress within stages.

V-MODEL

- SDLC model where execution of processes happens in a sequential manner in a V-shape. I
- Also known as Verification and Validation model.
- An extension of the waterfall model and is based on the association of a testing phase for each corresponding development stage.
- Under the V-Model, the corresponding testing phase of the development phase is planned in parallel.

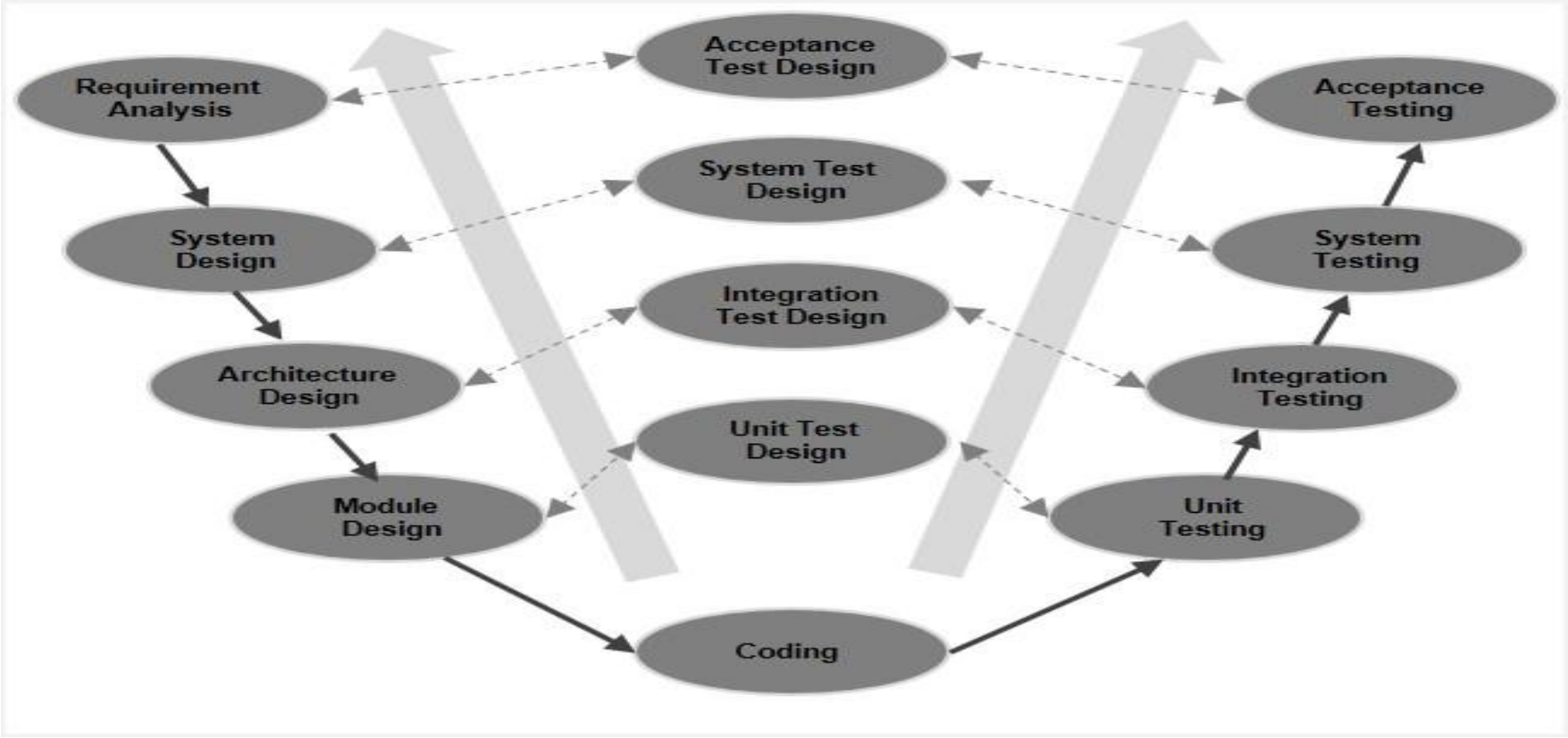

Figure 2 : V - Model

V-Model Phases

- Requirement Analysis & Acceptance Testing: This is the first phase in the development cycle where the product requirements are understood from the customer’s perspective. The acceptance test design planning is done at this stage as requirements can be used as an input for acceptance testing.
- System Design & System Testing : The system design will have the understanding and detailing the complete hardware and communication setup for the product under development. The system test plan is developed based on the system design. Doing this at an earlier stage leaves more time for the actual test execution later.
- Architectural Design & Integration Testing : The system design is broken down further into modules taking up different functionality. Integration tests can be designed and documented during this stage.Integration tests are performed to test the coexistence and communication of the internal modules within the system.

V-Model Phases…

- Module Design & Unit Testing : In this phase, the detailed internal design for all the system modules is specified, referred to as Low Level Design (LLD). The unit tests are an essential part of any development process and helps eliminate the maximum faults and errors at a very early stage.
- Coding Phase : The actual coding of the system modules designed in the design phase is taken up in the Coding phase. The best suitable programming language is decided based on the system and architectural requirements.

Advantages of V-Model

- Highly-disciplined model and phases are completed one at a time.
- Works well for smaller projects where requirements are very well understood.
- Simple and easy to understand and use.
- Easy to manage due to the rigidity of the model. Each phase has specific deliverables and a review process.

Disadvantages of V-Model

- Once an application is in the testing stage, it is difficult to go back and change a functionality.

CAN Message Transmission

1. Initialize the microcontroller.
2. Initialize the CAN Transceiver by clearing the RB2 pin and setting the RB3 pin.
3. Initialize the CAN control register (CANCON) for requesting the configuration mode.
4. Using CAN status register (CANSTAT) check CAN module is in configuration mode. If it is not in configuration mode then check continuously until it enters into configuration mode.
5. After CAN module enters into configuration mode, set the baud rate using CAN baud rate control registers.

CAN Message Transmission…

6. Initialize the CAN module i/o control register (CIOCON).
7. Initialize the CAN control register (CANCON) for requesting the normal mode.
8. Check if TXREQ bit is cleared and if it is normal mode and transmit buffer n.
9. Initialize the transmit buffer registers with Message ID, Data Length Code.
10. Configure transmitter buffer control register (TXBnCON) .
11. Call the delay function (1000ms).
12. Repeat the steps from step 8 to step 11 continuously.

Thank You