

28Pins

Variant: [No Variations]

20.03.2021  
v1I1

RELEASED 20-MAR-2021

Page	Index	Page	Index	Page	Index	Page	Index
1	COVER PAGE	11		21		31	
2	BLOCK DIAGRAM	12		22		32	
3	28PINS SCHEMATIC	13		23		33	
4	REVISION HISTORY	14		24		34	
5		15		25		35	
6		16		26		36	
7		17		27		37	
8		18		28		38	
9		19		29		39	
10		20		30		40	

DESIGN CONSIDERATIONS

DESIGN NOTE:  
Example text for informational  
design notes.

DESIGN NOTE:  
Example text for cautionary  
design notes.

DESIGN NOTE:  
Example text for debug notes.

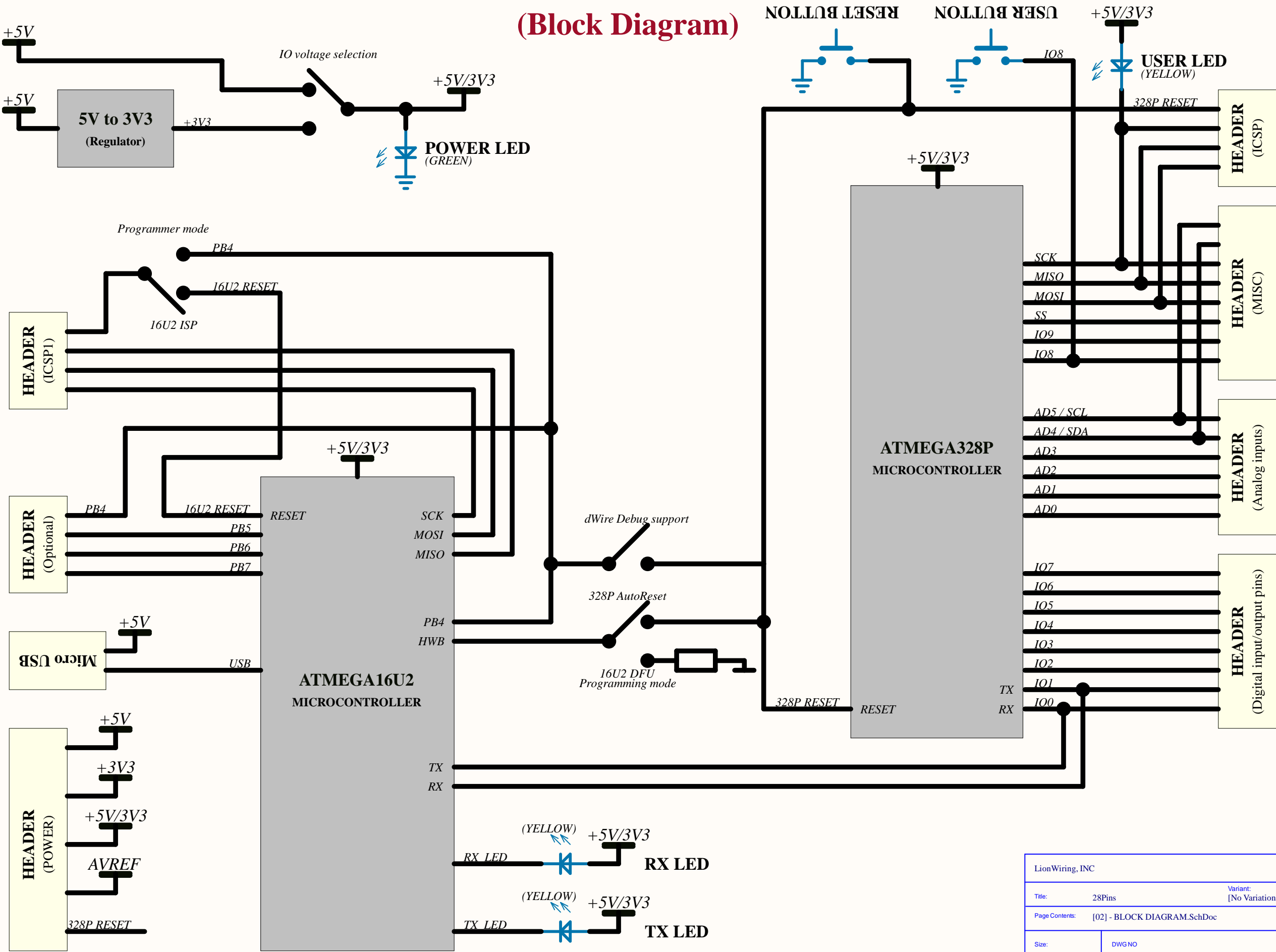
DESIGN NOTE:  
Example text for critical  
design notes.

LAYOUT NOTE:  
Example text for critical  
layout guidelines.

LionWiring, INC			
Title:	28Pins	Variant:	[No Variations]
Page Contents:	[01] - COVER PAGE.SchDoc		Checked by
Size:	DWG NO		Revision: v1I1
Date:	20.03.2021	Sheet	1 of 5

# 28Pins

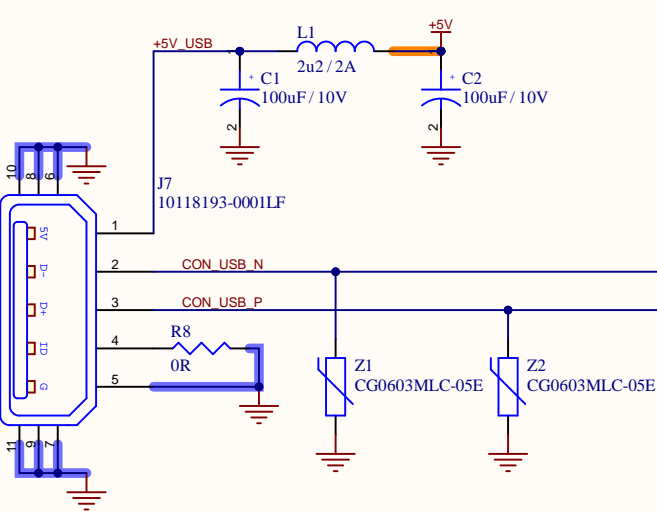
## (Block Diagram)



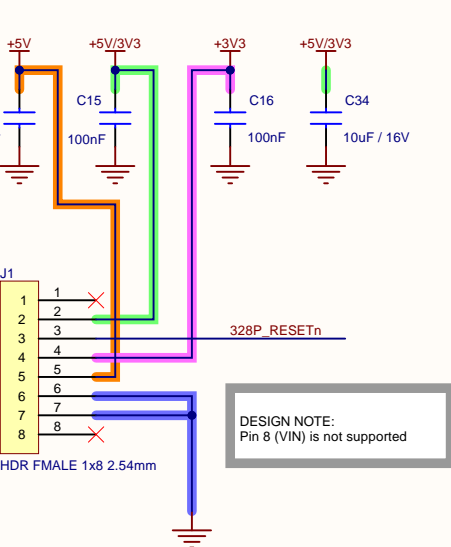
LionWiring, INC			
Title: 28Pins		Variant: [No Variations]	
Page Contents: [02] - BLOCK DIAGRAM.SchDoc			
Size:	DWG NO		Revision: vIII
Date: 20.03.2021		Sheet 2 of 5	

# 28Pins - SCHEMATIC

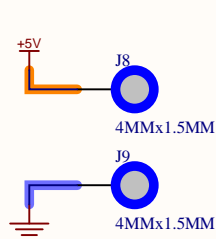
## Micro USB



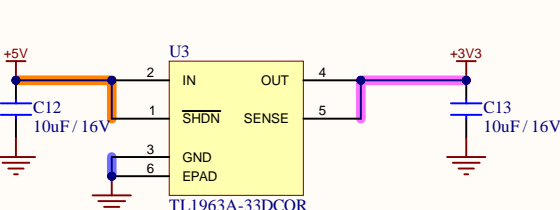
## POWER



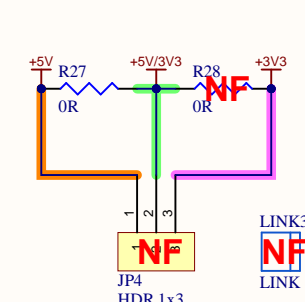
## POWER PADS



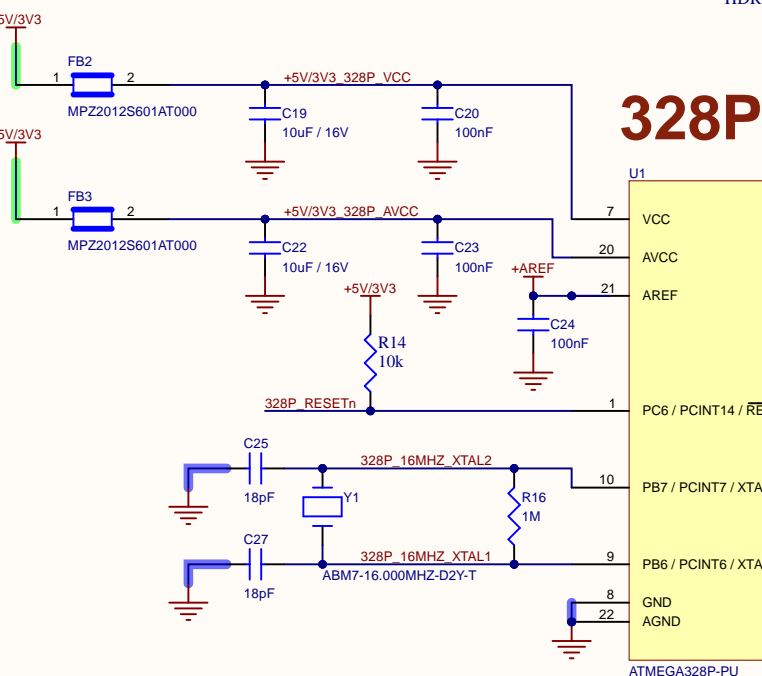
## 3V3 LDO



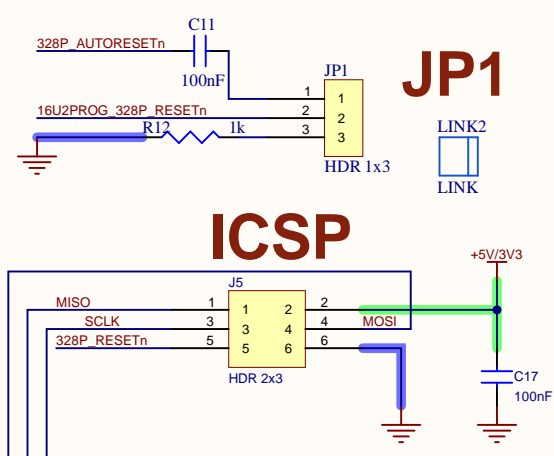
## Power Selection



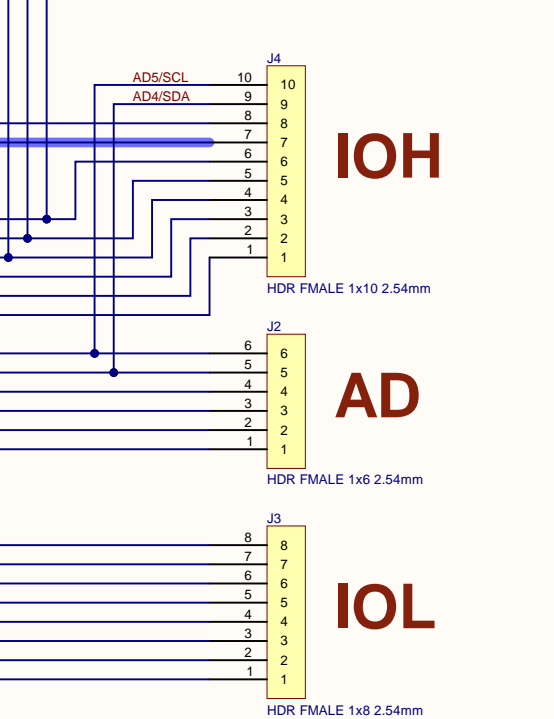
DESIGN NOTE:  
This board can be powered from micro USB connector (J7) or a single +3.3V power rail (through J1 pin 4). If +3.3V is used, fit R26 and R28. In this case, JP4 & R27 must NOT be fitted, otherwise the board may be damaged.



## 328P



## ICSP



## IOH

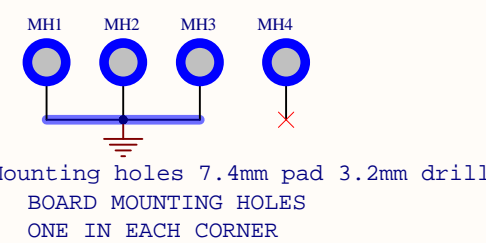
## AD

## IOL

## DIP SOCKET



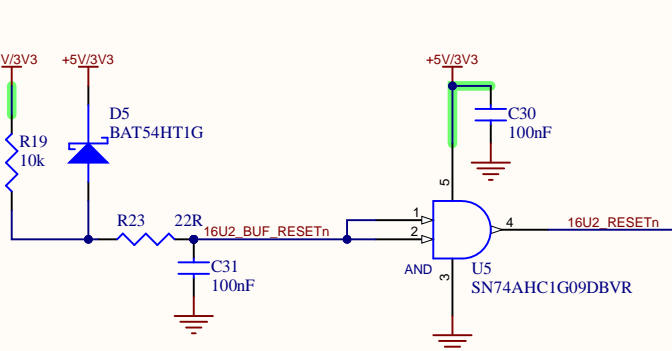
## MOUNTING HOLES



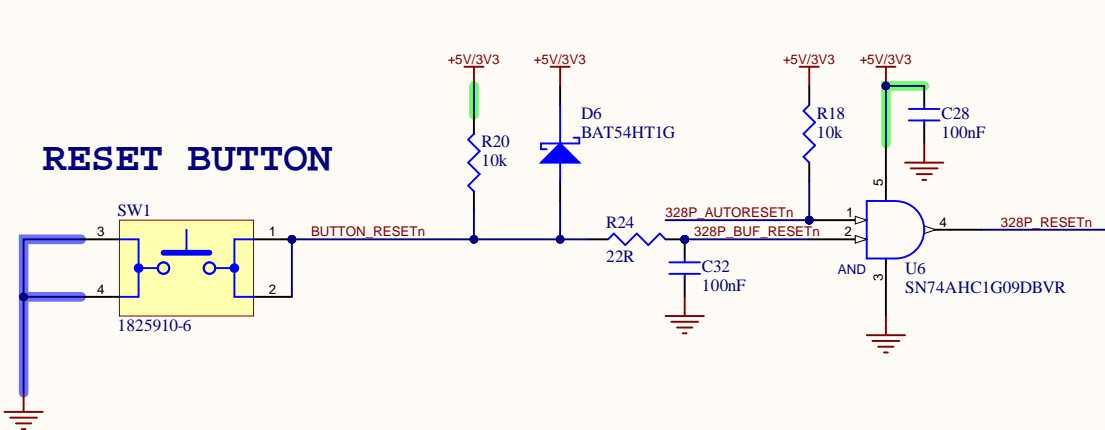
## FIDUCIALS



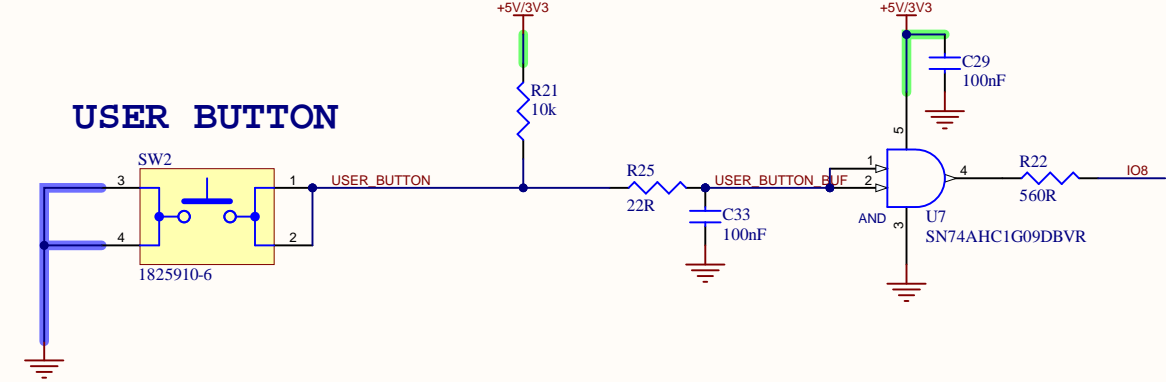
## RESET (16U2)



## RESET (328P)



## USER BUTTON



DESIGN NOTE:  
This board supports 5V or 3V3 voltage level on the IO pins:  
1) 5V IO - Fit everything as defined in this schematic. NF means do not fit this component.  
2) 3.3V IO - Remove R27, Fit R28, \*Replace Y1 (change from 16MHz to 10MHz), \*Replace Y2 (change from 16MHz to 8MHz).  
3) Both 5V and 3V3, selected through JP4 - Remove R27, Remove R28, Fit JP4, \*Replace Y1 (change from 16MHz to 10MHz), \*Replace Y2 (change from 16MHz to 8MHz).  
\*Note: The 16MHz crystals are not recommended for 3.3V operation. We need to adjust their values, that's why the change.  
IMPORTANT: Once you change the crystal value, you may need to re-compile your source code.

DESIGN NOTE:  
About JP3:  
1) DebugWire support - Short 1&2. This was added to support possible debugWire debugging (programming?) of 328P through 16U2. In this case, the 16U2 needs to have a correct firmware and has to behave as a debugWire tool.  
2) ISP programmer mode - Short 2&3. In this case, take a cable and connect J5 & J6 together. Upload AVRISP MKII firmware into 16U2 and you can program 328P. Example of AVRISP MKII firmware can be found at LUFA projects: <http://www.fourvalleddubicle.com/LUFA.php> (Tip: remap LEDs of the default AVRISP MKII LUFA project to the RX and TX LEDs on the 28Pin board)  
3) ISP header - Short 3 & 4. In this mode, the ICSP1 header is used as a standard ISP header to program 16U2 through ISP interface by an ISP programmer.

DESIGN NOTE:  
About JP1:  
1) Autoreset Enabled - Short 1&2. In this case, 16U2 is used to reset 328P when firmware inside 328P is updated from Arduino IDE.  
2) 16U2 DFU mode Enabled - Short 2&3. 16U2 HWB pin is sampled by 16U2 during RESET. If pulled low, then after Reset then 16U2 will go into DFU mode (it's the mode when you can flash 16U2 firmware through USB and Atmel Flip software: <http://www.atmel.com/tools/flip.aspx>).

LAYOUT NOTE:  
1) Route all the POWER tracks with minimum track width 0.4mm.  
2) Route all the other tracks by 0.4mm and change them by the end of the design to 0.2mm. To change all of them at once, use this filter  
(not InNet(".\*") and not InNet("GND")) and IsTrack and (OnLayer("L1") or OnLayer("L2")) and then set 0.2mm width in PCB Inspector panel.

LionWiring, INC		Variant: [No Variations]	
Title:	28Pins		
Page Contents:	[03] - 28PINS SCHEMATIC.SchDoc	Checked by	
Size:	DWG NO	Revision: vIII	
Date:	20.03.2021	Sheet 3 of 5	

1	2	3	4	5	6	7	8																																									
REVISION HISTORY																																																
A								A																																								
B								B																																								
C								C																																								
D							<table><tr><td colspan="8">LionWiring, INC</td></tr><tr><td>Title:</td><td colspan="2">28Pins</td><td colspan="5">Variant: [No Variations]</td></tr><tr><td>Page Contents:</td><td colspan="5">[04] - REVISION HISTORY.SchDoc</td><td colspan="2">Checked by</td></tr><tr><td>Size:</td><td colspan="5">DWG NO</td><td>Revision:</td><td>vIII</td></tr><tr><td>Date:</td><td colspan="3">20.03.2021</td><td>Sheet</td><td>4</td><td>of</td><td>5</td></tr></table>	LionWiring, INC								Title:	28Pins		Variant: [No Variations]					Page Contents:	[04] - REVISION HISTORY.SchDoc					Checked by		Size:	DWG NO					Revision:	vIII	Date:	20.03.2021			Sheet	4	of	5	D
LionWiring, INC																																																
Title:	28Pins		Variant: [No Variations]																																													
Page Contents:	[04] - REVISION HISTORY.SchDoc					Checked by																																										
Size:	DWG NO					Revision:	vIII																																									
Date:	20.03.2021			Sheet	4	of	5																																									
1	2	3	4	5	6	7	8																																									

	1	2	3	4	5	6	7	8
A	<div>Designator [01] - COVER PAGE.SchDoc</div> <div></div>	<div>Designator [02] - BLOCK DIAGRAM.SchDoc</div> <div></div>	<div>Designator [03] - 28PINS SCHEMATIC.SchDoc</div> <div></div>	<div>Designator [04] - REVISION HISTORY.SchDoc</div> <div></div>				
B								
C								
D							<div><div>LionWiring, INC</div><div><div>Title:</div>28Pins<div>Variant: [No Variations]</div></div><div><div>Page Contents:</div>28Pins_Project_V1111 Project.SchDoc<div>Checked by</div></div><div><div>Size:</div><div>DWG NO</div><div>Revision: v111</div></div><div><div>Date:</div>20.03.2021<div>Sheet 5 of 5</div></div></div>	
	1	2	3	4	5	6	7	8

# NOTES

Mark Not Fitted Components as  
**NF**

- DRAFT** - Very early stage of schematic, ignore details.
- PRELIMINARY** - Close to final schematic.
- CHECKED** - There should not be any mistakes. Tell the engineer if you find one.
- RELEASED** - A board with this schematic has been sent to production.