Path Summary

	Property	Value
1	From Node	FSM_Control:inst|U_Atual[0]
2	To Node	LEDR[15]
3	Launch Clock	CLOCK_50
4	Latch Clock	CLOCK_50
5	Data Arrival Time	8.159
6	Data Required Time	17.980
7	Slack	9.821

Statistics

	Property	Value	Count	Total Delay	% of Total	Min	Max
1	Setup Relationship	20.000					
2	Clock Skew	-3.029					
3	Data Delay	5.130					
4	Number of Logic Levels		0				
5	Physical Delays						
1	Arrival Path						
1	Clock						
1	IC		3	1.774	59	0.000	1.587
2	Cell		3	1.255	41	0.000	0.720
2	Data						
1	IC		1	0.000	0	0.000	0.000
2	Cell		3	4.921	96	0.000	4.461
3	uTco		1	0.209	4	0.209	0.209
2	Required Path						
1	Clock						
1	Clock Network (Lumped)		1	0.000		0.000	0.000

Data Path

Data Arrival

	Total	Incr	RF	Type	Fanout	Location	Element
1	0.000	0.000					launch edge time
2	3.029	3.029					clock path
1	0.000	0.000					source latency
2	0.000	0.000			1	PIN_Y2	CLOCK_50
3	0.000	0.000	RR	IC	1	IOIBUF_X0_Y36_N15	CLOCK_50~input|i
4	0.720	0.720	RR	CELL	1	IOIBUF_X0_Y36_N15	CLOCK_50~input|o
5	0.907	0.187	RR	IC	1	CLKCTRL_G4	CLOCK_50~inputclkctrl|inclk[0]
6	0.907	0.000	RR	CELL	27	CLKCTRL_G4	CLOCK_50~inputclkctrl|outclk
7	2.494	1.587	RR	IC	1	DDIOOUTCELL_X65_Y73_N11	inst|U_Atual[0]|clk
8	3.029	0.535	RR	CELL	1	DDIOOUTCELL_X65_Y73_N11	FSM_Control:inst|U_Atual[0]
3	8.159	5.130					data path

	Total	Incr	RF	Type	Fanout	Location	Element
1	3.238	0.209		uTco	1	DDIOOUTCELL_X65_Y73_N11	FSM_Control:inst|U_Atual[0]
2	3.698	0.460	RR	CELL	1	DDIOOUTCELL_X65_Y73_N11	inst|U_Atual[0]|q
3	3.698	0.000	RR	IC	1	IOOBUF_X65_Y73_N9	LEDR[15]~output|i
4	8.159	4.461	RR	CELL	1	IOOBUF_X65_Y73_N9	LEDR[15]~output|o
5	8.159	0.000	RR	CELL	0	PIN_G15	LEDR[15]

Data Required

	Total	Incr	RF	Type	Fanout	Location	Element
1	20.000	20.000					latch edge time
2	20.000	0.000					clock path
1	20.000	0.000	R				clock network delay
3	19.980	-0.020					clock uncertainty
4	17.980	-2.000	R	oExt	0	PIN_G15	LEDR[15]