

## Path Summary

	Property	Value
1	From Node	memory:inst altsyncram:altsyncram_component altsyncram_6ts3:auto_generated altsyncram_nar2:altsyncram1 q_a[6]
2	To Node	LEDR[9]
3	Launch Clock	CLK
4	Latch Clock	CLK
5	Data Arrival Time	10.523
6	Data Required Time	17.980
7	Slack	7.457

## Statistics

	Property	Value	Count	Total Delay	% of Total	Min	Max
1	Setup Relationship	20.000					
2	Clock Skew	-3.358					
3	Data Delay	7.165					
4	Number of Logic Levels		0				
5	Physical Delays						
1	Arrival Path						
1	Clock						
1	IC		3	1.750	52	0.000	1.563
2	Cell		3	1.608	48	0.000	0.914
2	Data						
1	IC		1	2.612	36	2.612	2.612
2	Cell		3	4.257	59	0.000	4.210
3	uTco		1	0.296	4	0.296	0.296
2	Required Path						
1	Clock						
1	Clock Network (Lumped)		1	0.000		0.000	0.000

## Data Path

### Data Arrival

	Total	Incr	RF	Type	Fanout	Location	Element
1	0.000	0.000					launch edge time
2	3.358	3.358					clock path
1	0.000	0.000					source latency
2	0.000	0.000			1	PIN_Y2	CLOCK_50
3	0.000	0.000	RR	IC	1	IOIBUF_X0_Y36_N15	CLOCK_50~input i
4	0.694	0.694	RR	CELL	1	IOIBUF_X0_Y36_N15	CLOCK_50~input o
5	0.881	0.187	RR	IC	1	CLKCTRL_G4	CLOCK_50~inputclkctrl inclk[0]
6	0.881	0.000	RR	CELL	51	CLKCTRL_G4	CLOCK_50~inputclkctrl outclk
7	2.444	1.563	RR	IC	20	M9K_X64_Y64_N0	inst altsyncram_component auto_generated altsyncram1 ram_block3a0 clk0
8	3.358	0.914	RR	CELL	1	M9K_X64_Y64_N0	memory:inst altsyncram:altsyncram_component altsyncram_6ts3:auto_generated altsyncram_nar2:altsyncram1 q_a[6]
3	10.523	7.165					data path
1	3.654	0.296		uTco	1	M9K_X64_Y64_N0	memory:inst altsyncram:altsyncram_component altsyncram_6ts3:auto_generated

	Total	Incr	RF	Type	Fanout	Location	Element
							altsyncram_nar2:altsyncram1 q_a[6]
2	3.701	0.047	RR	CELL	2	M9K_X64_Y64_N0	inst altsyncram_component auto_generated altsyncram1 ram_block3a0 portadataout[6]
3	6.313	2.612	RR	IC	1	IOOBUF_X83_Y73_N23	LEDR[9]~output i
4	10.523	4.210	RR	CELL	1	IOOBUF_X83_Y73_N23	LEDR[9]~output o
5	10.523	0.000	RR	CELL	0	PIN_G17	LEDR[9]

#### Data Required

	Total	Incr	RF	Type	Fanout	Location	Element
1	20.000	20.000					latch edge time
2	20.000	0.000					clock path
1	20.000	0.000	R				clock network delay
3	19.980	-0.020					clock uncertainty
4	17.980	-2.000	R	oExt	0	PIN_G17	LEDR[9]